QUARTUS II DESIGN SOFTWARE

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Fastest Path to Your Design

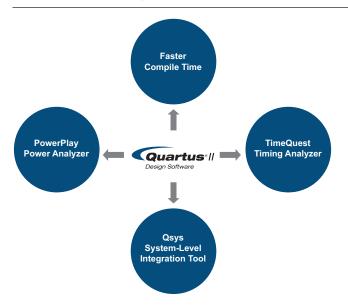
Quartus[®] II software is number one in performance and productivity for CPLD, FPGA, and SoC designs, providing the fastest path to convert your concept into reality. Quartus II software can easily adapt to your specific needs in all phases of FPGA and CPLD design in different platforms.

Quartus II software provides everything you need to design with Altera devices:

- Qsys system integration tool
- TimeQuest timing analyzer
- Transceiver Toolkit
- External Memory Interface Toolkit
- PowerPlay power analysis tools
- DSP Builder Advanced Blockset
- Altera SDK for OpenCL[™]
- ModelSim®-Altera Edition simulation software



Quartus II Software Key Features

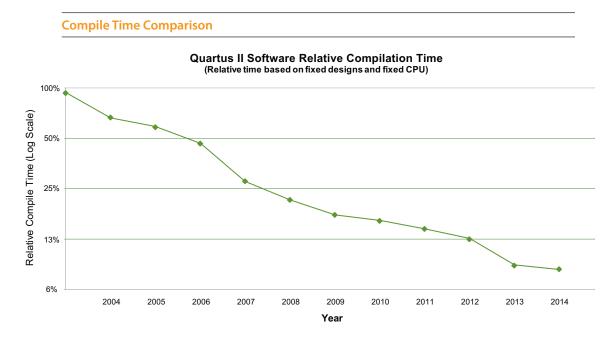


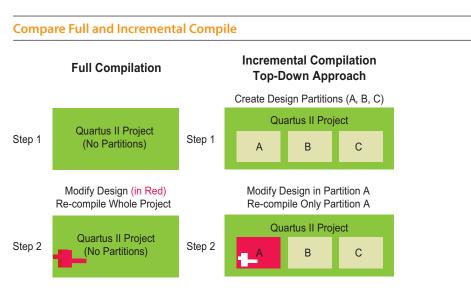
Industry-Leading Compile Time

Quartus II software delivers superior synthesis and placement and routing, resulting in compilation time advantages for both Web Edition and Subscription Edition software. Additional compilation time reduction features include the following:

- Multiprocessor support
- Incremental compile
- Advanced place-and-route algorithms





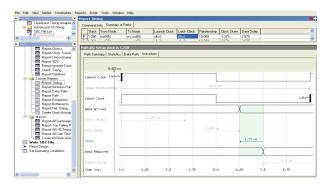


Incremental Compile

- Compiles only the changes in a partition to reduce compile time by up to 70 percent
- Preserves timing in unchanged partitions for performance preservation
- Enables team-based designs



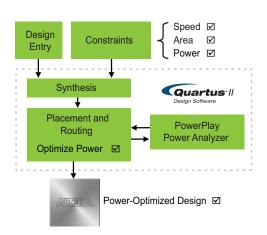
TimeQuest Timing Analyzer



TimeQuest Timing Analyzer GUI

- Comprehensive Synopsys® Design Constraints (SDC) support
- Second-generation, easy-to-use timing
 analyzer
- Complete GUI environment and scripting support to create timing constraints and reports
- Easy-to-use wizard to create SDC constraints

PowerPlay Power Analyzer Flow



PowerPlay Power Analyzer

- Push-button power optimization technology
- Automated power optimization for an average 10 percent reduction in power consumption



Qsys System Integration Tool

The Qsys system integration tool saves significant time and effort in the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions and subsystems. Qsys is powered by a new FPGA-optimized network-on-a-chip (NoC) technology, delivering higher performance, improved design reuse, and faster verification.

- High-performance Qsys interconnect based on the NoC architecture and automatic pipelining delivers up to 2X higher performance
- Hierarchical design flow enables scalable designs, supports team-based design, and maximizes design reuse
- Higher flexibility with support for mixing different industry-standard interfaces, such as the AMBA® AXI™, AMBA APB[™], AMBA AHB[™], and Avalon[®] interfaces
- IP management capabilities enable designs and systems to appear as an IP for easier reuse
- Faster board bring-up with a system-level debug approach using address-based transactions and System Console

Qsys – Altera's System Integration Tool





Quartus II Software Design Flow

	Quartus II Software Design Flow		
		Availability	
	Quartus II Software Key Features	Subscription Edition	Web Edition (Free)
Design Entry	Cyclone [®] FPGA and MAX [®] device support	1	1
	Arria [®] and Stratix [®] FPGA device support	1	\checkmark^1
	SoCs	1	1
	Multiprocessor support (faster compile time support)	1	√ ²
	IP Base Suite (includes licenses for 15 popular IP cores)	1	Available for purchase
	Qsys system integration tool	1	1
	Rapid Recompile (faster compile for small design changes)	1	
	Incremental compile (performance preservation and team-based design)	1	
Functional Simulation	ModelSim-Altera Starter Edition software	1	\checkmark
	ModelSim-Altera Edition software	√ ³	√ ³
Synthesis	Quartus Integrated Synthesis (synthesis tool)	1	1
Placement and Routing	Fitter (placement and routing tool)	1	1
Timing and Power Verification	TimeQuest tool (static timing analysis)	5	1
	PowerPlay tool and optimization (power analysis)	1	1
In-System Debug	SignalTap™ II Logic Analyzer (embedded logic analyzer)	1	√ ²
	Transceiver Toolkit (transceiver interface and verification tool)	1	
	JNEye link analysis tool	1	
System Design Software	Nios® II Embedded Design Suite	1	1
	Altera SDK for OpenCL	✓ ³	
	DSP Builder Advanced Blockset	✓3	√3
	Operating System Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 64 bit support	1	1

¹The only Arria II FPGA supported is the EP2AGX45 device.

² Available with TalkBack feature enabled.

³Requires an additional license.



Quartus II Software Ordering Information

Purchase Quartus II software and increase your productivity today.

Pricing	Description
\$2,995 (SW-QUARTUS-SE-FIX) Renewal \$2,495 (SWR-QUARTUS-SE-FIX)	Fixed-node license: subscription for one year—Windows only.
\$3,995 (SW-QUARTUS-SE-FLT) Renewal \$2,495 (SWR-QUARTUS-SE-FLT) Add seat \$3,995 (SW-QUARTUS-SE-ADD)	Floating-node license: subscription for one year—Windows/Linux.

ModelSim-Altera Edition Software				
\$945 (SW-MODELSIM-AE) Renewal \$945 (SWR-MODELSIM-AE)	ModelSim-Altera Edition software is available as a \$945 option for both Quartus II software Subscription Edition and Web Edition. It's 33 percent faster than Starter Edition, with no line limitation.			
ModelSim-Altera Starter Edition Software				
Free	Free for both Quartus II software Subscription Edition and Web Edition softwares with a 10,000 executable line limitation, ModelSim-Altera Starter Edition software is recommended for simulating small FPGA designs.			

Want to Dig Deeper?

Are you ready to accelerate your design process? Take these steps to gain proficiency in designing with Quartus II software:

Step 1: Download free Web Edition software www.altera.com/download

Step 2: Sign up for training

www.altera.com/training

Step 3: Download documentation www.altera.com/literature/lit-qts.jsp



MAIN CORPORATE OFFICES

Altera Corporation

101 Innovation Drive San Jose, CA 95134 USA Telephone: (408) 544 7000 www.altera.com

Altera European Headquarters

Holmers Farm Way High Wycombe Buckinghamshire HP12 4XF United Kingdom Telephone: (44) 1 494 602 000

Altera European Trading Company Ltd.

Building 2100 Cork Airport Business Park, Cork, Republic of Ireland Telephone: +353 21 454 7500

Altera Japan Ltd.

Shinjuku i-Land Tower 32F 6-5-1, Nishi Shinjuku Shinjuku-ku, Tokyo 163-1332 Japan Telephone: (81) 3 3340 9480 www.altera.co.jp

Altera International Ltd.

Unit 11- 18, 9/F Unit 11-18, 9/F Millennium City 1, Tower 1 388 Kwun Tong Road Kwun Tong Kowloon, Hong Kong Telephone: (852) 2945 7000 www.altera.com.cn

Altera Corporation Technology Center

Plot 6, Bayan Lepas Technoplex Medan Bayan Lepas 11900 Bayan Lepas Penang, Malaysia Telephone: 604 636 6100



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