TCS3471

Color Light-to-Digital Converter

General Description

The TCS3471 family of devices provides red, green, blue, and clear light sensing (RGBC) that detects light intensity under a variety of lighting conditions and through a variety of attenuation materials. An internal state machine provides the ability to put the device into a low power mode in between RGBC measurements providing very low average power consumption.

The TCS3471 is directly useful in lighting conditions containing minimal IR content such as LED RGB backlight control, reflected LED color sampler, or fluorescent light color temperature detector. With the addition of an IR blocking filter, the device is an excellent ambient light sensor, color temperature monitor, and general purpose color sensor.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3471, Color Light-to-Digital Converter are listed below:

Figure 1:
Added Value Of Using TCS3471

Benefits	Features
• Enables Accurate Color and Ambient Light Sensing Under Varying Lighting Conditions	• 1M:1 Dynamic Range
• Minimizes Motion / Transient Errors	• Four Independent Analog-to-Digital Converters
• Clear-Channel Provides a Reference Allows for Isolation of Color Content	• A Reference-Channel for Color Analysis (Clear Channel Photo-diode)
• Reduces Micro-Processor Interrupt Overhead	• Programmable Interrupt Function
• Reduces Board Space Requirements While Simplifying Designs	• Area Efficient 2mm x 2.4mm Dual Flat No-Lead (FN) Package

- Color Light Sensing
  - Programmable Analog Gain, Integration Time, and Interrupt Function with Upper and Lower Thresholds
  - Resolution Up to 16 Bits
  - Very High Sensitivity - Ideally Suited for Operation Behind Dark Glass
  - Up to 1,000,000:1 Dynamic Range

- Low Power Wait State
  - 65 µA Typical Current
  - Wait Timer is Programmable from 2.4 ms to > 7seconds
- Sleep Mode - 2.5 µA Typical Current
- I^2C Interface Compatible
  - Up to 400 kHz (I^2C Fast Mode)
- Dedicated Interrupt Pin
- Pin and Register Set Compatible with the TCS3x7x Family of Devices

Applications

TCS3471, Color Light-to-Digital Converter is ideal for:

- Color Temperature Sensing
- RGB LED Backlight Control
- Color Display Closed-Loop Feedback Control
- Ambient Light Sensing for Display Brightness Control
- Industrial Process Control
- Medical Diagnostics

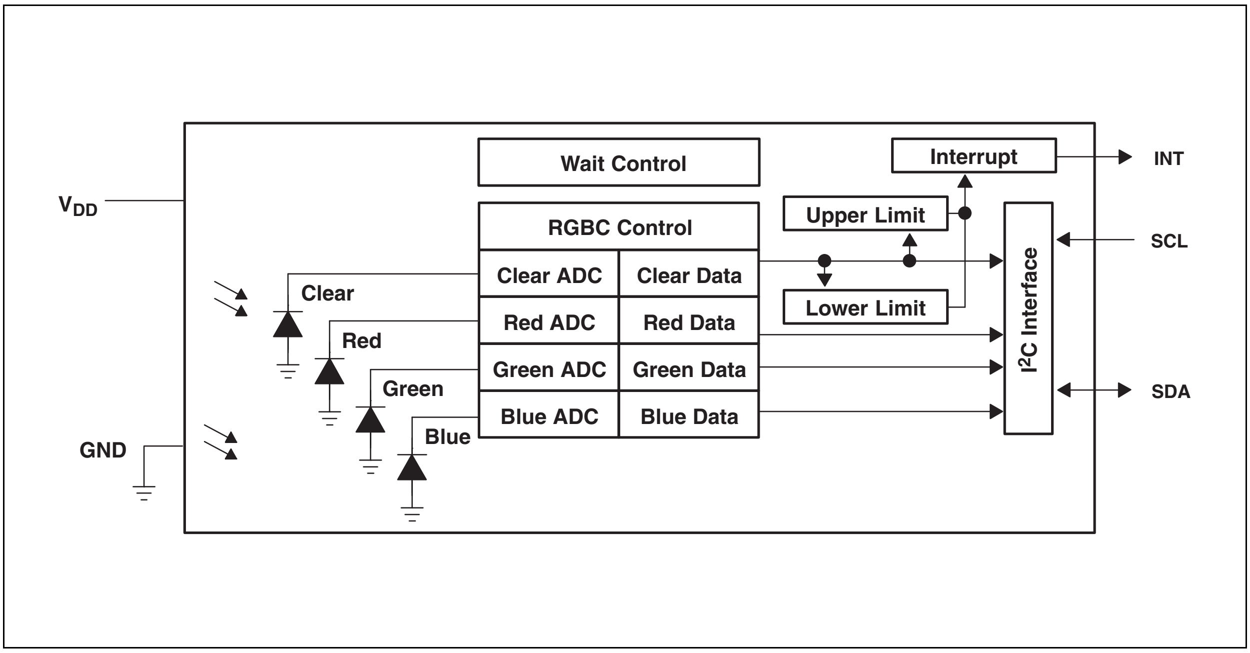
End Products and Market Segments

- HDTVs, Mobile Handsets, Tablets, Laptops, Monitors, PMP (Portable Media Payers)
- Medical Instrumentation
- Consumer Toys
- Industrial/Commercial Lighting

Functional Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TCS3471 Block Diagram



Pin Assignments

Figure 3:
Package FN Dual Flat No-Lead (Top View)

Pin Diagram:
Package Drawing Not to Scale

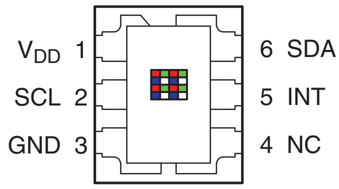


Figure 4:
Terminal Functions

Terminal		Type	Description
Name	No.		
V_{DD}	1		Supply voltage.
SCL	2	I	I^2C Serial clock input terminal - clock signal for I^2C serial data.
GND	3		Power supply ground. All voltages are referenced to GND.
NC	4		Do not connect
INT	5	O	Interrupt - open drain.
SDA	6	I/O	I^2C Serial data I/O terminal - serial data I/O for I^2C.

Detailed Description

The TCS3471 light-to-digital device contains a 4 × 4 photodiode array, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. The 4 × 4 photodiode array is composed of red-filtered, green-filtered, blue-filtered, and clear photodiodes — four of each type. Four integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. The transfers are double-buffered to ensure that the integrity of the data is maintained. Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller.

The TCS3471 provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. An interrupt is generated when the value of an RGBC conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{DD} (1)	Supply voltage		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{STRG}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.7	3	3.3	V
T_A	Operating free-air temperature	-30		70	°C

Figure 7:
Operating Characteristics; V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Active		235	330	µA
		Wait mode		65		
		Sleep mode - no I²C activity		2.5	10	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		−5		5	µA
I_{LEAK}	Leakage current, LDR pin		-1		+10	µA
V_{IH}	SCL, SDA input high voltage	TCS34711 & TCS34715	0.7 V_{DD}			V
		TCS34713 & TCS34717	1.25			
V_{IL}	SCL, SDA input low voltage	TCS34711 & TCS34715			0.3 V_{DD}	V
		TCS34713 & TCS34717			0.54	

Figure 8:
Optical Characteristics; V_{DD} = 3 V, T_A = 25°C, GAIN = 16, ATIME = 0xF6 (unless otherwise noted)

Parameter	Test Conditions	Red Channel		Green Channel		Blue Channel		Clear Channel			Unit
		Min	Max	Min	Max	Min	Max	Min	Typ	Max	
R_e Irradiance responsivtiy	λ_D = 465 nm(2)	0%	15%	10%	42%	65%	88%	19.2	24	28.8	counts/ (µW/cm²)
	λ_D = 525 nm(3)	8%	25%	60%	85%	9%	35%	22.4	28	33.6	
	λ_D = 625 nm(4)	85%	110%	0%	15%	5%	25%	27.2	34	40.8	

Note(s):

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda½$ = 22 nm, and luminous efficacy = 75 lm/W.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda½$ = 35 nm, and luminous efficacy = 520 lm/W.
4. The 625 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 625 nm, spectral halfwidth $\Delta\lambda½$ = 9 nm, and luminous efficacy = 155 lm/W.

Figure 9:
RGBC Characteristics; V_{DD} = 3 V, T_A = 25°C, AGAIN = 16, AEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
Dark ADC count value	Ee = 0, AGAIN = 60×, ATIME= 0xD6 (100 ms)	0	1	5	counts
ADC integration time step size	ATIME = 0xFF	2.27	2.4	2.56	ms
ADC number of integration steps		1		256	steps
ADC counts per step		0		1024	counts
ADC count value	ATIME = 0xC0 (153.6 ms)	0		65535	counts
Gain scaling, relative to 1× gain setting	4×	3.8	4	4.2	%
	16×	15	16	16.8	
	60×	58	60	63	

Figure 10:
Wait Characteristics; V_{DD} = 3 V, T_A = 25°C, Gain = 16, WEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Wait step size	WTIME = 0xFF		2.27	2.4	2.56	ms
Wait number steps			1		256	steps

Figure 11:
AC Electrical Characteristics; V_{DD} = 3 V, T_A = 25°C, (unless otherwise noted)

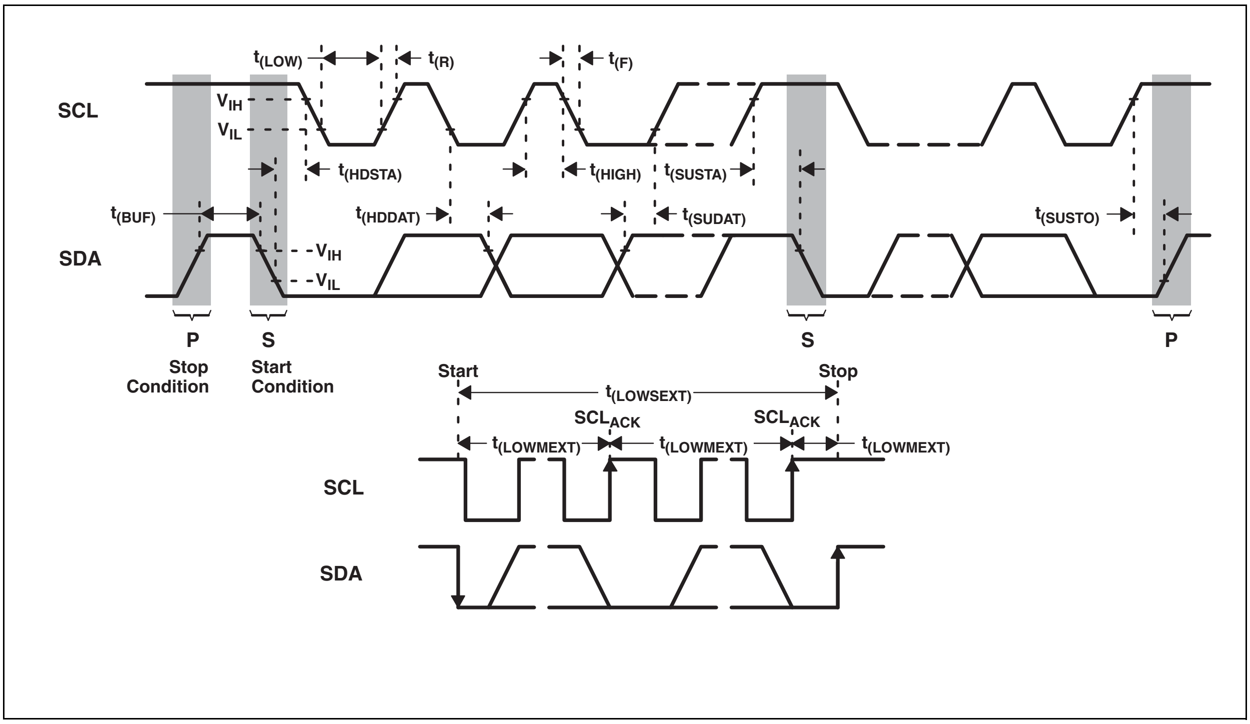
Symbol	Parameter[1]	Test Conditions	Min	Typ	Max	Unit
$f_{(SCL)}$	Clock frequency (I^2C)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			μs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			μs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			μs
$t_{(SUSTO)}$	Stop condition setup time		0.6			μs
$t_{(HDDAT)}$	Data hold time		0			μs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			μs
$t_{(HIGH)}$	SCL clock high period		0.6			μs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Parameter Measurement Information

Figure 12:
Timing Diagrams



Typical Operating Characteristics

Figure 13:
Photodiode Spectral Responsivity

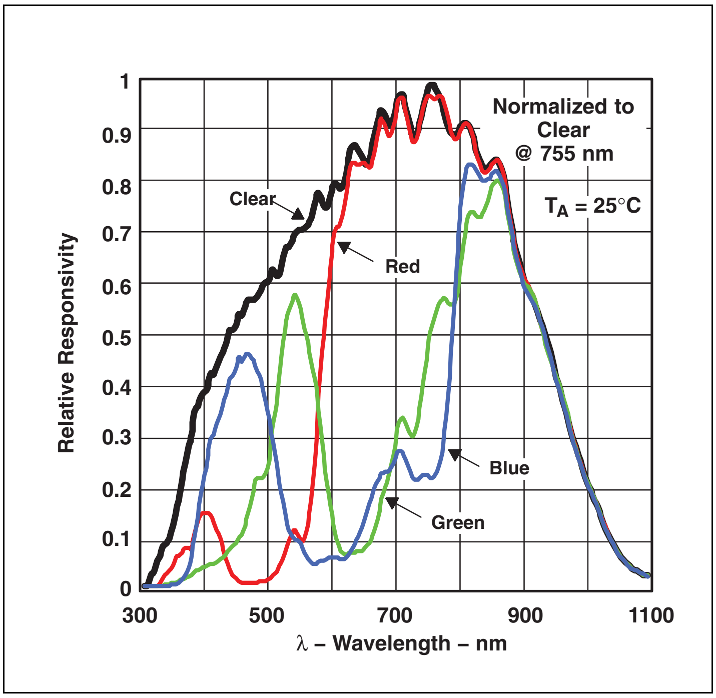


Figure 14:
Normalized I_{DD} vs.V_{DD} and Temperature

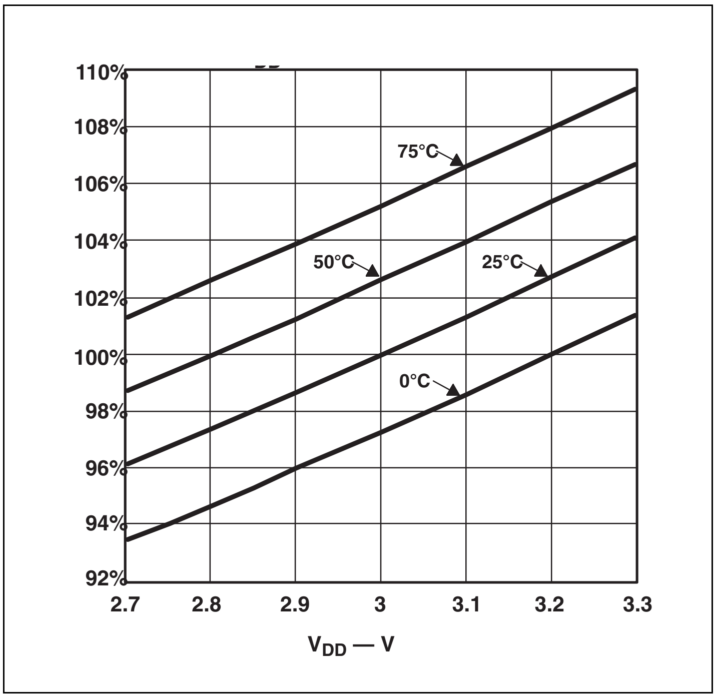


Figure 15:
Normalized Responsivity vs. Angular Displacement

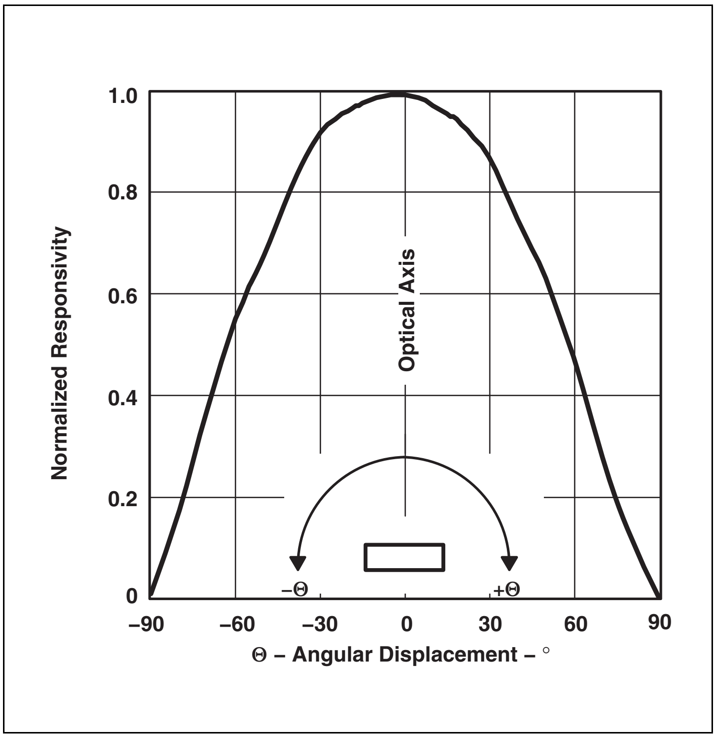
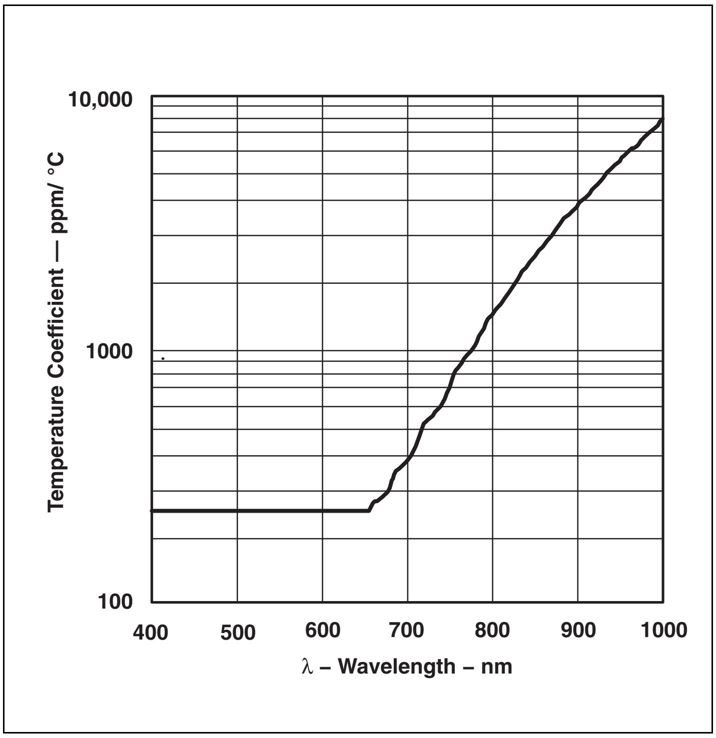


Figure 16:
Responsivity Temperature Coefficient

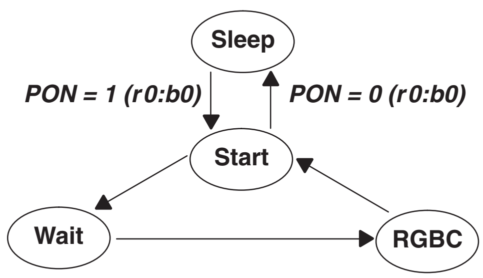


Principles Of Operation

System State Machine

The TCS3471 provides control of RGBC and power management functionality through an internal state machine (Figure 17). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Wait and RGBC states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

Figure 17:
Simplified State Diagram



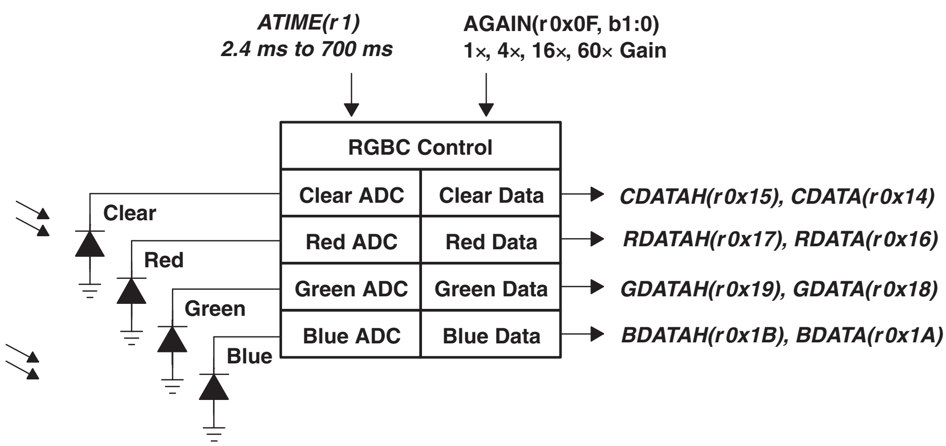
Note(s): In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

RGBC Operation

The RGBC engine contains RGBC gain control (AGAIN) and four integrating analog-to-digital converters (ADC) for the RGBC photodiodes. The RGBC integration time (ATIME) impacts both the resolution and the sensitivity of the RGBC reading. Integration of all four channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the color data registers. This data is also referred to as channel *count*.

The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

Figure 18:
RGBC Operation



The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

(EQ1) ATIME = 256 - Integration Time / 2.4 ms

Inversely, the time can be calculated from the register value as follows:

(EQ2) Integration Time = 2.4 ms × (256 - ATIME)

For example, if a 100ms integration time is needed, the device needs to be programmed to:

256 - (100 / 2.4) = 256 - 42 = 214 = 0xD6

Conversely, the programmed value of 0xC0 would correspond to:

(256 - 0xC0) × 2.4 = 64 × 2.4 = 154 ms.

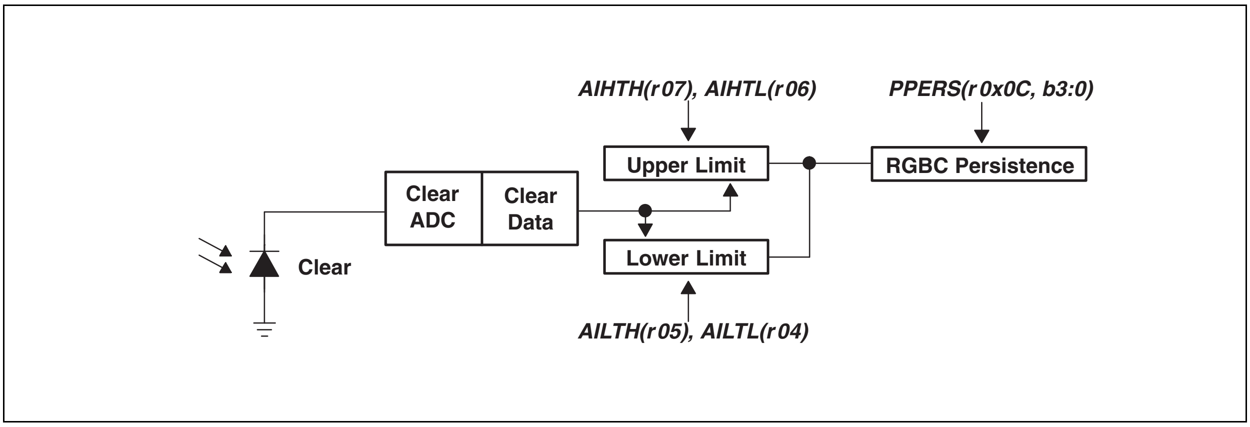
Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the RGBC interrupt enable (AIEN) field in the enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level range. An interrupt can be generated when the RGBC Clear data (CDATA) falls outside of the desired light level range, as determined by the values in the RGBC interrupt low threshold registers (AILTx) and RGBC interrupt high threshold registers (AIHTx). It is important to note that the low threshold value must be less than the high threshold value for proper operation.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range RGBC occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the persistence (APERS) value. See the Persistence Register (0x0C) for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see Command Register).

Figure 19:
Programmable Interrupt

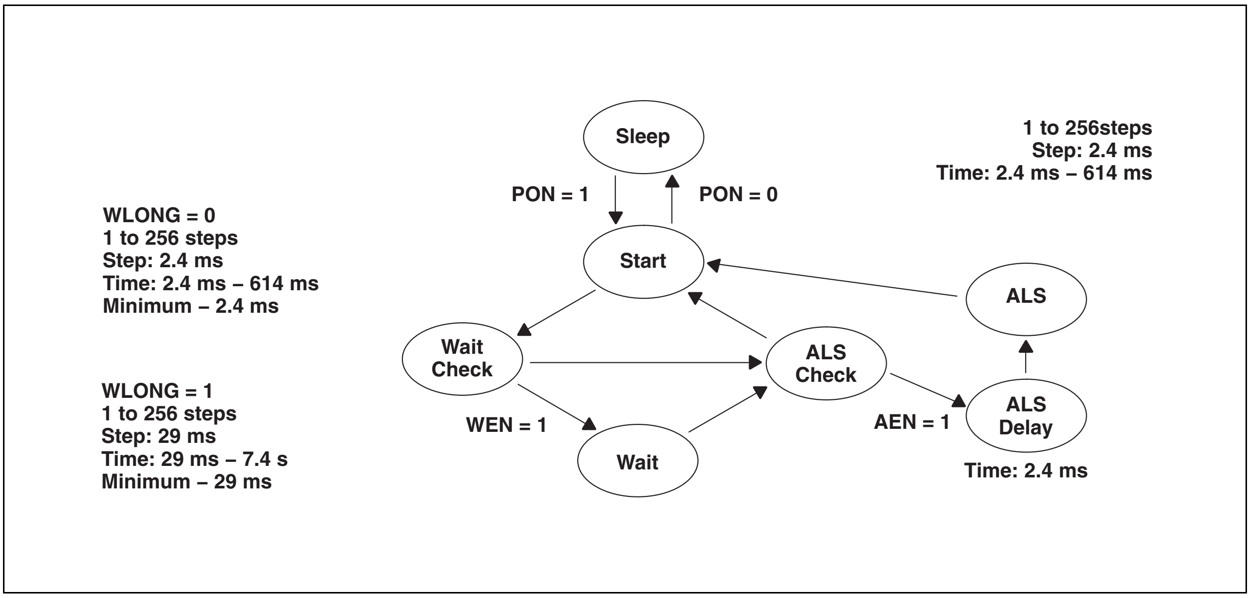


State Diagram

Figure 20 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.4ms delay will occur before entering the start state. If the WEN bit is set, the state machine will cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will step to the RGBC state.

The AEN should always be set. In this case, a minimum of 1 integration time step should be programmed. The RGBC state machine will continue until it reaches the terminal count, at which point the data will be latched in the RGBC register and the interrupt set, if enabled.

Figure 20:
Expanded State Diagram



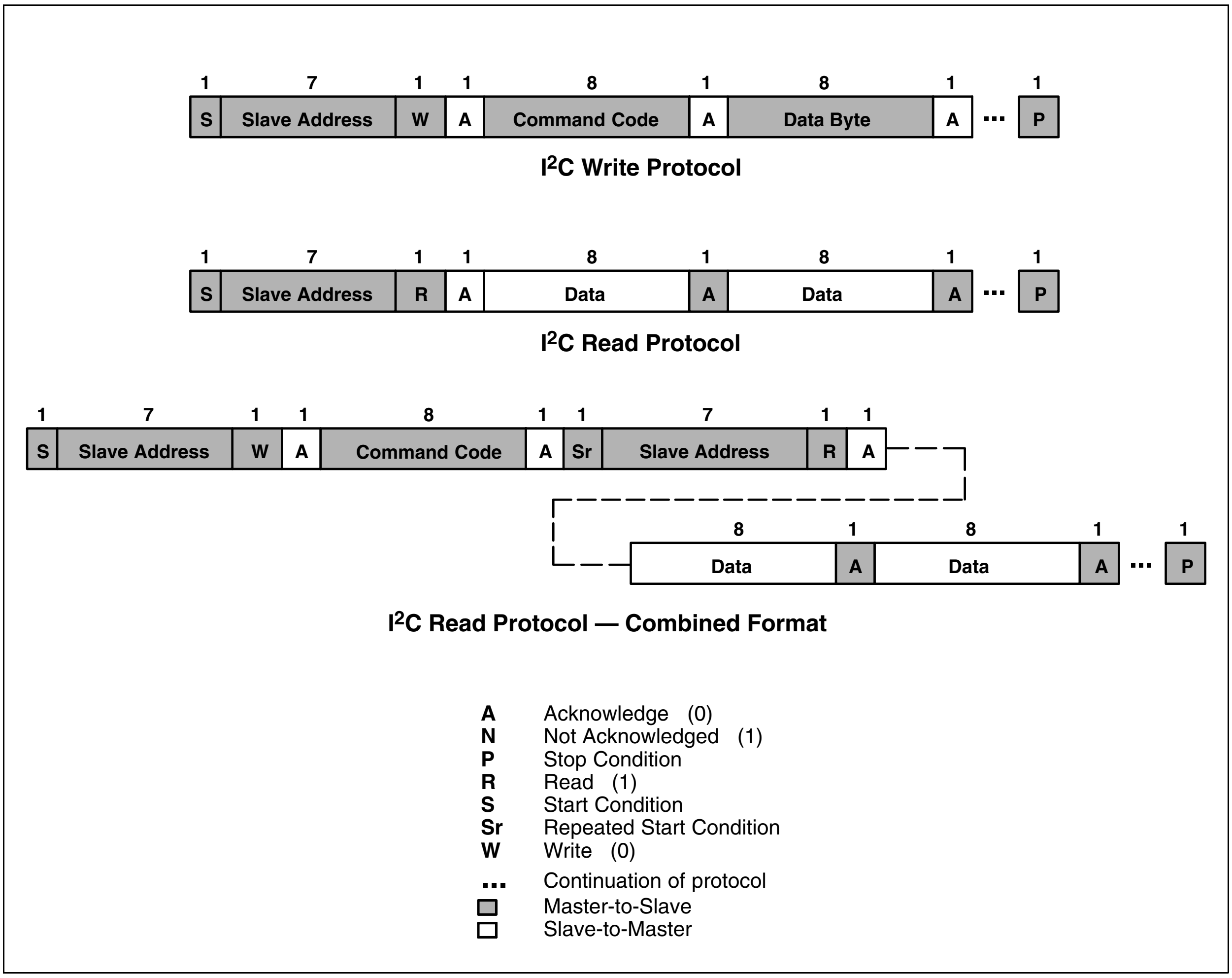
I²C Protocols

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 21). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c-bus.org/references/.

Figure 21:
I²C Protocols



Register Description

The TCS3471 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 22.

Figure 22:
Register Set

Address	Register Name	R/W	Register Function	Reset Value
−−	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	RGBC ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	RGBC interrupt low threshold low byte	0x00
0x05	AILTH	R/W	RGBC interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	RGBC interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	RGBC interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0F	CONTROL	R/W	Gain control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	CDATA	R	Clear ADC low data register	0x00
0x15	CDATAH	R	Clear ADC high data register	0x00
0x16	RDATA	R	Red ADC low data register	0x00
0x17	RDATAH	R	Red ADC high data register	0x00
0x18	GDATA	R	Green ADC low data register	0x00
0x19	GDATAH	R	Green ADC high data register	0x00
0x1A	BDATA	R	Blue ADC low data register	0x00
0x1B	BDATAH	R	Blue ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for the following read/write operations.

Command Register

The command registers specifies the address of the target register for future write and read operations.

Figure 23:
Command Register

7	6	5	4	3	2	1	0
COMMAND	TYPE		ADD				

<table>
<tr><th>Field</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>COMMAND</td><td>7</td><td colspan="2">Select Command Register. Must write as 1 when addressing COMMAND register.</td></tr>
<tr><td rowspan="7">TYPE</td><td rowspan="7">6:5</td><td colspan="2">Selects type of transaction to follow in subsequent data transfers:</td></tr>
<tr><td>FIELD VALUE</td><td>INTEGRATION TIME</td></tr>
<tr><td>00</td><td>Repeated byte protocol transaction</td></tr>
<tr><td>01</td><td>Auto-increment protocol transaction</td></tr>
<tr><td>10</td><td>Reserved — Do not use</td></tr>
<tr><td>11</td><td>Special function — See description below</td></tr>
<tr><td colspan="2">Byte protocol will repeatedly read the same register with each data access.
Block protocol will provide auto-increment function to read successive bytes.</td></tr>
<tr><td rowspan="6">ADD</td><td rowspan="6">4:0</td><td colspan="2">Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands:</td></tr>
<tr><td>FIELD VALUE</td><td>READ VALUE</td></tr>
<tr><td>00000</td><td>Normal — no action</td></tr>
<tr><td>00110</td><td>RGBC interrupt clear</td></tr>
<tr><td>other</td><td>Reserved — Do not write</td></tr>
<tr><td colspan="2">RGBC Interrupt Clear. Clears any pending RGBC interrupt. This special function is self clearing.</td></tr>
</table>

Enable Register (0x00)

The Enable register is used primarily to power the TCS3471 device on and off, and enable functions and interrupts as shown in Figure 24.

Figure 24:
Enable Register

7	6	5	4	3	2	1	0
Reserved			AIEN	WEN	Reserved	AEN	PON

Field	Bits	Description
Reserved	7:5	Reserved. Write as 0.
AIEN	4	RGBC interrupt enable. When asserted, permits RGBC interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
Reserved	2	Reserved. Write as 0.
AEN	1	RGBC enable. This bit actives the two-channel ADC. Writing a 1 activates the RGBC. Writing a 0 disables the RGBC.
PON(1)	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator. During reads and writes over the I^2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON.

Note(s):

1. A minimum interval of 2.4 ms must pass after PON is asserted before an RGBC can be initiated.

RGBC Timing Register (0x01)

The RGBC timing register controls the internal integration time of the RGBC clear and IR channel ADCs in 2.4 ms increments. Max RGBC Count = (256 - ATIME) × 1024 up to a maximum of 65535.

Figure 25:
RGBC Timing Register

Field	Bits	Description			
ATIME	7:0	**VALUE**	**INTEG_CYCLES**	**TIME**	**MAX COUNT**
		0xFF	1	2.4 ms	1024
		0xF6	10	24 ms	10240
		0xD5	42	101 ms	43008
		0xC0	64	154 ms	65535
		0x00	256	700 ms	65535

Wait Time Register (0x03)

Wait time is set 2.4 ms increments unless the WLONG bit is asserted, in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number.

Figure 26:
Wait Time Register

Field	Bits	Description			
WTIME	7:0	**REGISTER VALUE**	**WAIT TIME**	**TIME (WLONG = 0)**	**TIME (WLONG = 1)**
		0xFF	1	2.4 ms	0.029 s
		0xAB	85	204 ms	2.45 s
		0x00	256	614 ms	7.4 s

RGBC Interrupt Threshold Registers (0x04 - 0x07)

The RGBC interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by the clear channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Figure 27:
RGBC Interrupt Threshold Register

Register	Address	Bits	Description
AILTL	0x04	7:0	RGBC clear channel low threshold lower byte
AILTH	0x05	7:0	RGBC clear channel low threshold upper byte
AIHTL	0x06	7:0	RGBC clear channel high threshold lower byte
AIHTH	0x07	7:0	RGBC clear channel high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each integration cycle or if the integration has produced a result that is outside of the values specified by the threshold register for some specified amount of time.

Figure 28:
Persistence Register

7	6	5	4	3	2	1	0
Reserved				APERS			

Field	Bits	Description		
Reserved	7:4	Reserved.		
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
APERS	3:0	**FIELD VALUE**	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
APERS	3:0	0000	Every	Every RGBC cycle generates an interrupt
APERS	3:0	0001	1	1 clear channel value outside of threshold range
APERS	3:0	0010	2	2 clear channel consecutive values out of range
APERS	3:0	0011	3	3 clear channel consecutive values out of range
APERS	3:0	0100	5	5 clear channel consecutive values out of range
APERS	3:0	0101	10	10 clear channel consecutive values out of range
APERS	3:0	0110	15	15 clear channel consecutive values out of range
APERS	3:0	0111	20	20 clear channel consecutive values out of range
APERS	3:0	1000	25	25 clear channel consecutive values out of range
APERS	3:0	1001	30	30 clear channel consecutive values out of range
APERS	3:0	1010	35	35 clear channel consecutive values out of range
APERS	3:0	1011	40	40 clear channel consecutive values out of range
APERS	3:0	1100	45	45 clear channel consecutive values out of range
APERS	3:0	1101	50	50 clear channel consecutive values out of range
APERS	3:0	1110	55	55 clear channel consecutive values out of range
APERS	3:0	1111	60	60 clear channel consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Figure 29:
Configuration Register

7	6	5	4	3	2	1	0
Reserved						WLONG	Reserved

Field	Bits	Description
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Figure 30:
Control Register

7	6	5	4	3	2	1	0
Reserved						AGAIN	

Field	Bits	Description	
Reserved	7:2	Reserved. Write bits as 0	
AGAIN	1:0	RGBC Gain Control.	
		FIELD VALUE	**RGBC GAIN VALUE**
		00	1x gain
		01	4x gain
		10	16x gain
		11	60x gain

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Figure 31:
ID Register

7	6	5	4	3	2	1	0
ID							

Field	Bit	Description	
ID	7:0	Part number identification	0x14 = TCS34711 & TCS34715
			0x1D = TCS34713 & TCS34717

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 32:
Status Register

7	6	5	4	3	2	1	0
Reserved			AINT	Reserved			AVALID

Field	Bit	Description
Reserved	7:5	Reserved.
AINT	4	RGBC clear channel Interrupt.
Reserved	3:1	Reserved.
AVALID	0	RGBC Valid. Indicates that the RGBC channels have completed an integration cycle.

RGBC Channel Data Registers (0x14 - 0x1B)

Clear, red, green, and blue data is stored as 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with a read word protocol bit set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 33:
ADC Channel Data Registers

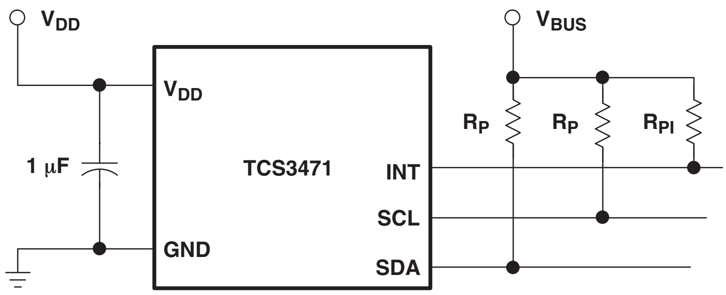
Register	Address	Bits	Description
CDATA	0x14	7:0	Clear data low byte
CDATAH	0x15	7:0	Clear data high byte
RDATA	0x16	7:0	Red data low byte
RDATAH	0x17	7:0	Red data high byte
GDATA	0x18	7:0	Green data low byte
GDATAH	0x19	7:0	Green data high byte
BDATA	0x1A	7:0	Blue data low byte
BDATAH	0x1B	7:0	Blue data high byte

Application Information: Hardware

Typical Hardware Application

A typical hardware application circuit is shown in Figure 34. A 1-µF low-ESR decoupling capacitor should be placed as close as possible to the V_{DD} pin.

Figure 34:
Typical Application Hardware Circuit



V_{BUS} in Figure 34 refers to the I^2C bus voltage, which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

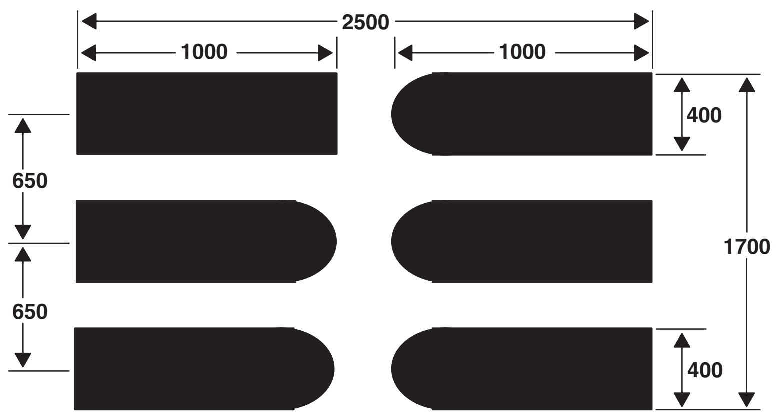
The I^2C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

PCB Pad Layouts

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 35.

Note(s): Pads can be extended further if hand soldering is needed.

Figure 35:
Suggested FN Package PCB Layout

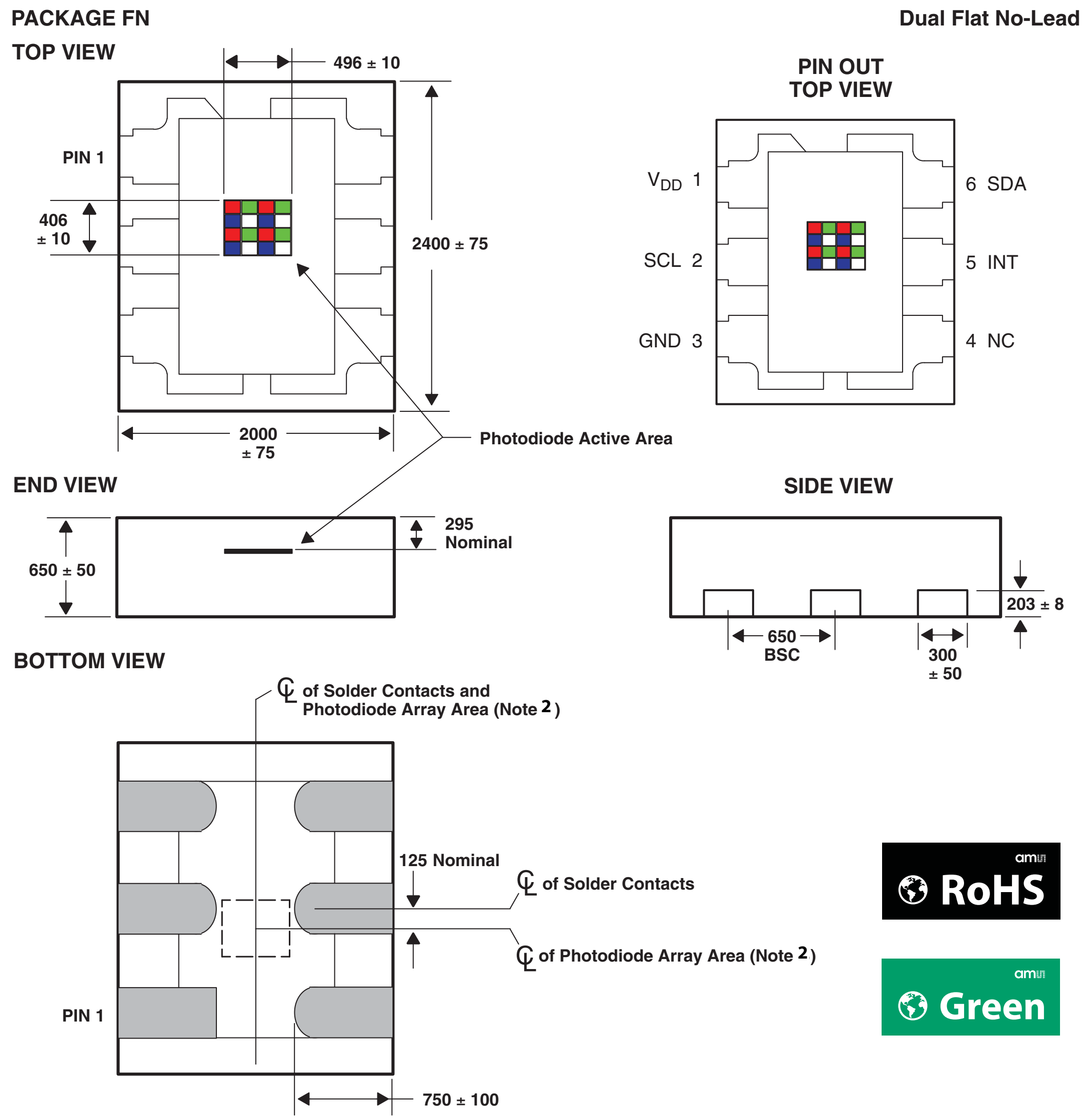


Note(s):

1. All linear dimensions are in micrometers.
2. This drawing is subject to change without notice.

Mechanical Data

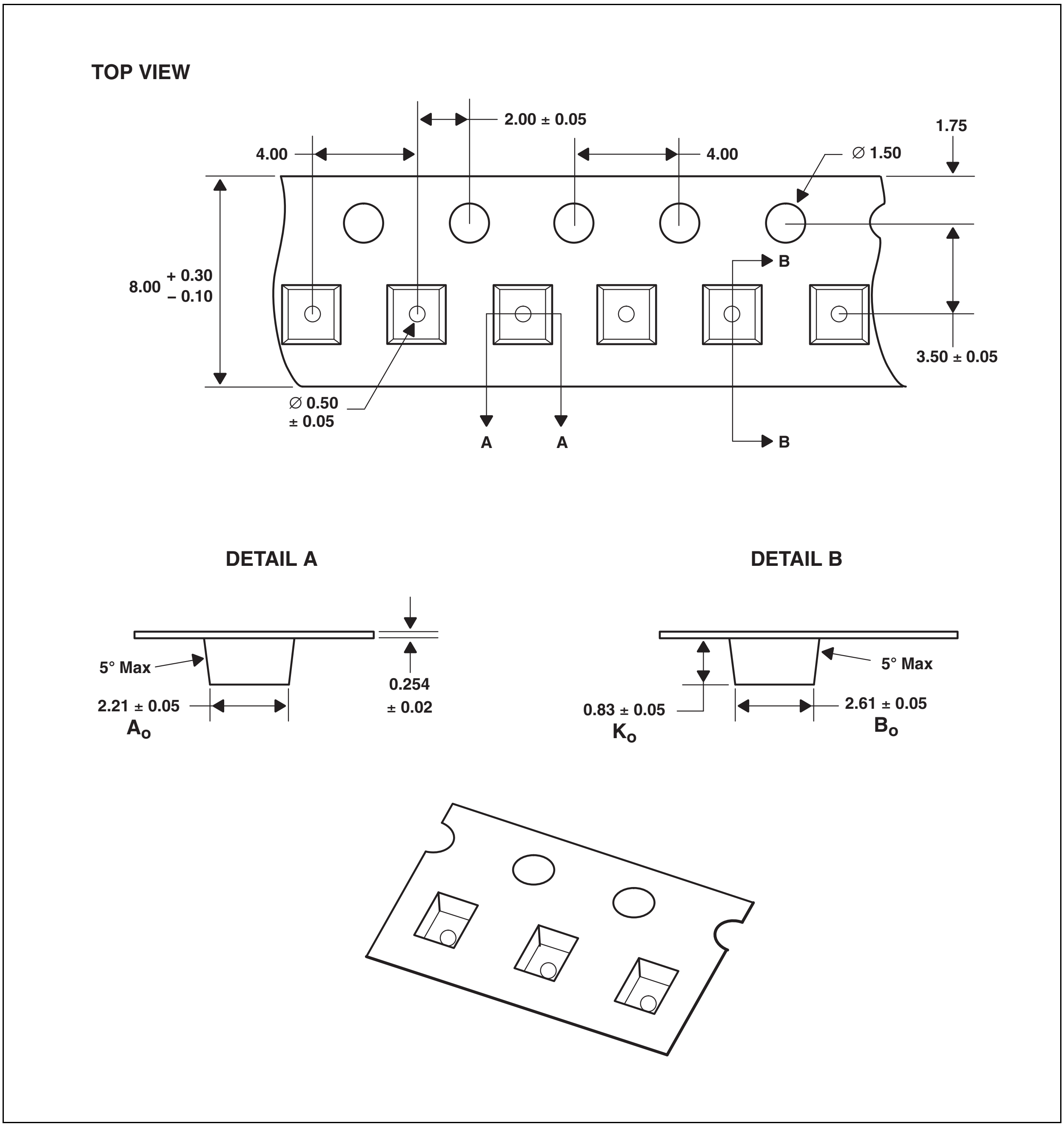
Figure 36:
Package FN — Dual Flat No-Lead Packaging Configuration



Note(s):

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of ± 75 µm.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Figure 37:
Package FN Carrier Tape



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Manufacturing Information

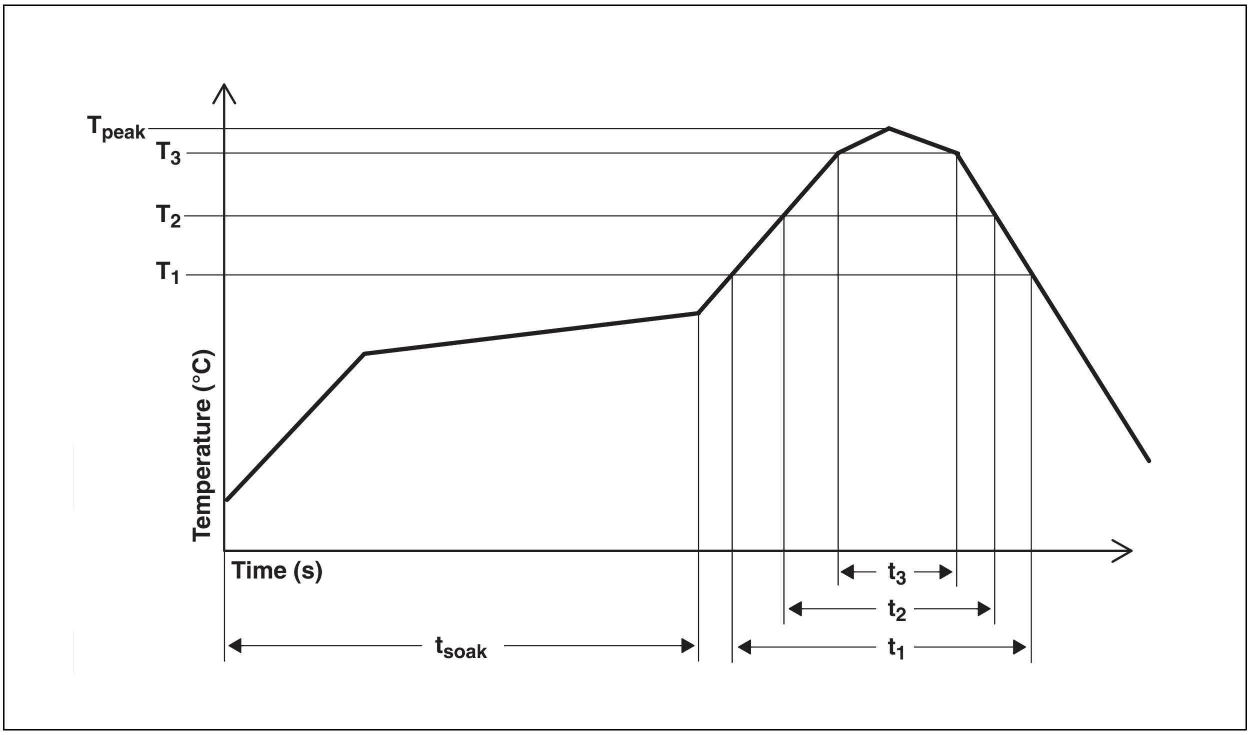
The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 38:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above T_{peak} −10°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max −5°C/s

Figure 39:
Solder Reflow Profile Graph



Note(s):

1. Not to scale — for reference only

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C
- Relative Humidity: 60% maximum
- Total Time: 12 months from the date code on the aluminized envelope — if unopened
- Opened Time: 168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 12 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 50°C for 12 hours.

Ordering & Contact Information

Figure 40:
Ordering Information

Ordering Code	Description	Device	Address	Package - Leads
TCS34711FN	I^2C Vbus = V_{DD} Interface	TCS34711	0x39	FN–6
TCS34713FN	I^2C Vbus = 1.8 V Interface	TCS34713	0x39	FN–6
TCS34715FN	I^2C Vbus = V_{DD} Interface	TCS34715	0x29	FN–6
TCS34717FN	I^2C Vbus = 1.8 V Interface	TCS34717	0x29	FN–6

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Revision Information

Changes from 1-00 (2016-May-23) to current revision 1-01 (2018-Mar-27)	Page
Updated Figure 40	33

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision
2. Correction of typographical errors is not explicitly mentioned.

Content Guide