

General description

The epc611 chip is a general-purpose, monolithic, fully integrated photoelectric CMOS device for optical distance measurements and object detection. Its working principle is based on 3D TOF measurement.

The system-on-chip (SOC) contains:

- A full data acquisition path including the modulation driver for LEDs or Laser Diodes, the photo-receiver with an 8x8 pixel TOF CCD array, the signal conditioning, the A/D converter and the basic signal processing.
- An on-chip controller managing data acquisition and data communication.
- An SPI interface for the command and data communication.
- A supply-voltage power management unit.

Various modes allow the chip to operate as a very fast one-pixel range-finder chip, as fast one-pixel range-finder chip with low distance noise, as 8 x 8 TOF imager chip, etc. By adding a micro-processor and few external components, a fully functional TOF range-finder or a TOF camera can be built. It measures the object distance per pixel individually and simultaneously.

The working principle is based on the elapsed time-of-flight (TOF) of a photon (modulated light) emitted by the illumination and reflected back by the object to the photosensitive receiver. The receiver measures the phase-shift between the emitted and received signal which is proportional to the distance.

The very high photo-sensitivity allows operating ranges of several meters and an accuracy down to a centimeter depending on the lens and the illumination power.

Features

- Operating range up to 30 m
- Resolution in the millimeter range
- On-chip high power LED or Laser Diode driver
- Easy-to-use operation in combination with a microprocessor
- Fast frame rates:
 - 4-pixel-sum range-finder UFS mode: up to 8'000 fps
 - 64-pixel-sum range-finder ULN mode: 4'000 fps
 - 64-pixel imager TIM mode: up to 3'000 fps
- Output data: 12..18 bit resolution, depending on operating mode
- HDR (High-Dynamic-Range) range-finder mode
- Excellent ambient-light suppression up to 100 kLux.
- Internal or external modulation control
- Low power consumption
- Fast SPI interface for command and data transfer
- Fully SMD compatible flip-chip CSP24 package with very small footprint

Applications

- Altimeter for drones
- Scanner for SLAM data acquisition in mobile robots
- People and object counting
- Door opening, machine controlling and safeguarding
- Volumetric mapping of objects
- Automatic vehicle guidance
- Low cost seating position detection in cars
- Gesture control (man-machine-interface)

Functional block diagram

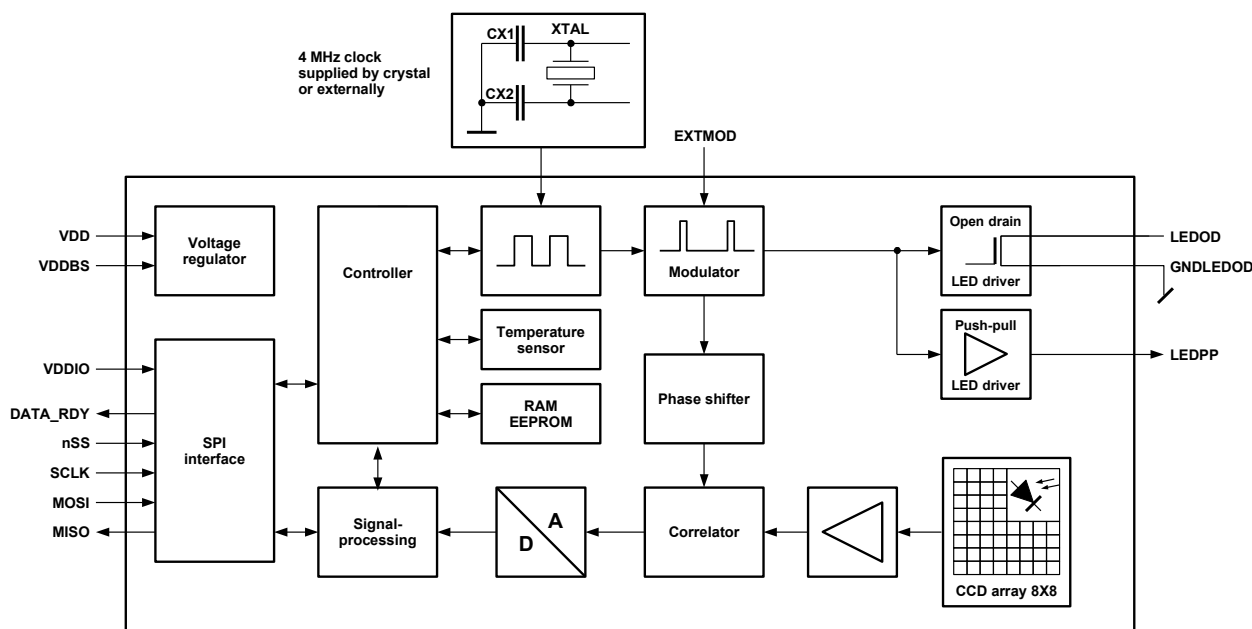


Figure 1: epc611 block diagram

Table of Contents

1. Electrical, optical and timing characteristics	4
1.1. Operating conditions and electrical characteristics	4
1.2. Absolute maximum ratings	4
1.3. Timing parameters	5
1.4. Optical characteristics	5
1.5. Sensitivity	6
1.6. Ambient-light suppression (ABS)	6
1.7. Other optical parameters	7
1.8. Temperature sensor characteristics	7
1.9. Distance measurement temperature drift	7
2. Pin-out	8
2.1. Pin mapping	8
2.2. Pin list	8
2.3. Power domain separation and ESD protection	9
3. Packaging and layout information	10
3.1. Mechanical dimensions	10
3.2. Parasitic light sensitivity (PLS)	11
3.3. Pin 1 marking	11
3.4. PCB design and SMD manufacturing process considerations	12
3.5. Design precautions	12
4. Packaging information	13
5. Ordering information	13
5.1. Notes for various chip releases	13
6. Hardware implementation	14
6.1. Block diagram	14
6.2. Typical application diagram	15
6.3. Application diagram part list	15
6.4. Hardware implementation notes	15
6.5. Clock sources	16
6.5.1. System clock supply	16
6.5.2. External modulation EXTMOD	16
6.6. Illumination (LED) driver	17
6.6.1. LEDOD pin	17
6.6.2. LEDPP pin	18
6.7. DLL (Delay line)	18
6.8. Pixel-field	19
6.8.1. Pixel architecture	19
6.8.2. Pixel-field organization and readout	19
6.8.3. Pixel saturation detection	20
6.8.4. ADC conversion over- and underflow	20
7. Imaging	20
7.1. epc611 functional overview	20
7.2. Time-of-flight modes (TOF)	21
7.2.1. TIM mode: 8x8 pixel 3D ToF IMager	22
7.2.2. ULN mode: Ultra Low Noise range-finder (sum of 8x8 pixels)	25
7.2.3. UFS mode: Ultra Fast and Sensitive range-finder (sum of 2x2 binned pixels)	28
7.2.4. UHD mode: Ultra High Dynamic range-finder, low noise (8 different int. times, each sum of 8 pixels)	31
7.2.5. LNH mode: Low Noise High dynamic range-finder, sensitive (4 int. times, each sum of 4 binned pixels)	34
7.2.6. RBH mode: Reduced motion-Blur HDR range-finder, sens., low noise (2 DCS, 2 int. times, each sum of 4 bin. pixels)	37
7.2.7. NBF mode: No motion-Blur Fast range-finder, low noise (4 DCS, each sum twice of 8 pixels)	40
7.3. Grayscale imager modes	43
7.3.1. GIM mode: 8x8 pixel Grayscale IMager	43
7.3.2. GBI mode: 4x4 pixel Grayscale Binned pixel Imager	46
7.3.3. Alternative grayscale modes	49
7.4. Imaging timing and frame rates	49
7.4.1. Single measurement control	50
7.4.2. Continuous measurement control (auto-run)	50
7.5. Integration time setting	50
7.5.1. Single integration time per frame	50
7.5.2. Multiple integration times per frame	51
7.6. Distance measurement (3D TOF)	52
7.7. Distance calculation algorithm	52
7.8. Unambiguity range versus time base setting	53
7.9. Quality of the measurement	53

7.10. Grayscale imaging / ambient-light measurement	55
7.11. Calibration and compensation of TOF cameras	56
7.12. Noise reduction and signal filtering	56
8. Temperature sensor	57
8.1. Initialization	57
8.2. Read-out during runtime	57
8.3. Calculating temperature in °C	58
9. Application information	59
9.1. Example sequence from start-up to frame acquisition	59
9.2. 3D TOF distance measurement flow	59
9.3. Rolling DCS frames	60
9.4. Enhanced rolling DCS frame mode	61
10. Parameter and configuration memory	62
10.1. Sequencer program	62
10.2. Data memory map	62
10.2.1. Control page	62
10.2.2. RAM page	63
10.2.3. EEPROM page	63
11. SPI interface	63
11.1. SPI timing	63
11.2. SPI frame format	64
11.3. SPI commands	65
11.4. SPI response	65
11.5. SPI pixel data readout and DATA_RDY	66
12. Register map	67
12.1. SPI Page 0	67
12.2. SPI Page 1	67
12.3. SPI Page 2	68
12.4. SPI Page 3	69
12.5. SPI Page 4	69
12.6. SPI Page 5	71
12.7. SPI Page 6	71
12.8. SPI Page 7	72
13. Control command examples	72
13.1. Reading part version	72
13.2. Reading IC version	72
13.3. Reading WAFER ID and CHIP ID	73
13.4. Writing to EEPROM	73
13.5. Reading from EEPROM	73
13.6. Latest version of the sequencer program	74
14. Addendum	75
14.1. Terms, definitions and abbreviations	75
14.2. Related documents	75
15. IMPORTANT NOTICE	76

1. Electrical, optical and timing characteristics

All characteristics are at typical operational ratings, $T_A = +25^\circ\text{C}$, modulation frequency 10MHz, unless otherwise stated.

1.1. Operating conditions and electrical characteristics

Parameter	Description	Conditions/Comments	V_{SC}	Min.	Typ.	Max.	Units
V_{DD}	Main supply voltage	Ripple ¹ < ± 100 mV	V_{DD}	8.0	8.5	9.0	V
V_{DDIO}	IO supply voltage	Ripple ¹ < ± 50 mV	V_{DDIO}	2.43	3.3	5.5	V
V_{DDBS}	Bias supply voltage	Ripple ¹ < ± 50 mV	V_{DDBS}	-10.5	-10	-9.5	V
$I_{VDD-Average}$	Average main supply current	@ nominal voltage			18		mA
$I_{VDDIO-Average}$	Average IO supply current	@ 3.3 V			100		μA
I_{VDDBS}	Bias supply current ²				0.1	2.0	mA
V_{ON_LEDOD}	LEDOD on-voltage forward voltage (refer to section 6.6.1.)	@ $I_{LEDOD-ON} = 100$ mA @ $I_{LEDOD-ON} = 400$ mA			0.1 0.9		V V
I_{OFF_LEDOD}	LEDOD leakage current	@ LEDOD off-voltage				10	μA
V_{IH_VDDIO}	Digital high level input voltage	Excluding XTALIN	V_{DDIO}	$0.7 \times V_{DDIO}$			V
V_{IL_VDDIO}	Digital low level input voltage	Excluding XTALIN				$0.3 \times V_{DDIO}$	V
V_{IH_XTALIN}	Digital high level input voltage	XTALIN	+1.8V	1.35			V
V_{IL_XTALIN}	Digital low level input voltage	XTALIN				0.2	V
I_{IH_VDDIO}	Digital high level input current	V_{IH} max.				10.0	μA
I_{IL_VDDIO}	Digital low level input current	V_{IL} min.		-10			μA
C_{in_VDDIO}	Digital input capacitance					3	pF
V_{OH_VDDIO}	Digital high level output voltage		V_{DDIO}	$0.8 \times V_{DDIO}$			V
V_{OL_VDDIO}	Digital low level output voltage					$0.2 \times V_{DDIO}$	V
I_{OH_VDDIO}	Digital high level output current	Push-pull pin LEDPP only				50	mA
I_{OL_VDDIO}	Digital low level output current			-50			mA
C_{out_VDDIO}	Digital output load capacitance					20	pF
$P_{Average}$	Power dissipation (average)				155		mW
R_{Th}	Thermal resistance	on PCB with underfill			65		$^\circ\text{K/W}$
T_{OP}	Operating temperature			-40		105	$^\circ\text{C}$

Table 1: Operating conditions

Notes:

¹ Min. and Max. voltage values include noise and ripple voltages.

² Value 0.1 mA is for a camera with lens and a bright illuminated white target. Goes up for strong illumination (approx. $550 \mu\text{W}/\text{mm}^2$, no lens) up to typ. 2 mA.

1.2. Absolute maximum ratings

Parameter	Conditions
Main supply voltage V_{DD}	-0.5 ... +9.5 V
IO supply voltage V_{DDIO}	-0.5 ... +5.5 V
Bias supply voltage V_{DDBS}	-12.0 ... +0.5 V
Voltage to any pin in the same V_{SC} supply class. Refer to Figure 4 and Table 9.	$V_{SC} \text{ min} - 0.3 \text{ V} \dots V_{SC} \text{ max} + 0.3 \text{ V}$
LED sink current I_{ON_LED} (modulated peak current, refer to Figure 16 and section 6.6.1.) ¹	400 mA @ T_j 85 $^\circ\text{C}$ 25 mA @ T_j 125 $^\circ\text{C}$ linear reduction between 85 and 125 $^\circ\text{C}$
LED off-voltage V_{OFF_LED} (open-drain output)	7.5 V
ESD rating	JEDEC HBM class 1C (1kV to < 2kV)
Junction temperature (T_j)	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Relative humidity	0 ... 95%, non-condensing

Table 2: Absolute maximum rating

Notes:

¹ The overall ON/OFF time of the LED during the measurement cycle shall not exceed a 28% duty-cycle. Refer to t_{INT} and t_{FRAME} of

Figure 47 and Figure 48. The duty-cycle of the modulation signal itself is always 1:1 resp. 50%.

1.3. Timing parameters

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
t _{STARTUP}	Start-up time or RESET	After applying external supplies		340	1'000	µs
t _{RESET}	RESET			340		µs
t _{EEPROM_Write}	Write EEPROM	Waiting time per byte			25	ms
t _{DLL}	DLL delay for 1 step	Approx. 30 cm distance shift per step. Refer for details to register P3[0x13] and Figure 19, for exact value to register P6[0x1A].		2.1	30	ns
f _{XTAL}	Clock frequency	Refers to crystal (or ceramic resonator)	---	4	---	MHz
df _{XTAL}	Clock frequency deviation	Any deviation is added as a linear distance error			±100	ppm
f _{JITTER}	Clock frequency phase jitter	Peak-to-peak, cycle to cycle			50	ps
f _{LED}	LED modulation frequency		0.625		20	MHz
f _{EXTMOD}	Ext. modulation clock	Refer to Chapter 6.5.2			80	MHz
t _{LED_rise/fall}	Required rise/fall time of the illumination LED/LD	@ 50 ohm load Note: Use VCSELs or high-speed LEDs with short switching times e.g. Osram SFH4059, etc.			12	ns
f _{SCLK}	SPI clock frequency				16	MHz
t _H / t _L	SCLK HIGH / LOW period		15			ns

Table 3: Timing parameters

1.4. Optical characteristics

Typ. operational ratings, T_A = +25°C, unless otherwise stated.

Parameter	Description	Conditions/Comments	Min.	Typ.	Max.	Units
A _{PIXEL}	Pixel photosensitive area	100% fill factor		20 x 20		µm
A _{SENSOR}	Pixel-field area	8x8 pixel		0.16 x 0.16		mm

Table 4: Optical characteristics

1.5. Sensitivity

@ integration time 100 μ s

Parameter	Description	Min.	Typ.	Max.	Units	
TOF sensitivity S_{TOF}	<ul style="list-style-type: none"> Modulation frequency 12MHz Amplitude 1,400 LSB 	640nm	0.75	0.9	1.05	$\frac{nW/mm^2}{LSB}$
		850nm	0.50	0.6	0.70	
		940nm	0.65	0.8	0.95	
TOF _{SENS} FPN	Sensitivity fix pattern noise, @ 1,400 LSB		40	100	LSB	
TOF _{DIST} FPN	Distance fix pattern noise, @ 1,400 LSB		18	50	mm	
I_{Dark}	Dark current (drift during readout)		5	20	LSB/ms	
Grayscale sensitivity	Normal operation	0.117	0.156	0.187	$\frac{nW/mm^2}{LSB}$	
	Temperature sensing mode	0.48	0.62	0.76		
H_v	Optical sensitivity		150k		$\frac{LSB}{Lux/sec}$	
GS _{STD}	Grayscale standard deviation		25	100	LSB	

Table 5: Sensitivity

1.6. Ambient-light suppression (ABS)

An important function of the 3D TOF pixel is the ambient-light suppression. It removes DC or low frequency modulated light caused by sunlight, room illumination, etc. from the modulated light generated by the camera illumination. The amount of collected ambient light is proportional to the integration time. The longer the integration time, the more unwanted light will be collected. It's a good practice to keep the integration time for TOF imaging below 1ms. In addition, optical bandpass filters to block the unwanted light spectrum is mandatory.

Parameter	Ambient light suppression	Integration time	Wavelength	Min.	Typ.	Max.	Units
E_e	Irradiance, DC light	100 μ s	640nm	0.30			mW/mm^2
			850nm	0.20			
			940nm	0.25			

Parameter	Ambient light suppression	Integration time	Center wavelength	Bandwidth	Min.	Typ.	Max.	Units
E_v	Luminance equivalent, sunlight	500 μ s	640nm	$\pm 27.5nm$	85			kLux
			850nm	$\pm 32.5nm$	70			
			940nm	$\pm 30nm$	190			

Table 6: Ambient light suppression

Note:

The default and suggested chip configuration is set to achieve highest possible frame rate and using additional ambient-light correction according the Application note AN10 Calibration and compensation: Register P4[0x10], bit 3 = 0 and P5[0x0B] = 0x00. A 20% more efficient ambient-light suppression is possible, if the the following registers are modified:

P4[0x10], bit 3 = 1

P5[0x0B] = 0x01

It turns the LED modulation before each integration for additional 40 μ s @ 20MHz modulation frequency on. This modulation is independent of the effective integration time. The on-time depends on the modulation frequency by $t_{ON} = 40\mu s * 20MHz / \text{modulation frequency}$.

1.7. Other optical parameters

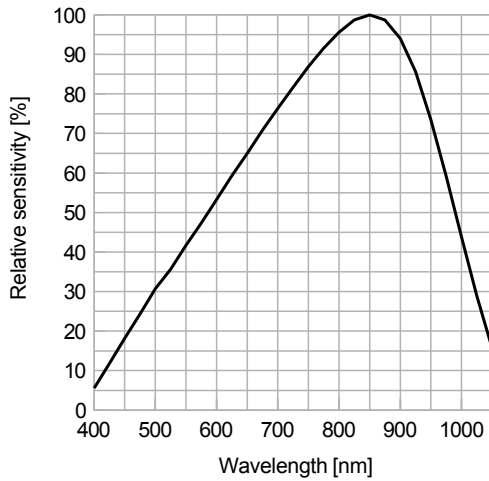


Figure 2: Relative spectral sensitivity (S_{λ}) vs. wavelength

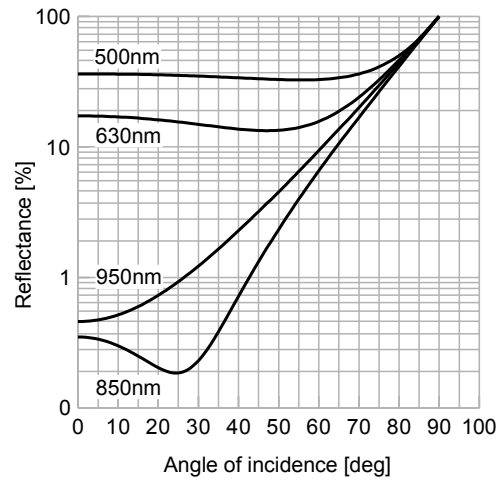


Figure 3: Reflectance vs. illumination angle (AOI)

1.8. Temperature sensor characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
T_{TEMP}	Measurement range		-40		+105	°C
P_{TEMP}	Sensor resolution			14		bit
k	Temperature sensor gain			0.134		K/LSB
Lin	Linearity	Over temperature range		5		%
T_{CAL}	Calibration temperature		26.5	27.0	27.5	°C

Table 7: Temperature sensor characteristics

Note: Refer also to chapter 8.

1.9. Distance measurement temperature drift

@10MHz modulation frequency

Parameter	Description	Min.	Typ.	Max.	Units
TC_{PIX}	Pixel		11.3		mm/K
TC_{OD}	LED/LD driver		2.7		mm/K
TC_{DLLn}	DLL stage, per stage		0.65		mm/K

Table 8: Optical characteristics

Note: Values vary from imager to imager. Refer for details to Figure 20 and application note AN10 Calibration and Compensation, chapter temperature compensation.

2. Pin-out

2.1. Pin mapping

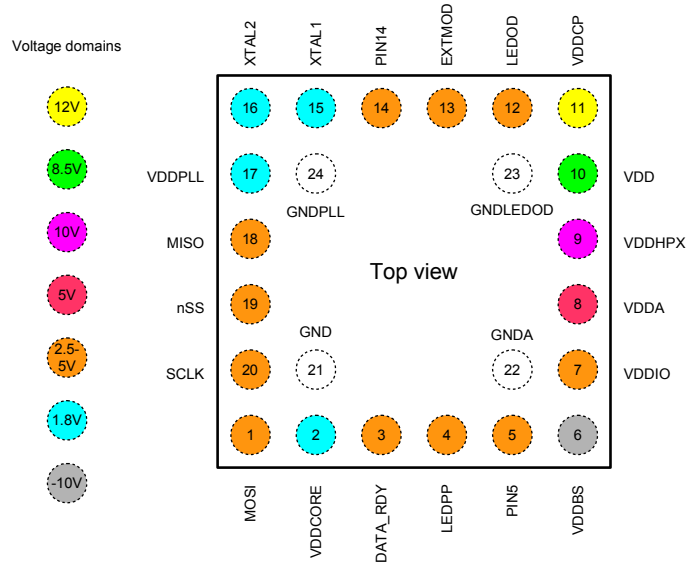


Figure 4: Pin mapping (top view, solder balls are bottom-side, pixel-field is top-side)

2.2. Pin list

Pin No.	Pin name	Supply class V_{sc}	Pin type	Rst level	Description
I/O pins					
19	nSS	V_{DDIO}	DI	V_{OH}	SPI slave selection
20	SCLK	V_{DDIO}	DI	V_{OL}	SPI slave clock
1	MOSI	V_{DDIO}	DI	V_{OL}	SPI slave data input
18	MISO	V_{DDIO}	DO	V_{OL}	SPI slave data output
3	DATA_RDY	V_{DDIO}	DIO	V_{OL}	Data ready notifier, no pull-up or pull-down resistor on this pin
4	LEDPP ¹	V_{DDIO}	DIO	V_{OL}	LED push/pull output
13	EXTMOD	V_{DDIO}	DIO	V_{OL}	Modulator/demodulator external clock input
Analog pins					
15	XTAL1	V_{DDPLL}	AI		Oscillator clock input for crystal, resonator or digital clock
16	XTAL2	V_{DDPLL}	AO		Oscillator output to crystal or resonator
12	LEDOD ¹	$V_{DDLEDOD}$	AOD		LED open-drain output
14	PIN14	V_{DDIO}	AI		Connect this pin to GND
5	PIN5	V_{DDA}	AOI		Test pad (suggested), no connection
Supply pins					
10	VDD	V_{DD}	PWR		Main supply voltage +8.5V
6	VDDBS	V_{DDBS}	PWR		Bias supply voltage -10V
7	VDDIO	V_{DDIO}	PWR		Digital IO supply voltage
11	VDDCP	V_{DDCP}	PWR		Internally generated analog supply voltage +12V
9	VDDHPX	V_{DDHPX}	PWR		Internally generated analog supply voltage +10V
8	VDDA	V_{DDA}	PWR		Internally generated analog supply voltage +5V
2	VDDCORE	V_{DDC}	PWR		Internally generated digital supply voltage +1.8V
17	VDDPLL	V_{DDPLL}	PWR		Internally generated digital supply voltage +1.8V
22	GND A	V_{SSA}	GND		Analog ground
23	GND LEDOD	$V_{SSLEDOD}$	GND		LED driver ground
21	GND	V_{SSIO}	GND		Digital ground
24	GND PLL	V_{VDDPLL}	GND		PLL ground

Table 9: Pin list

Notes:

¹ LEDPP and LEDOD should not be used at the same time to drive LEDs on the PCB because they exhibit different phase delays.

"Pin type" in Table 9 defines the following:

- DI: Digital input
- DO: Digital output
- DIO: Digital input/output (bidirectional)
- AI: Analog input
- AO: Analog output
- AOD: Analog output, open-drain
- PWR: Supply

"Rst. Level" in Table 9 defines the level of the IO pins during/after reset.

2.3. Power domain separation and ESD protection

The epc611 chip has 9 different power domains and 4 ground references internally, which are interconnected with ESD protection diodes. All pins are also equipped with ESD protection diodes. The diodes have a breakthrough voltage of 0.3V. The designer has to take care that none of these diodes become conductive either at power-up, power-down or during normal operation.

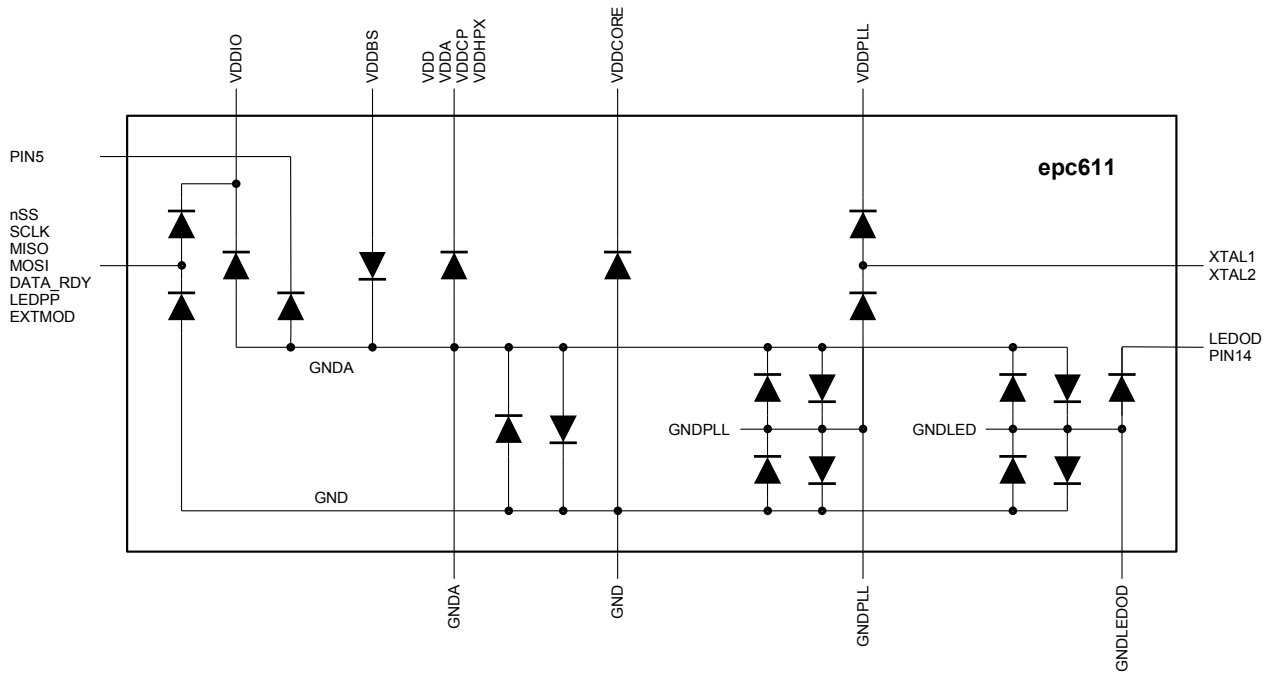


Figure 5: I/O pins and ESD protection diagram

3. Packaging and layout information

3.1. Mechanical dimensions

The packaging technology is chip scale packaging (CSP).

The center of the effective pixel-field (8x8) is positioned relative to the center of CSP pin 1. This point corresponds to the intersection of the middle of columns and the middle of rows when mapped to the pixel-field coordinate system on the die (see Figure 6 and Figure 7).

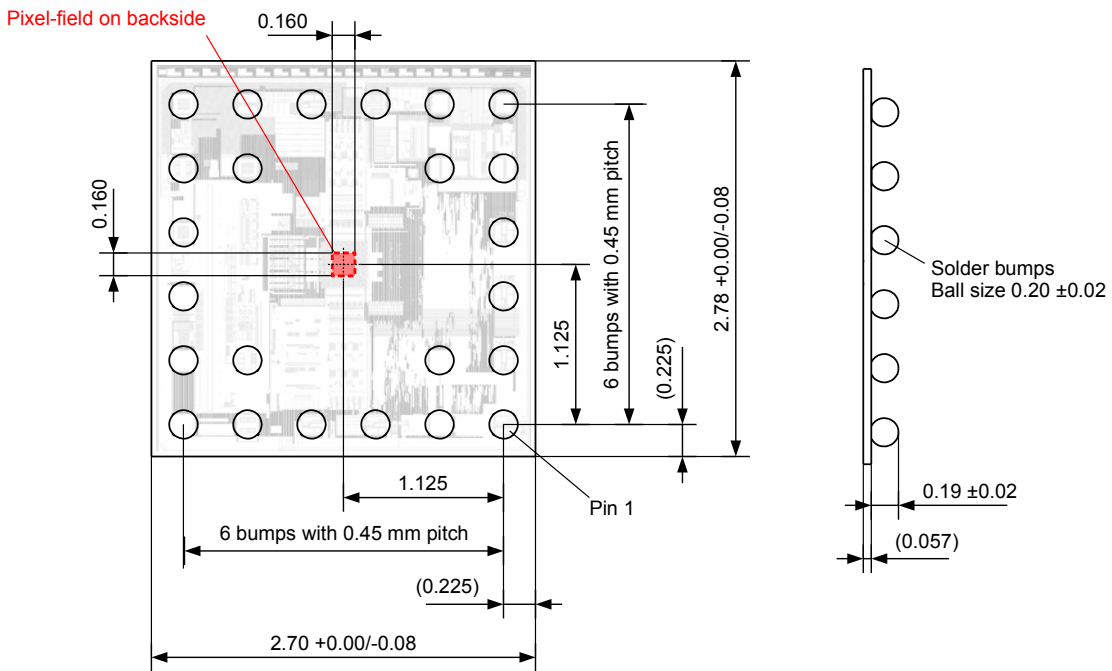



Figure 6: Mechanical dimensions

Notes:

-  Top side is illumination side
- All dimensions in mm
- Not specified tolerances: ± 0.001 mm
- Dimensions in brackets: Informal only

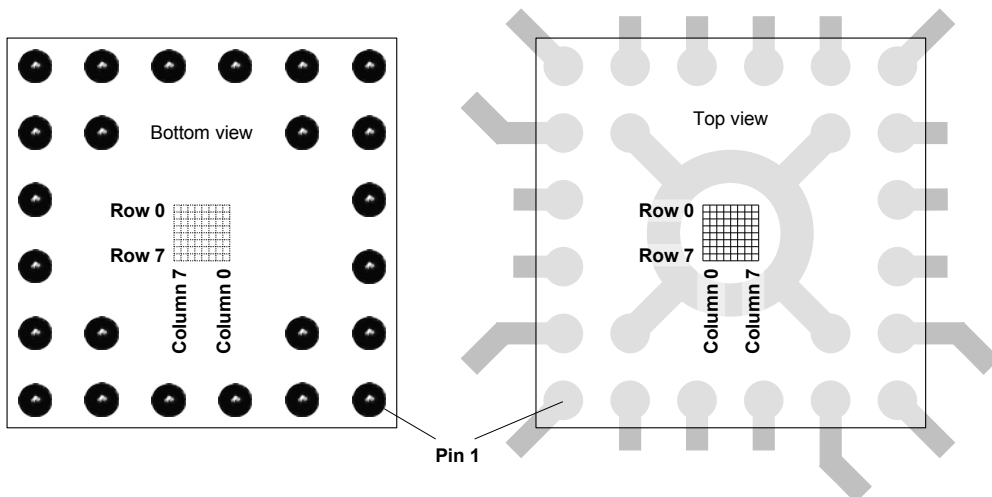


Figure 7: Orientation of the pixel-field (pixel order)
Note: Readout is different. Refer to Figure 21.

3.2. Parasitic light sensitivity (PLS)

CMOS circuits are sensitive to light. That is why they can be used for photo-sensing, imaging, etc. However, if strong light is radiating the chip beside the pixel field, analog and digital circuits can be affected in its function by such parasitic light. It is called parasitic light sensitivity (PLS). A known effect is a shift of the measured distance under strong ambient light.

Imager lenses have always a larger field of view than the pixel-field area (refer to Figure 22). In order to prevent the chip being illuminated by strong ambient light, an opaque aperture should be placed onto the photo-sensitive side of the imager as shown in Figure 8. The cover shall have an opening of 450 μm. With regard to the 160 x 160 μm pixel-field size, this shield can be assembled with a tolerance of ±120 μm in x and y axis. Such a cover can be made by a thin sheet metal stencil like an SMD solder paste printing stencil or by silk screen printing of black color.

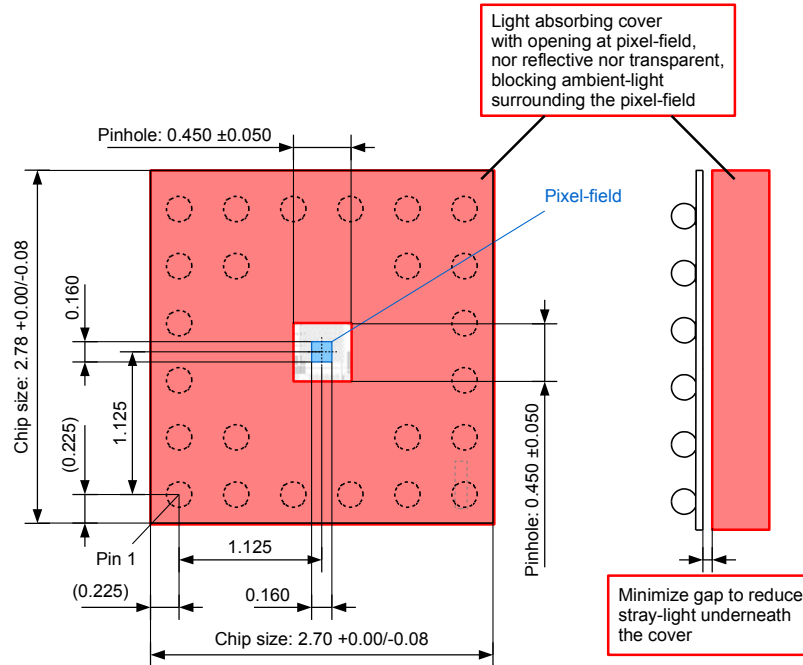



Figure 8: Opaque cover for protection against unwanted ambient-light

Notes:

- 
- All dimensions in mm
- Not specified tolerances: ±0.001 mm
- Dimensions in brackets: Informal only
- Top side is photosensitive side

3.3. Pin 1 marking

The following images show the epc611 chip from the bottom side with a view of the solder balls. Please note the location of pin 1. Please note the location of pin 1. It's highly recommended to check the pin 1 orientation with a vision system during the SMT assembly process.

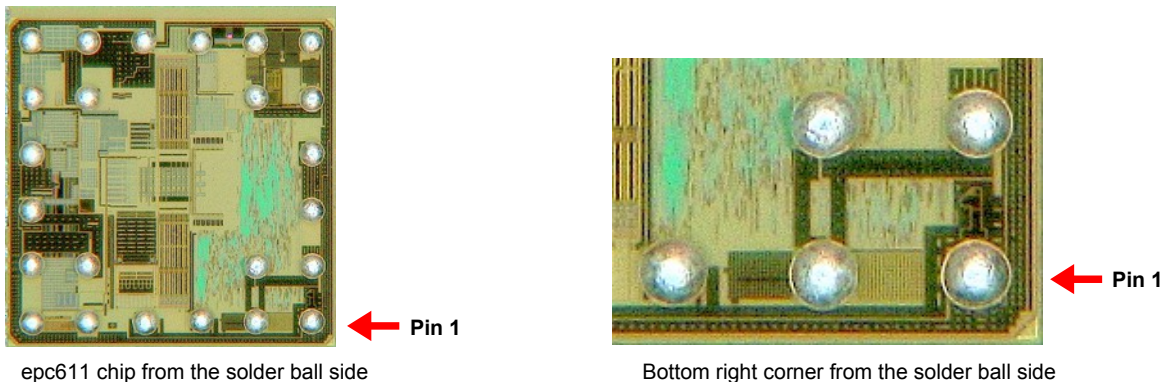


Figure 9: Pin 1 marking

Location of the pixel-field area

The pixel-field area is neither marked on the front nor on the backside of the IC. As a visible reference, a metal ring of the IC can be used. It is visible from the solder ball side. From the front side (photosensitive side) it can also be seen with a camera, which is sensitive in the near infrared wavelength domain (950 ... 1'150 nm).

3.4. PCB design and SMD manufacturing process considerations

As the epc611 chip comes in a very small 24 pin chip scale package with only 50 µm thickness, special care must be taken when making the PCB layout. In addition, careful handling during the assembly process must be ensured in order to avoid mechanical damage during the assembly process. Because the silicon chip is small and lightweight compared to the solder balls, it is highly recommended that all tracks to the chip come straight from the side. A symmetrical design is highly recommended to achieve high production yields. The pads and the tracks should also have exactly the same width, at least 1mm from the pad. They should be covered by a solder-resistant mask in order to avoid drain of the solder tin alloy onto the track.

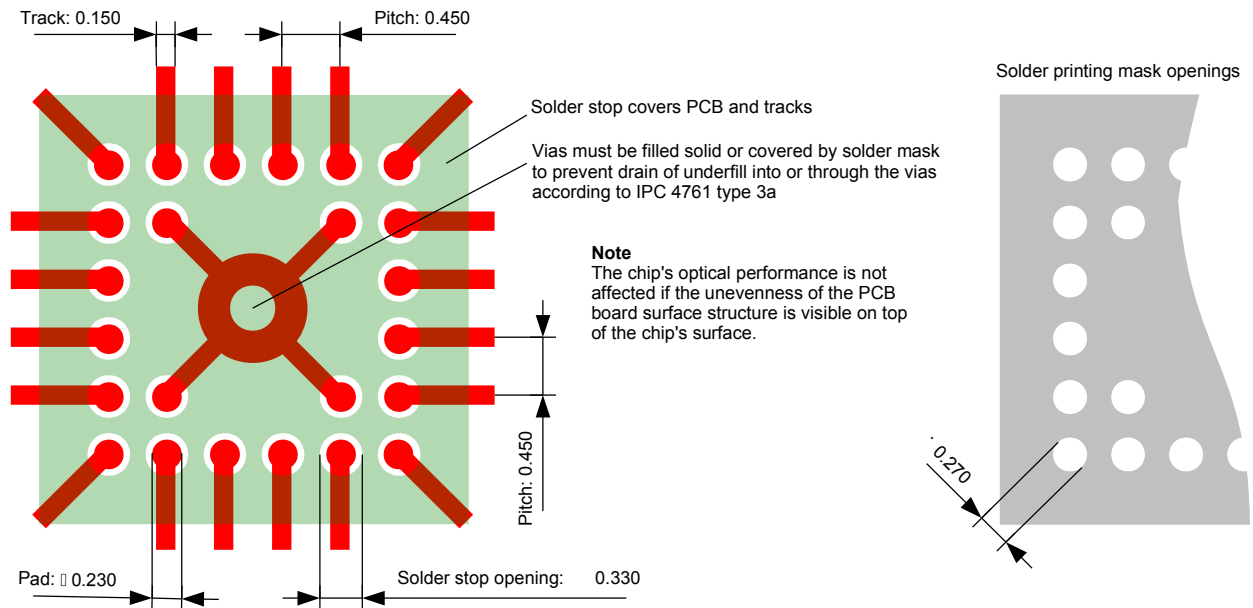


Figure 10: Layout recommendations (dimensions in mm)

Underfill of the components reduces stress on the solder pads caused by temperature cycling, mechanical bending, etc. Furthermore, thermal and mechanical fatigue is reduced and longterm reliability increased. Underfill material and underfill selection is application specific. It should follow JEDEC-STD JEP150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components. Please also, refer to the AN08 CSP Assembly Process-Rules Application Note, which can be downloaded from the ESPROS Website at www.espros.com, section Downloads. Following these recommendations will help to achieve high manufacturing yield.

3.5. Design precautions

The sensitivity of the sensor area is very high in order to achieve a long operating range. As a result, the epc611 device is very sensitive to EMI. Special care should be taken to keep the chip away from the signal tracks and other sources which may induce unwanted signals. To keep the noise floor low in the sensitive receiver path of the chip, a low ohmic and low inductive connection to the supply ground is needed. Figure 10 suggests a recommended grounding of the chip (if a ground plane is not feasible): Feed all grounds into a central via-hole with a drill diameter e.g. 0.5 ... 0.6 mm

4. Packaging information

Tape and reel information

The devices are packaged into embossed tapes for automatic placement systems. The tape is wound on 178 mm (7 inch) or 330 mm (13 inch) reels and individually packaged for shipment. General tape-and-reel specification data are available in a separate datasheet and indicate the tape size for various package types. Further tape-and-reel specifications can be found in the Electronic Industries Association EIA-Standard 481-1, 481-2, 481-3.

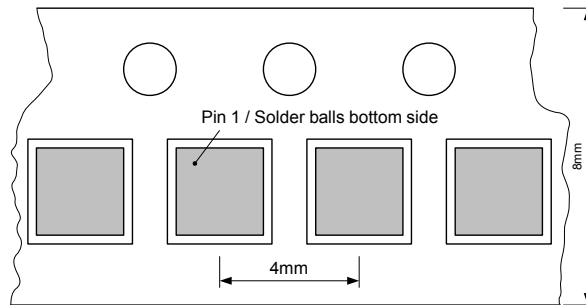


Figure 11: Tape dimensions (in mm)

ESPROS does not guarantee that there are no empty cavities in the tape. The pick-and-place machine should check for the presence of a chip during picking.

5. Ordering information

Part number	Part name	Package	RoHS compliance
P100 378	epc611-CSP24	CSP24	Yes

Table 10: Ordering information

5.1. Notes for various chip releases

The supplied chip version can be identified by

- reading the extension -XXX of the part name on the packaging labels or delivery papers: epc611-CSP24-XXX.
- reading the part version register P7[0x0B]. Refer to Chapter 12.8.

More detailed information for the chip releases, as well as the latest download code for each chip version, can be found in Chapter 13.6.

6. Hardware implementation

6.1. Block diagram

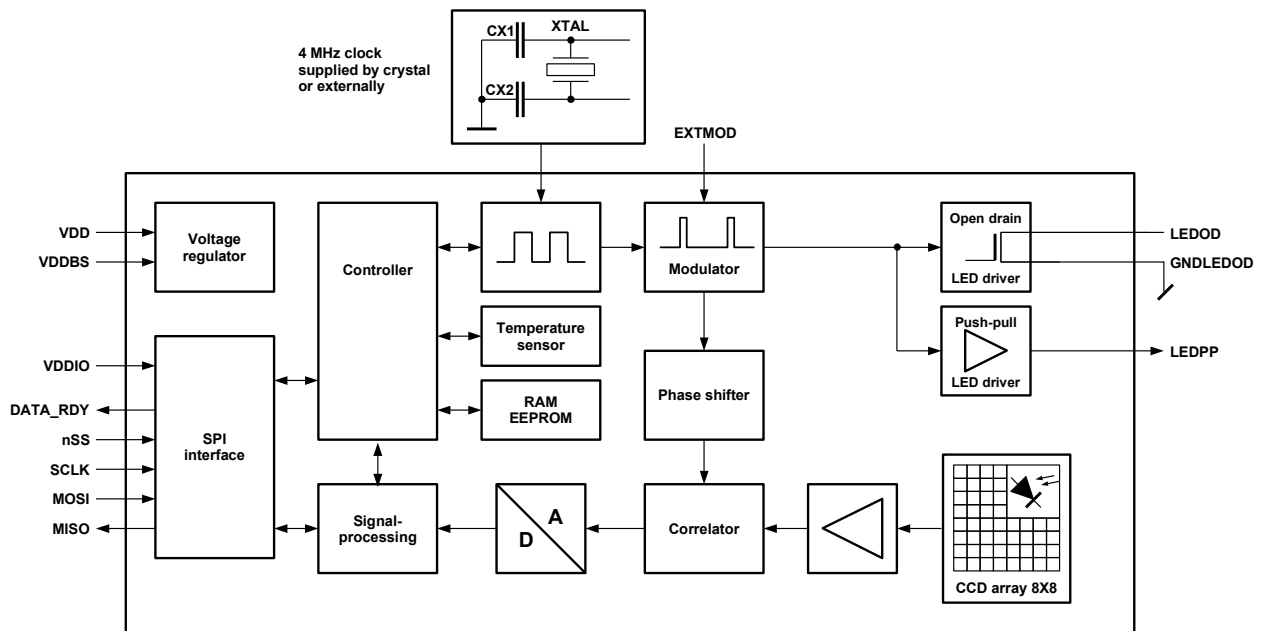


Figure 12: epc611 block diagram

Figure 12 shows the relationship between the functional blocks and the signal flow. Based on clock and mode setup, the modulation signal is generated and output over the LED driver to the external illumination (LED, VCSEL or laser diode LD). The illumination can be driven either directly by an open-drain MOS transistor (LEDOD) or digitally by the LEDPP output alternatively.

The pixel-field converts the returning IR light from the object to electrons. They are transferred depending on the phase information of the demodulation signal into two storage gates within each pixel (MGA and MGB). The AD conversion translates the phase information into a digital signal. After formatting, this is transmitted by the Serial Peripheral Interface (SPI) for external distance calculation.

All communication and/or data exchange with the epc611 occurs via the SPI interface.

The EEPROM holds default configuration and calibration data. The configuration is copied into the RAM registers during power up.

6.2. Typical application diagram

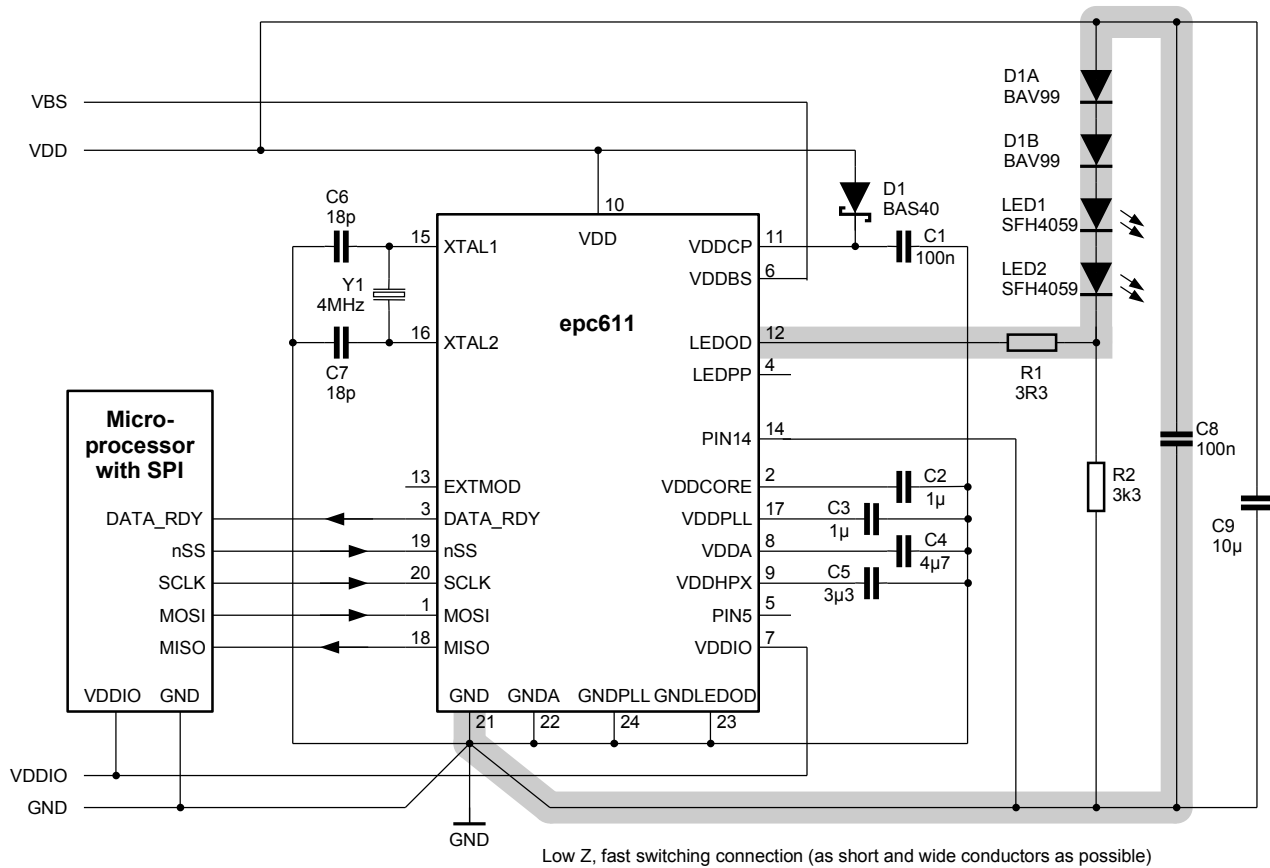


Figure 13: Typical application diagram

6.3. Application diagram part list

Part No.	Description	Pin No.	Value			Tolerance	Supply class V_{sc}	Comments
			Min.	Typ.	Max.			
C1	VDDCP	11 - 22	18 nF	100 nF	100 nF	±20 %	+12 V	Ceramic X7R
C2	VDDCORE	2 - 21	1 µF	1 µF	3.3 µF	±20 %	+1.8 V	Ceramic X7R
C3	VDDPLL	17 - 24	1 µF	1 µF	3.3 µF	±20 %	+1.8 V	Ceramic X7R
C4	VDDA	8 - 22	3.3 µF	4.7 µF	4.7 µF	±20 %	+5 V	Ceramic X7R
C5	VDDHPX	9 - 22	3.3 µF	3.3 µF	4.7 µF	±20 %	+10 V	Ceramic X7R
C6	XTAL1	15 - 21	See note ¹				+1.8 V	Ceramic NP0
C7	XTAL1	16 - 21	See note ¹				+1.8 V	Ceramic NP0
D1	VDD and VDDCP	10 - 11						Schottky diode
X1	XTAL	15 - 16	---	4 MHz	---	±100 ppm	+1.8 V	Quartz / Resonator

Table 11: Values of the components related to epc611 chip (Figure 13)

Notes:

¹ Refer to the datasheet of the crystal or resonator manufacturer, e.g. 18 pF

² Pin PIN5: Do not make any electrical connection except on a test pad (suggested)

6.4. Hardware implementation notes

- epc611 is supplied with two positive (V_{DDIO} and V_{DD}) and one negative (V_{DDBS}) DC voltages. Further voltages are generated on-chip from the V_{DD} supply (+8.5V).
- Internally generated supplies are decoupled by corresponding external capacitors. Decoupling capacitors must be placed next to each supply pair in order to minimise noise and instantaneous voltage drops. Do not use any of these voltages to supply any other circuitry.
- V_{DD} is the main supply. It needs to be stable and well regulated. It supplies all internally generated voltages.
- V_{DDIO} supplies the SPI interface digital I/Os. It must match the microprocessor's I/O voltage levels e.g. to 3.3 V. The supply range is according the specifications in Table 1.

5. V_{DDBS} voltage biases the pixel-field such as the reverse-bias of a photodiode. The use of a stable supply source with a low ripple is recommended. There is no circuit dependent current consumption, except ambient-light dependent leakage current (refer to Table 1, note 3).
6. All GND pins must have a good, powerful common connection with a minimum of noise.
7. The D1 Schottky diode is vital to ensure the correct power-up of the device.
8. Digital IO pins run up to 16 MHz and the high speed digital IO pin EXTMOD up to 80 MHz. The IO supply wires and layers need to be carefully designed and isolated so as to not introduce any noise onto the digital IO pins.
9. The nSS, SCLK, MOSI, and MISO signals refer to the SPI slave interface. Refer to Chapter 11.
10. DATA_RDY indicates valid image data.
IMPORTANT: It is not permitted to have any pull-up or pull-down resistor on this pin including pins of the application's CPU. The pin configuration of the application's CPU must always be set to input and never to output.
11. EXTMOD is an option to inject an external modulation clock.
12. Pin PIN5: It is not permitted to have any electrical connection except on a test pad (suggested).
13. It is recommended to have "not connected pins" (PINxx) available on test pads. This helps in several ways e.g. checking for correct orientation of the chip or for short-cuts after assembly.
14. Pins not listed here or explained later have to be connected according to Figure 13.

6.5. Clock sources

6.5.1. System clock supply

1. XTAL1 and XTAL2 are the input/output pins of the internal oscillator. They can be used either with a 4.0 MHz quartz crystal or resonator. The capacitor values C6 and C7 should follow the recommendation in the datasheet of the quartz or resonator (refer to Figure 13).
2. Instead of a crystal, an external 4 MHz clock source can be connected to the XTAL1. XTAL2 output pin left unconnected. The input clock signal level must match V_{DDPLL} supply level (see Table 1). If the external clock source comes from the +2.5/5.0V voltage domain, a resistor divider adapts it e.g. in Figure 14 and Table 12.
3. **IMPORTANT:** Precision and stability of the optical performance depends directly on this signal. Therefore, the external clock source must provide a clean, jitter-free and stable clock with fast rise and fall times.

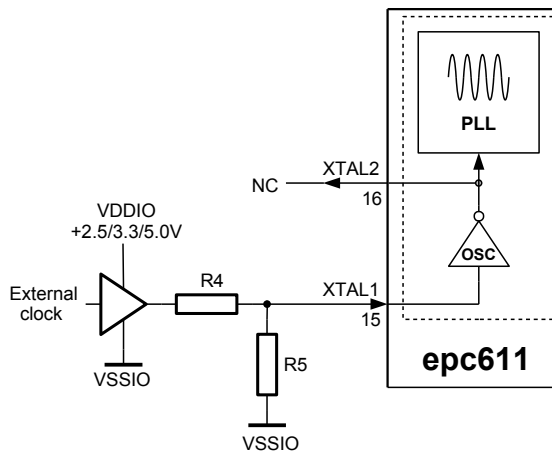


Figure 14: Resistor divider to adjust clock levels to V_{DDPLL}

Resistor	Clock signal amplitude V_{CLK}		
	2.5 V	3.3 V	5.0 V
R4	1.0 kOhm	1.0 kOhm	2.0 kOhm
R5	2.2 kOhm	1.2 kOhm	1.2 kOhm

Table 12: Resistor divider table

6.5.2. External modulation EXTMOD

An enhanced user application can also supply an external modulation clock to the chip. The optional EXTMOD input injects a user controlled/modulated clock for the LED driver and the pixel demodulator, see Figure 15.

The external EXTMOD clock is used for example in concepts for reliable multi camera applications. It allows the use of other modulation patterns e.g. frequency-division multiple access (FDMA). These concepts are explained in detail in various relevant documents. The user is free to apply any digital waveform up to 80 MHz during frame acquisition as EXTMOD signal. The user is also free to use modulations such as pseudo-random edge jitter, dithering, etc.

The signal from the EXTMOD pin is used as input for register P4[0x05] if bit 6 in register P4[0x00] is set to 1, instead of the clock generated internally.

Refer for the effective LED modulation signal to register P4[0x05].

The unambiguity range and the integration time are in this case based on the EXTMOD:

$$\text{Integration time} = \text{integration length multiplier} * (\text{Integration length} + 1) * (1 / f_{\text{mod_clk}})$$

For more details refer to register P4[0x05], Chapter 7.5. and 7.8.

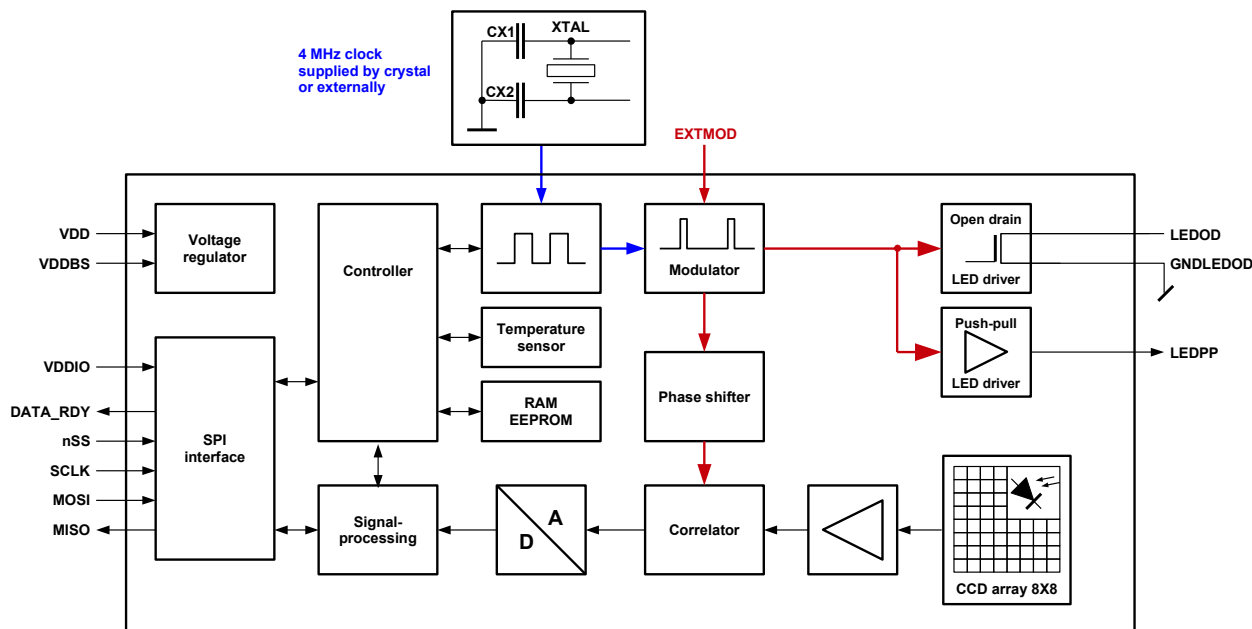


Figure 15: The EXTMOD signal flow (marked red)

6.6. Illumination (LED) driver

The chip can either directly drive laser diodes (LD e.g. VCSELs) and LEDs (LEDOD pin) or supply the modulation signal at I/O level on LEDPP pin for driving external, more powerful illumination sources. The modulation signal is 50% duty-cycle square-wave modulated and toggles up to 20 MHz.

The register P4[0x10] allows various settings e.g. polarity (inverts both LEDOD and LEDPP pins), depending on the external LED circuit used.

IMPORTANT:

- There are certain non-modulating DC modes which keep LED driver output turned on. Users must take care to avoid any damage by not exceeding operating conditions and max. limits of components.
- LEDOD is a power driving pin. Take care of the additional on-chip heat dissipation depending on the switching current, the integration time and the frame rate. It heats up the chip additionally and causes an additional temperature drift.
- Phase stability of the illumination may suffer from temperature, aging, etc. of the components. This can result in a distance error. A corresponding compensation by the user's software is suggested.

6.6.1. LEDOD pin

LEDOD is an open-drain nMOS FET driver output. This allows direct drive of illumination sources e.g. LD or LED. When the LED driver is active (ON), the LED current flows through the resistor R1 into the LEDOD pin, through the on-chip driver and comes out of the chip on the VSSLED ground pin (Figure 13).

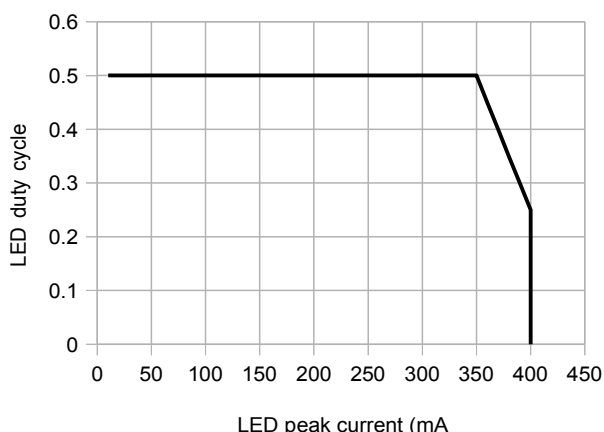


Figure 16: LED duty-cycle limits of LEDOD output

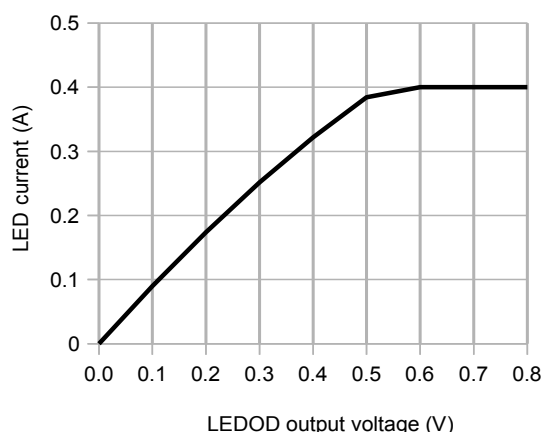


Figure 17: Typ. LEDOD output characteristics
Refer for maximum values to Table 1 and Table 2

The LEDOD pin toggles up to 20 MHz, or according to the modulation clock, with a current maximum of 400 mA limited by the R1 resistor. This signal creates a lot of ground noise. Therefore, the VSSLED pin is decoupled from the other analog grounds internally. It must be shorted with the other analog ground pins using a low-ohmic connection the shortest distance possible on the PCB. This way, there will be minimal voltage differences in the ground planes of the board. The LED supply line must be isolated properly from any analog supply on the PCB to minimize noise coupling from the LED drivers.

The number of LEDs depends on the level of the LED supply voltage and the turned-on forward voltage drop of the LEDs. The maximum voltage to the LEDOD pin is limited by the resistor R2 during LED off state.

6.6.2. LEDPP pin

The LEDPP pin is the alternative push-pull driver providing symmetric rise/fall times to drive external illumination drivers. It works from the +2.5/+5.0V V_{DDIO} supply and swings in the same voltage range as the IO pins. Do not use SPI communication during integration time. LEDPP pin solely should toggle during integration time. As a result, the LEDPP signal is not affected by the switching noise of other signal lines. LEDPP = LOW (approx. 0V) corresponds to LEDOD = OFF (max. output voltage).

LEDOD and LEDPP pins must not be used at the same time for driving the external illumination. They exhibit different phase delays and this can result in incorrect distance measurements.

6.7. DLL (Delay line)

The modulation signal can intentionally be delayed in order to add a phase-shift between the modulation of the light source and the demodulation of the backscattered light, refer to Figure 19.

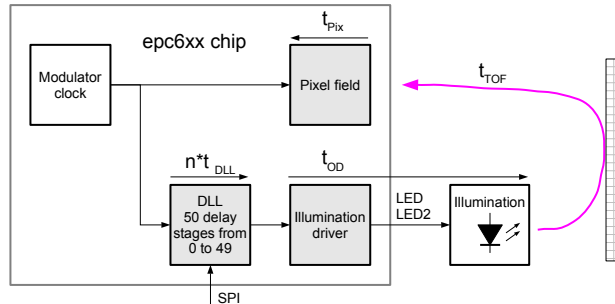


Figure 18: Block diagram of the DLL function

The purpose in doing this can be to ensure, the phase-shift between the modulated and the demodulated signal has a certain value in a specific distance range. For example, the highest distance accuracy with lowest distance noise can be achieved when the phase angle of demodulation is 45° . This is the case when all four DCS amplitudes have the same or a similar value. The worst situation is if one DCS pair is at its maximal amplitude whereas the other DCS pair is around zero (refer to Figure 18).

The DLL can be enabled in register P5[0x0E] whereas the delay of the LED modulation can be set in steps t_{DLL} by register P3[0x13] (approx. 2ns/step). The exact step t_{DLL} can be calculated with the value and the formula listed in register P6[0x1A]. This value varies from chip to chip and is also temperature dependent. The user must characterize the overall temperature drift of the complete camera to match the compensation.

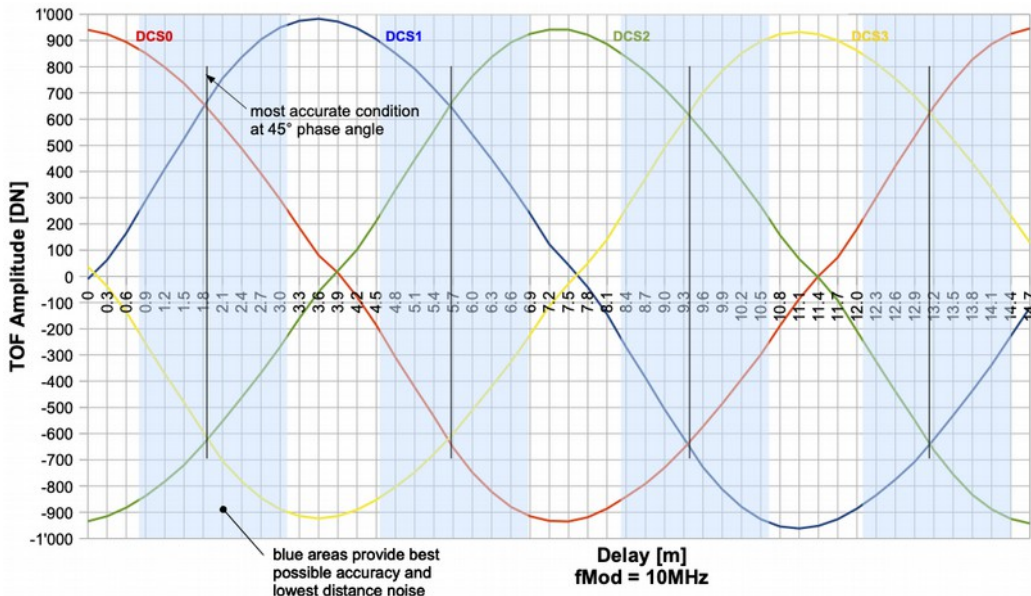


Figure 19: DCS amplitudes for the 4 DCSx (measurement data)

Example for 10 MHz modulation frequency:

If we want to optimize the accuracy of our TOF camera in the short range domain, e.g. 0m to 1m, the situation shown in Figure 19 is not ideal at all. The modulation frequency of the data shown in Figure 19 is 10 MHz whereas 50 DLL steps of approx. 2 ns are equivalent to 15 m distance. Shown in the diagram, the worst condition is in the first three DLL steps, which is equal to 0 ... 0.9 m. From then on, the

distance accuracy improves until DLL step 12. In other words, the distance accuracy from distance 0.9 ... 3.0 m is very good, but not from 0 ... 0.9 m. In order to be within an accurate distance measurement regime, the DLL should be shifted by 3 steps which means that the LED is delayed by 6ns.

6.8. Pixel-field

6.8.1. Pixel architecture

The pixels are placed in groups of 2x2 pixels (UE, UO, LE, LO), referred to hereafter as "pixel group". They are binned depending on the operating mode. The pixel performs two basic operations: Measurement (integration) and readout (A/D conversion).

This pixel group architecture allows the epc611 to operate the pixel-field in different modes and in combinations thereof, according to the following chapters.

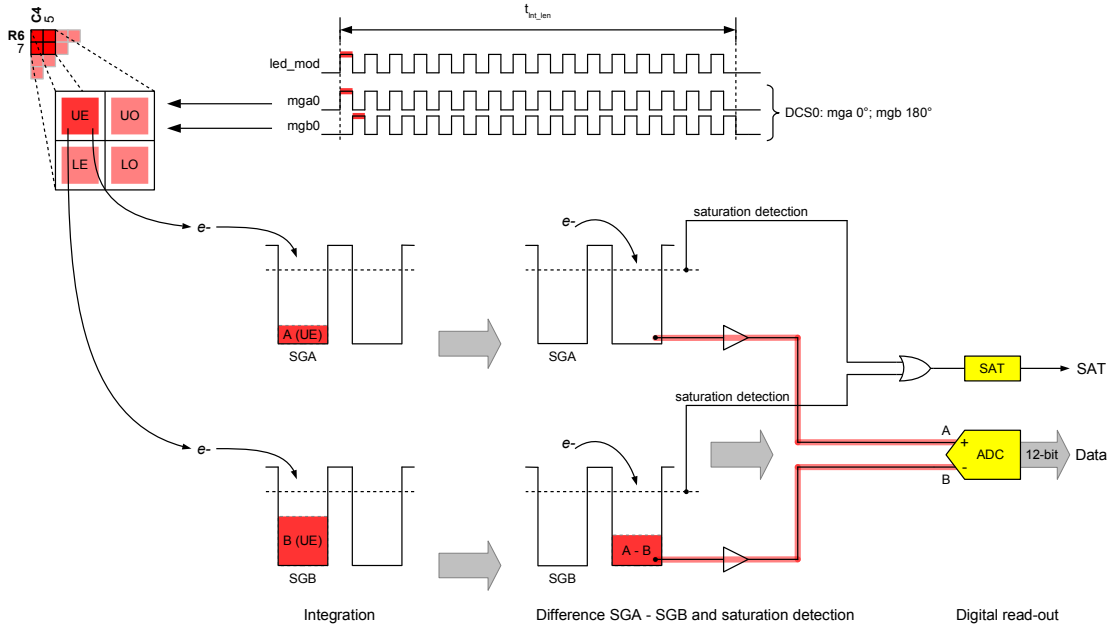


Figure 20: The 2x2 pixel group and simplified function overview

Each pixel has its own pair of storage gates, SGA and SGB. During integration, they accumulate the charges (e-) created by the modulated light reflected from the object (see Figure 25). They are controlled by the mga and mgb demodulation signals. When the integration is finished, the stored charges of SGA and SGB are read out as the difference A - B (ambient-light suppression) and converted into a single 12 bit digital value and 1 bit saturation flag. The output value can be either positive or negative, depending on the demodulated phase and the offset of the signal chain.

6.8.2. Pixel-field organization and readout

The basic pixel-field of the epc611 is 8x8 pixels (Figure 21).

Parameter	Pixel-field		Units
	Basic pixel	Binned pixel	
Pixel size	20 x 20	40 x 40	µm
Pixel-field organization	8 x 8	4 x 4	Pixel
Sensitivity	1x	approx. 4x	
Resolution	12	12	bit

Table 13: Pixel-field organization

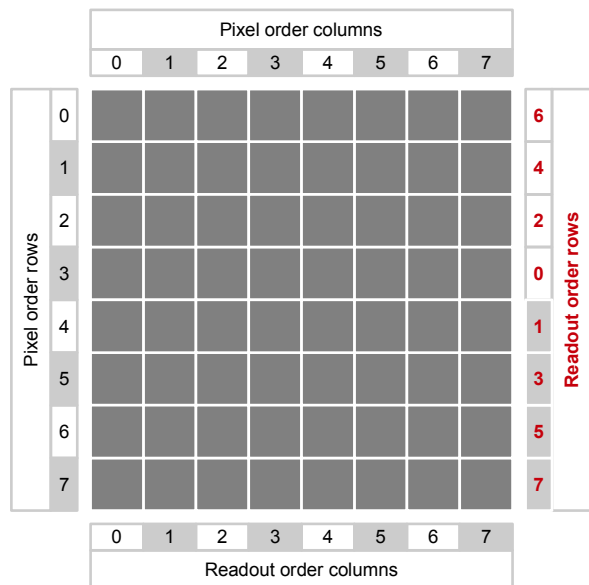


Figure 21: Basic pixel-field

Alternatively, enhanced range-finder features use horizontally and vertically analog binned 2x2 pixel groups, so-called “binned pixels”. Refer to Table 13 and for example Figure 30. More details are listed in the descriptions of the different specific operating modes.

In general, the data readout of the pixel-field is vertically split in the middle into two equal parts, top and bottom. Refer to the right y-axis description in red in Figure 21. This is due to the row readout which always converts two rows at same time, one from upper half and one from bottom half of the pixel-field, starting at the centre. The readout order for the columns is from left to right.

6.8.3. Pixel saturation detection

The pixels collect continuously modulated and non-modulated ambient-light during the integration period. Depending on these light intensities, sometimes the pixels collect more charge (over-exposure) than they can accommodate in their storage gates (refer to Figure 20). In such a case, the 12 bit sample data is not valid and cannot be used for distance calculation. Therefore, each pixel generates a “saturation flag” together with the sample data. It is set if one or more (in case of binned or summed pixels) are saturated. Binned pixels cannot collect more charge than a basic single pixel. The saturation flag is embedded and transmitted in the SPI data, depending on the operating mode. Refer for details to the specific mode description and Chapter 7.9.

6.8.4. ADC conversion over- and underflow

If pixels are strongly illuminated, they can reach the top or bottom end of the AD converter. This will be indicated by the flags “ADC over- or underflow”. Pixels, summed up on-chip, set this flag if one (or more) of the summing pixels reaches one of these limits. The flag is embedded and transmitted in the SPI data depending on the operating mode. Refer for details to the specific mode description and Chapter 7.9.

7. Imaging

7.1. epc611 functional overview

The epc611 design offers the possibility to adapt the properties of the chip to the user's target application. Instead of operating the chip as an TOF imager with 8x8 pixel, the configuration of the pixel-field can be changed to optimized, case specific, range-finder applications e.g. lowest noise, fastest speed, highest distance dynamic, no motion-blur, a mixture of these, etc. An overview is shown in Table 14 and Table 15 whereas more detailed information is available in the chapter of each specific operation mode.

Abbrev.	Description	Additional features
TIM	8x8 pixel 3D TOF Imager	
ULN	Ultra low noise range-finder	Digital sum of 8x8 pixels
UFS	Ultra fast and sensitive range-finder	Digital sum of 2x2 binned pixels
UHD	Ultra high dynamic (HDR) range-finder	Low noise, 8 different int. times, each digital sum of 8 pixels
LNH	Low noise high dynamic (HDR) range-finder	Sensitive, 4 int. times, each digital sum of 4 binned pixels
RBH	Reduced motion-blur HDR range-finder	Sensitive, low noise, 2 DCS, 2 int. times, each digital sum of 4 binned pixels
NBF	No motion-blur fast range-finder	Low noise, 4 DCS, each digital sum twice of 8 pixels
GIM	8x8 pixel grayscale imager	
GBI	4x4 pixel grayscale binned pixel imager	Binned pixels

Table 14: Basic mode overview

Abbrev.	Frame rate ³	Sensitivity	Signal output (Reference TIM mode)				Dynamic range	Motion blur
			per pixel size	Noise reduction	max. signal	Data format		
TIM	---	--- / 20 µm	---	---	12 bit	± 2'047 LSB	---	---
ULN	~ 1.1x	--- / 20 µm	8x	64x	18 bit	± 131'071 LSB	---	---
UFS	ultra fast: ~ 3.2x ¹	4x / 40 µm	2x	4x	14 bit	± 8'191 LSB	---	---
UHD	~ 1.1x	--- / 20 µm	2.8x	8x	15 bit	± 16'383 LSB	ultra HDR: ≤ 8x	---
LNH	fast: ~ 2.4x	4x / 40 µm	2x	4x	14 bit	± 8'191 LSB	high HDR: ≤ 4x	---
RBH	(~ 1.1x) ²	4x / 40 µm	2x (ext. sum)	4x	14 bit	± 8'191 LSB	high HDR: ≤ 2x	reduced
NBF	(~ 1.1x) ²	--- / 20 µm	4x (ext. sum)	8x	15 bit	± 16'383 LSB	---	no

Table 15: Basic features TOF modes (reference: TIM mode)

Notes:

¹ UFS mode uses a reduced photosensitive area 80 x 80 µm instead of 160 x 160 µm. This allows having 4x more illumination on the chip surface by using same optical emitting power with an adequately adapted receiving lens system.

² Based on 4 DCS mode. 1 DCS rolling mode not available.

³ Frame rate estimation is based on Table 70. Find more details in Chapter 7.4.

Notes on distance resolution and noise:

■ 4 DCS mode:

The distance resolution is the unambiguity distance divided by 8 times the current TOF amplitude (educated guess). The distance noise depends on the current TOF amplitude and decreases with increasing TOF amplitude. Refer to the graph of the corresponding operation mode e.g. Figure 29.

■ 2 DCS mode:

Decreases distance resolution by factor 2 compared to 4 DCS mode. Increases distance noise by factor 1.4 compared to 4 DCS mode.

■ Data reduction:

Distance data - Take care, data reduction of data formats during distance calculation and compensation can/will increase distance noise. Recommendation: Do data reduction only at last stage of the distance calculation and compensation.

■ Values used in the manual for specification, unless otherwise stated:

DCS data: normalized to 12 bit, signed integer
 TOF amplitude data: normalized to 11 bit, unsigned integer.

7.2. Time-of-flight modes (TOF)

The epc611 can be used in two basic time-of-flight application modes:

- Imager mode : Multipoint measurement by using the 8x8 pixel 3D TOF imager mode (TIM).
- Range-finder mode: Single point measurement. It is applicable for all the other modes.

IMPORTANT ADVICES FOR RANGE-FINDER MODES:

1. Homogeneous illumination of the pixel-field

The field of view of the entire 8x8 pixel pixel-field must be equal to or smaller than the target. Conversely, the size of the 8x8 pixel pixel-field must be smaller than the spot-size image of the object on the chip.

Rule: The pixels collect all the photons in their FOV independent of target's distances and reflectivities. The distance will be calculated based on the collected photons (DCSx values of the pixels). The result, sum over the involved pixels, is equally to the vectorial addition of their vectors.

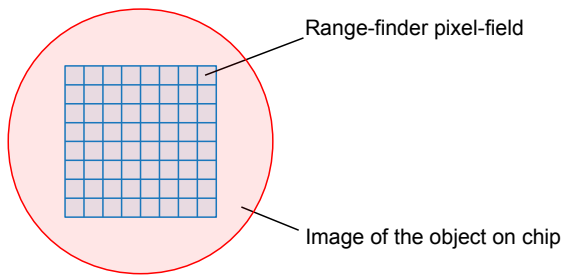


Figure 22: Homogeneous illumination

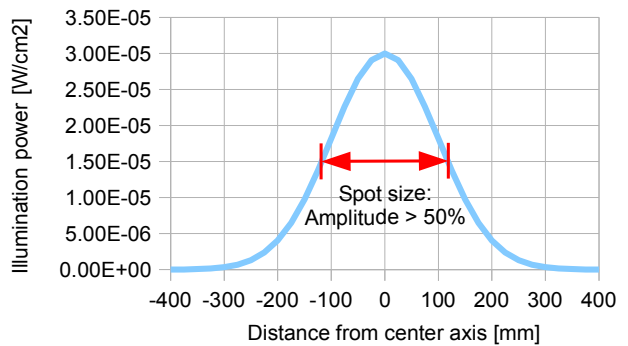


Figure 23: Intensity of spot size (principle graph)

2. Orientation of the pixel-field versus the divergence of the emitting and receiving beam

The plane formed by the emitting and receiving diverging beam axis must be parallel to the row axis. It reduces the influences of the intensity variations over distance, caused by divergence. The effect is usually visible due to fact that the spot on the object is not perfectly illuminated evenly.

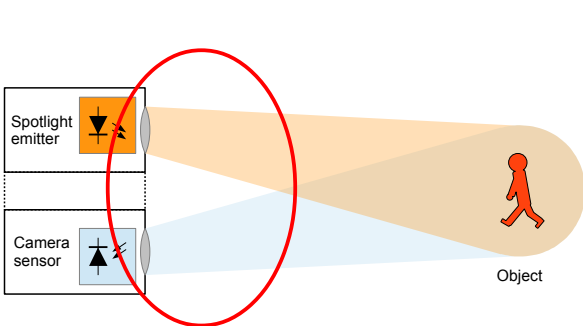


Figure 24: Divergence of emitting and receiving beam

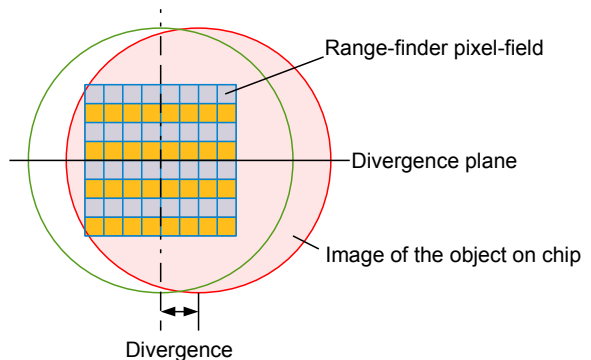


Figure 25: Pixel-field versus beam divergence

7.2.1. TIM mode: 8x8 pixel 3D ToF IMager

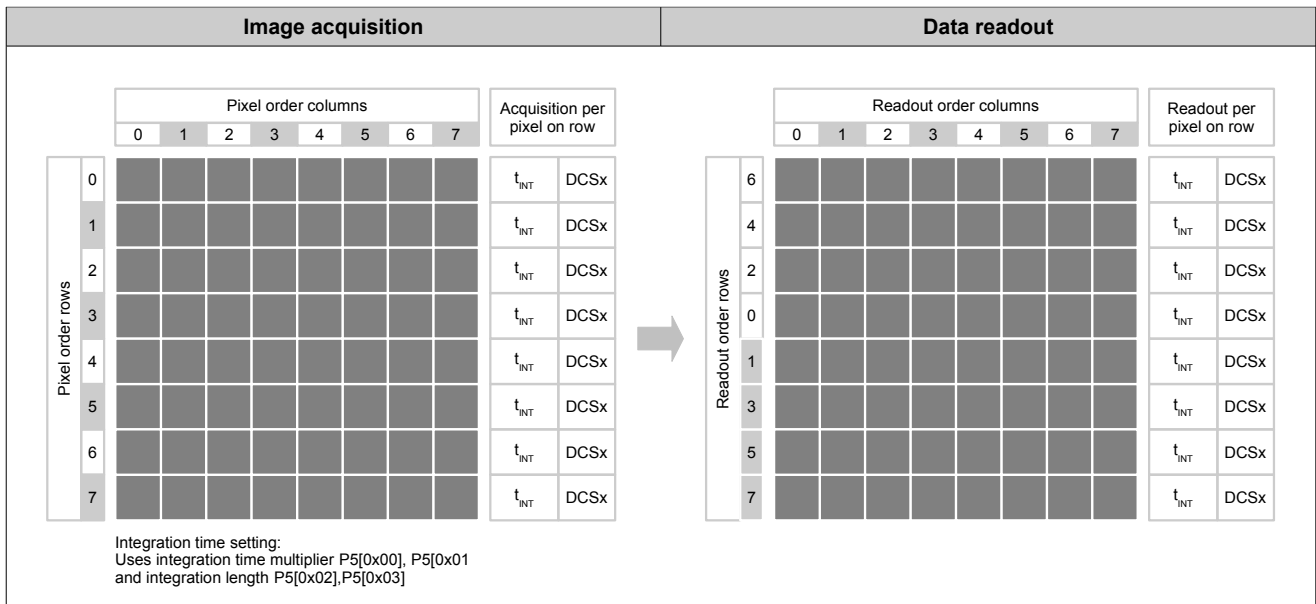


Figure 26: Pixel-field organization image acquisition		Figure 27: Pixel-field organization data readout	
No. of pixels / pixel size	64 pcs / 20 x 20 μm	No. of pixels / pixel size	64 pcs / 20 x 20 μm
Photosensitive area	160 x 160 μm	Data reduction on-chip	no
Sensitivity increase	no, basic sensitivity	Noise reduction	no
Integration times per frame	1x t_{INT}	Output data format	12 bit: $\pm 2^{047}$ LSB
Dynamic distance range increase	no	SPI transmission per frame	64 pixels in 96 words
DCS per frame	1x DCSx	TOF image rate @ 4 DCS, 50 μs int. time	up to 966 TOF images / sec.

Table 16: Operating mode specification

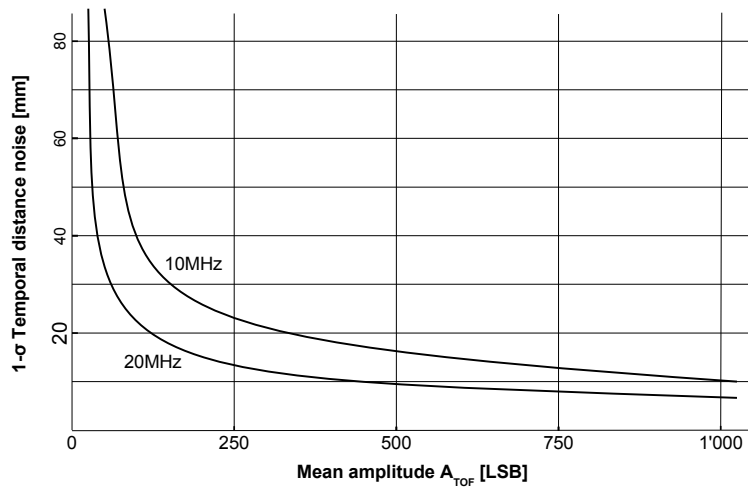


Figure 28: 1 sigma distance noise in TIM mode (typ.) as function of modulation frequency (single shot, 4 DCS, no ambient-light, graph shows lower amplitude range only)

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3D	0x30	0x23
2 DCS	DCS 0, 1	0x34	0x3D	0x10	
	DCS 2, 3	0x32	0x33		
1 DCS rolling	DCS 0	0x34	Not used	0x00	
	DCS 1	0x31			
	DCS 2	0x32			
	DCS 3	0x33			

Table 17: Register settings for the operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 12 bit/pixel, 64 pixel/frame with 96 SPI accesses

It starts in the centre of the vertical axis and uses a 2 pixel packed data format (pixel pair). It follows Table 18 and Table 19. The application must rearrange the pixels according to the pixel-field orientation.

The readout sequence is: 3 SPI readouts / pixel pair, 4 pair readouts / row, 8 row readouts / frame = 96 SPI readouts in total.

No sum readout: A pair of even and odd column pixels are packed into 3 SPI data bytes. Read 3x register P2[0x0C] per pixel pair																							
1 st SPI data byte: MSByte							2 nd SPI data byte							3 rd SPI data byte: LSByte									
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PIXEL_EVEN[11:4]							PIXEL_EVEN[3:0]					PIXEL_ODD[3:0]			PIXEL_ODD[11:4]								

Table 18: Pixel data SPI readout: Pixel pair read; refer to Figure 27

	1 st pair read / row	2 nd pair read / row	3 rd pair read / row	4 th pair read / row
1 st row read	Pixels row 3 / column 0 & 1	Pixels row 3 / column 2 & 3	Pixels row 3 / column 4 & 5	Pixels row 3 / column 6 & 7
2 nd row read	Pixels row 4 / column 0 & 1	Pixels row 4 / column 2 & 3	Pixels row 4 / column 4 & 5	Pixels row 4 / column 6 & 7
3 rd row read	Pixels row 2 / column 0 & 1	Pixels row 2 / column 2 & 3	Pixels row 2 / column 4 & 5	Pixels row 2 / column 6 & 7
4 th row read	Pixels row 5 / column 0 & 1	Pixels row 5 / column 2 & 3	Pixels row 5 / column 4 & 5	Pixels row 5 / column 6 & 7
...
7 th row read	Pixels row 0 / column 0 & 1	Pixels row 0 / column 2 & 3	Pixels row 0 / column 4 & 5	Pixels row 0 / column 6 & 7
8 th row read	Pixels row 7 / column 0 & 1	Pixels row 7 / column 2 & 3	Pixels row 7 / column 4 & 5	Pixels row 7 / column 6 & 7

Table 19: Pixel-field SPI double-row readout order; refer to Figure 27, based on pixel-field coordinates Figure 26

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 07 FF	Read register P2[0x0D] and P2[0x0E] ²
ADC overflow	0x 07 FE	Read register P2[0x10] and P2[0x11] ²
ADC underflow	0x 08 00	Read register P2[0x12] and P2[0x13] ²
Valid pixel data	0x 08 01 < ... < 0x 07 FD	[11:0]

Table 20: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Note 2: More details can be found in the corresponding register description.

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
- load sequencer program							
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 30	0x 84 00	4	0x12	0x30	
	Set TIM mode	0x 55 23	0x 52 30	4	0x15	0x23	Set 4 DCS 8x8 pixel ToF Imager Mode
	NOP	0x 00 00	0x 55 23				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- repeat for 4 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 98				Data ready – or alternatively DATA_RDY pin
	24 bytes available for readout = readout of a double-row						
	READ data 1	0x 2C 00	0x 00 00	2	0x0C		Readout double-row, uses embedded data format
	READ data 2	0x 2C 00	0x 2C ..	2	0x0C		MSByte0 (Row 3, pixel 0)
	READ data 3	0x 2C 00	0x 2C ..	2	0x0C		LSNibble0 LSNibble1
	READ data 4	0x 2C 00	0x 2C ..	2	0x0C		MSByte1 (Row 3, pixel 1)
	READ data 5	0x 2C 00	0x 2C ..	2	0x0C		MSByte2 (Row 3, pixel 2)

	READ data 22	0x 2C 00	0x 2C ..	2	0x0C		MSByte13 (Row 4, pixel 5)
	READ data 23	0x 2C 00	0x 2C ..	2	0x0C		MSByte14 (Row 4, pixel 6)
	READ data 24	0x 2C 00	0x 2C ..	2	0x0C		LSNibble14 LSNibble15
	NOP	0x 00 00	0x 2C ..				MSByte15 (Row 4, pixel 7)
Next row	- repeat 3x "Read row" for next 3 double-rows						
Next DCSx	- repeat 3x "Read frame DCSx" for next 3 frames						
End measurement							

Table 21: Basic example of TIM mode

7.2.2. ULN mode: Ultra Low Noise range-finder (sum of 8x8 pixels)

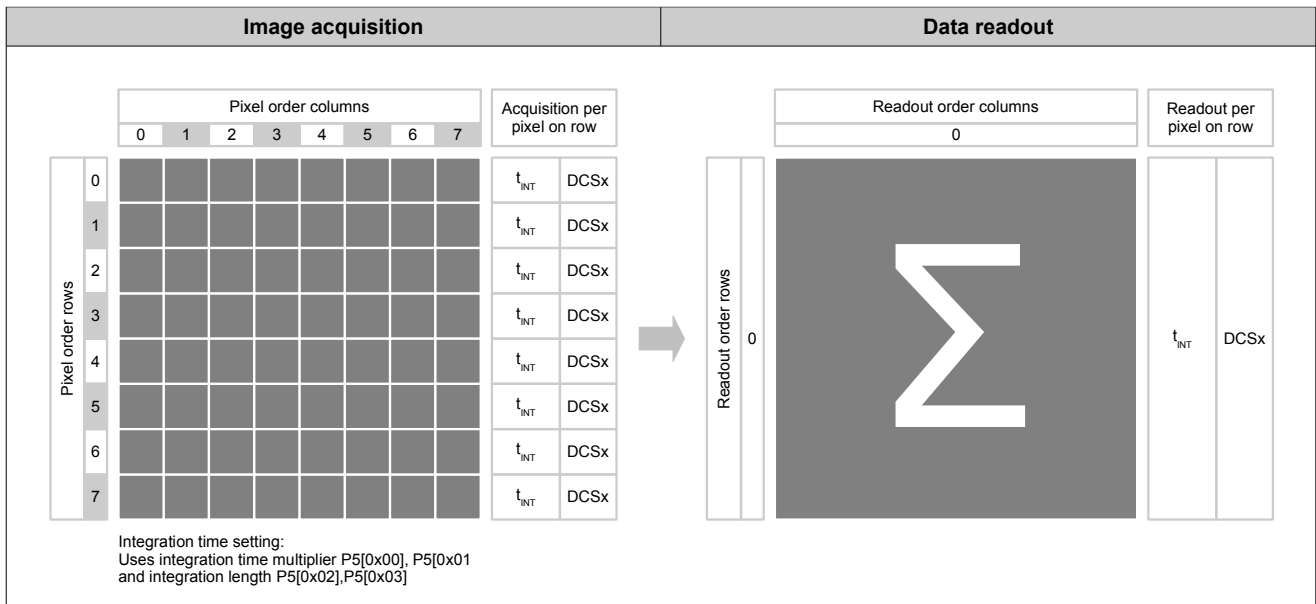


Figure 29: Pixel-field organization image acquisition		Figure 30: Pixel-field organization data readout	
No. of pixels / pixel size	64 pcs / 20 x 20 μm	No. of pixels / pixel size	1 pcs / 160 x 160 μm
Photosensitive area	160 x 160 μm	Data reduction on-chip	Digital sum of 64 pixels
Sensitivity increase	no	Noise reduction	8x
Integration times per frame	1x t_{INT}	Output data format	18 bit: $\pm 131'071$ LSB
Dynamic distance range increase	no	SPI transmission per frame	1 pixel in 3 words
DCS per frame	1x DCSx	TOF image rate @ 4 DCS, 50 μs int. time	up to 1'052 TOF images / sec.

Table 22: Operating mode specification

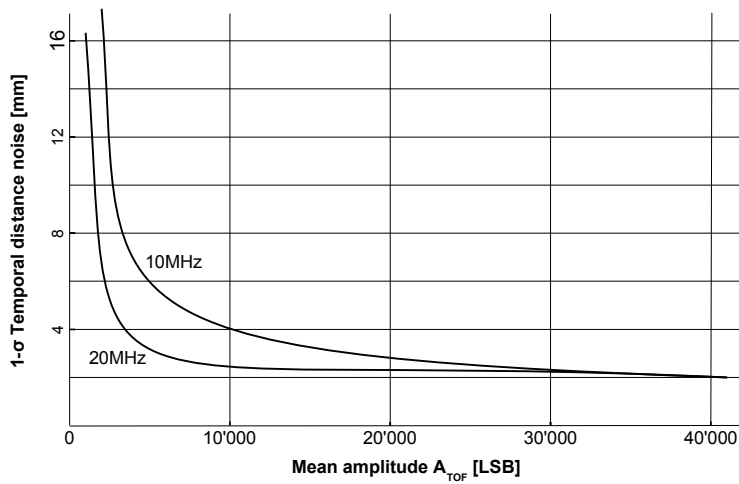


Figure 31: 1 sigma distance noise in ULN mode (typ.) as function of modulation frequency (single shot, 4 DCS, no ambient-light graph shows lower amplitude range only)

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3D	0x30	0x27
2 DCS	DCS 0, 1	0x34	0x3D	0x10	
	DCS 2, 3	0x32	0x33		
1 DCS rolling	DCS 0	0x34	Not used	0x00	
	DCS 1	0x31			
	DCS 2	0x32			
	DCS 3	0x33			

Table 23: Operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 1 pixel / frame with 3 SPI accesses

The data readout is 18 bit/pixel and only 1 pixel per frame. It follows Table 24.

64 pixel sum readout: Read 3x register P2[0x14] per pixel																							
1 st SPI data byte: MSByte							2 nd SPI data byte							3 rd SPI data byte: LSByte									
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SUM_DATA[17:0]																	0	0	0	UF	OF	SA	

Table 24: Pixel data SPI readout: 1 pixel only; refer to Figure 30

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 01 FF FF	SA
ADC overflow	0x 01 FF FE	OF
ADC underflow	0x 02 00 00	UF
Pixel data	0x 02 00 01 < ... < 0x 01 0F FD	[23:6]

Table 25: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 30	0x 84 00	4	0x12	0x30	
	Set ULN mode	0x 55 27	0x 52 30	4	0x15	0x27	Set 4 DCS Ultra Low-Noise mode
	NOP	0x 00 00	0x 55 27				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- read 1 pixel per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 83				Data ready – or alternatively DATA_RDY pin
	READ data 1	0x 34 00	0x 00 00	2	0x14		Readout 1 pixel, uses embedded data format
	READ data 2	0x 34 00	0x 34 ..	2	0x14		MSByte0
	READ data 3	0x 34 00	0x 34 ..	2	0x14		2 nd Byte0
	NOP	0x 00 00	0x 34 ..				LSByte0
Next DCSx	- repeat 3x "Read frame DCSx" for next 3 frames						
End measurement							

Table 26: Basic example of ULN mode

7.2.3. UFS mode: Ultra Fast and Sensitive range-finder (sum of 2x2 binned pixels)

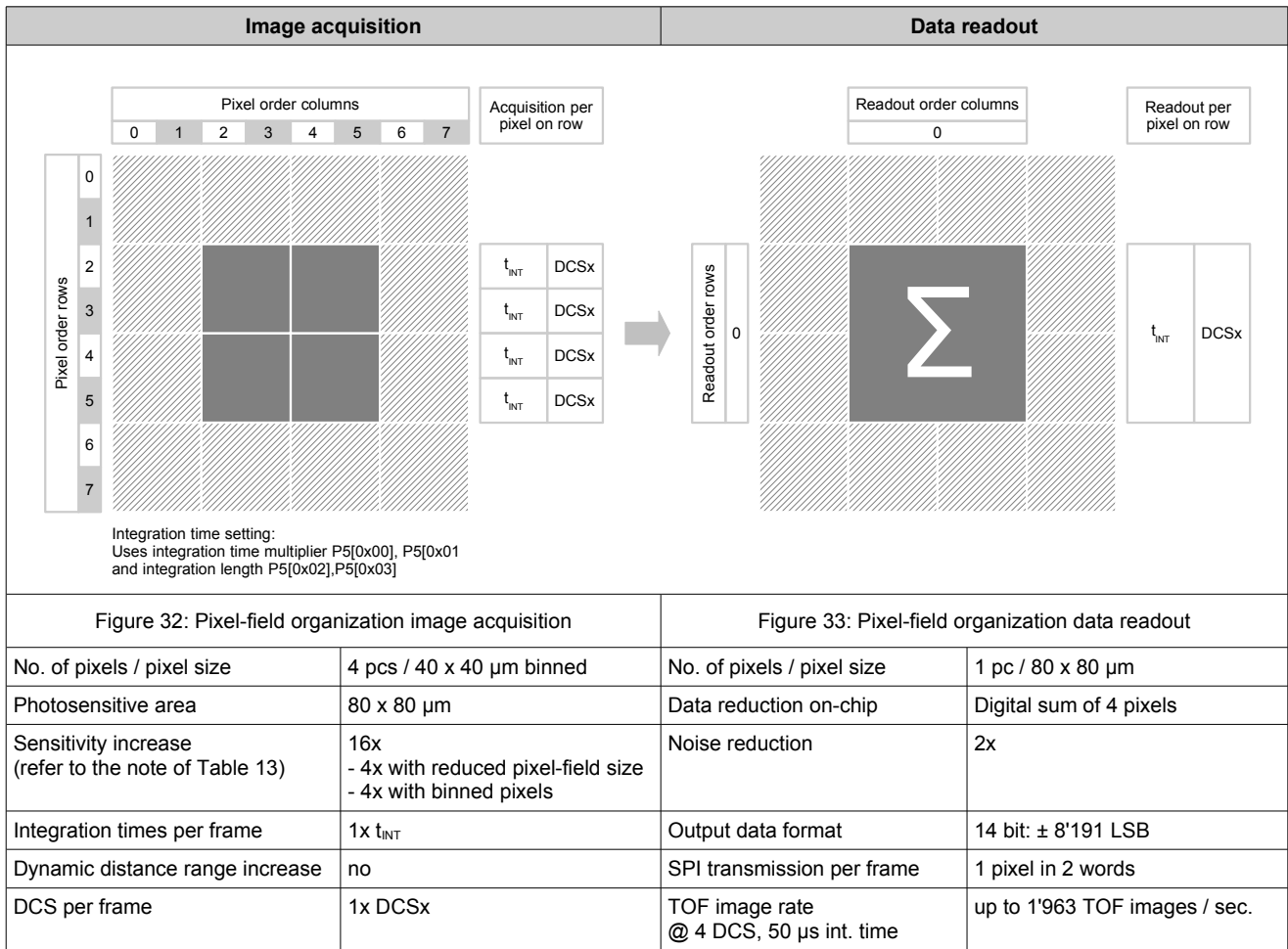


Table 27: Operating mode specification

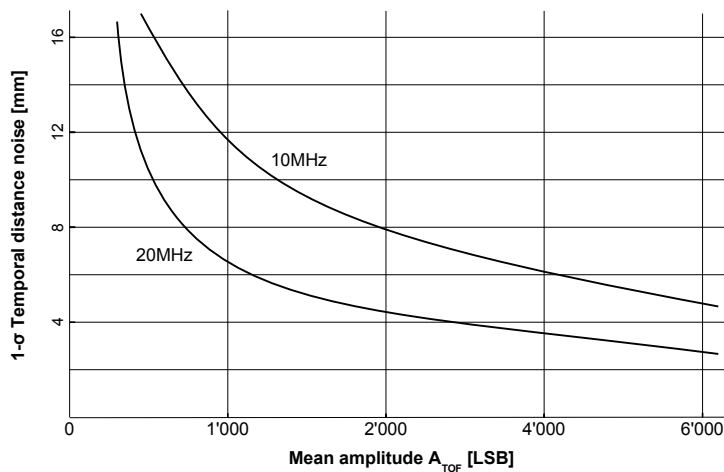


Figure 34: 1 sigma distance noise in UFS mode (typ.) as function of modulation frequency (single shot, 4 DCS, no ambient-light graph shows lower amplitude range only)

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3D	0x30	0x2B
2 DCS	DCS 0, 1	0x34	0x3D	0x10	
	DCS 2, 3	0x32	0x33		
1 DCS rolling	DCS 0	0x34	Not used	0x00	
	DCS 1	0x31			
	DCS 2	0x32			
	DCS 3	0x33			

Table 28: Operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 1 pixel / frame with 2 SPI accesses

The data readout is 14 bit/pixel and only 1 pixel per frame. It follows Table 24.

4 pixel sum readout: Read 2x register P2[0x14] per pixel															
1 st SPI data byte: MSByte								2 nd SPI data byte: LSByte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SUM_DATA[13:0]														OU	SA

Table 29: Pixel data SPI readout: 1 pixel only; refer to Figure 33

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 1F FF	SA
ADC overflow	0x 1F FE	OU
ADC underflow	0x 20 00	OU
Pixel data	0x 20 01 < ... < 0x 1F FD	[15:2]

Table 30: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 30	0x 84 00	4	0x12	0x30	
	Set UFS mode	0x 55 2B	0x 52 30	4	0x15	0x2B	Set 4 DCS Ultra Fast & Sensitive mode
	NOP	0x 00 00	0x 55 2B				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- read 1 pixel per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 82				Data ready – or alternatively DATA_RDY pin
	READ data 1	0x 34 00	0x 00 00	2	0x14		Readout 1 pixel, uses embedded data format
	READ data 2	0x 34 00	0x 34 ..	2	0x0C		MSByte0
	NOP	0x 00 00	0x 34 ..				LSByte0
Next DCSx	- repeat 3x "Read frame DCSx" for next 3 frames						
End measurement							

Table 31: Basic example of UFS mode

7.2.4. UHD mode: Ultra High Dynamic range-finder, low noise (8 different int. times, each sum of 8 pixels)

Image acquisition				Data readout													
		Pixel order columns					Acquisition per pixel on row				Readout order columns					Readout per pixel on row	
		0 1 2 3 4 5 6 7									0						
Pixel order rows	0	[8 blue pixels]					t_{INT_ROW0}	DCSx	Readout order rows	6	[Sum of 8 blue pixels]					t_{INT_ROW0}	DCSx
	1	[8 dark blue pixels]					t_{INT_ROW1}	DCSx		4	[Sum of 8 dark blue pixels]					t_{INT_ROW1}	DCSx
	2	[8 orange pixels]					t_{INT_ROW2}	DCSx		2	[Sum of 8 orange pixels]					t_{INT_ROW2}	DCSx
	3	[8 red pixels]					t_{INT_ROW3}	DCSx		0	[Sum of 8 red pixels]					t_{INT_ROW3}	DCSx
	4	[8 brown pixels]					t_{INT_ROW4}	DCSx		1	[Sum of 8 brown pixels]					t_{INT_ROW4}	DCSx
	5	[8 dark brown pixels]					t_{INT_ROW5}	DCSx		3	[Sum of 8 dark brown pixels]					t_{INT_ROW5}	DCSx
	6	[8 yellow-green pixels]					t_{INT_ROW6}	DCSx		5	[Sum of 8 yellow-green pixels]					t_{INT_ROW6}	DCSx
	7	[8 green pixels]					t_{INT_ROW7}	DCSx		7	[Sum of 8 green pixels]					t_{INT_ROW7}	DCSx
Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length row P7[0x00] ... P7[0x0F]																	
Figure 35: Pixel-field organization image acquisition				Figure 36: Pixel-field organization data readout													
No. of pixels / pixel size	64 pcs / 20 x 20 μm			No. of pixels / pixel size	8 pcs / 160 x 20 μm												
Photosensitive area	160 x 160 μm			Data reduction on-chip	Digital sum of 8 pixels												
Sensitivity increase	no			Noise reduction	2.8x												
Integration times per frame	8x t_{INT}			Output data format	15 bit: $\pm 16^{\wedge}383$ LSB												
Dynamic distance range increase	8x for range in dB			SPI transmission per frame	8 pixel in 16 words												
DCS per frame	1x DCSx			TOF image rate @ 4 DCS, 50 μs int. time	up to 518 TOF images/ sec.												

Table 32: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3D	0x38	0x2F
2 DCS	DCS 0, 1	0x34	0x3D	0x18	
	DCS 2, 3	0x32	0x33		
1 DCS rolling	DCS 0	0x34	Not used	0x08	
	DCS 1	0x31			
	DCS 2	0x32			
	DCS 3	0x33			

Table 33: Operating mode selection

Integration time setting: Follow Chapter 7.5.2, Multiple integration times per frame.

Data readout: 8 pixel / frame with 16 SPI accesses

The data readout is 15 bit/pixel. It starts in the centre of the vertical axis, has 1 pixel per row and follows Table 34 and Table 35. The application must rearrange the pixels according the pixel-field orientation.

8 pixel sum readout: Read 2x register P2[0x14] per pixel															
1 st SPI data byte: MSByte								2 nd SPI data byte: LSByte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SUM_DATA[14:0]															SA

Table 34: Pixel data SPI readout

1 st read	2 nd read	3 rd read	4 th read	5 th read	6 th read	7 th read	8 th read
Pixel row 3	Pixel row 4	Pixel row 2	Pixel row 5	Pixel row 1	Pixel row 6	Pixel row 0	Pixel row 7
t _{INT_ROW3}	t _{INT_ROW4}	t _{INT_ROW2}	t _{INT_ROW5}	t _{INT_ROW1}	t _{INT_ROW6}	t _{INT_ROW6}	t _{INT_ROW7}

Table 35: SPI double-row readout order; refer to Figure 36

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 3F FF	SA
ADC overflow	0x 3F FE	n/a
ADC underflow	0x 40 00	n/a
Valid pixel data	0x 40 01 < ... < 0x 3F FD	[15:1]

Table 36: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE, ready for communication
- load sequencer program							
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 38	0x 84 00	4	0x12	0x38	
	Set UHD mode	0x 55 2F	0x 52 38	4	0x15	0x2F	Set 4 DCS Ultra High-Dynamic range mode
	NOP	0x 00 00	0x 55 2F				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set INTM of max. int. time e.g. 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte. Same multiplier for all integration length registers
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
	Page select	0x 87 00	0x 41 01	7			
	Set int_len 16'384/128	0x E0 01	0x 87 00	7	0x00	0x01	Integration length row0, high byte
		0x E1 FF	0x E0 01	7	0x01	0xFF	Integration length row0, low byte
	Set int_len 16'384/64	0x E2 03	0x E1 FF	7	0x02	0x03	Integration length row1, high byte
		0x E3 FF	0x E2 03	7	0x03	0xFF	Integration length row1, low byte
	Set int_len 16'384/32	0x E4 07	0x E3 FF	7	0x04	0x07	Integration length row2, high byte
		0x E5 FF	0x E4 07	7	0x05	0xFF	Integration length row2, low byte
	Set int_len 16'384/16	0x E6 0F	0x E5 FF	7	0x06	0x0F	Integration length row3, high byte
		0x E7 FF	0x E6 0F	7	0x07	0xFF	Integration length row3, low byte
	Set int_len 16'384/8	0x E8 1F	0x E7 FF	7	0x08	0x1F	Integration length row4, high byte
		0x E9 FF	0x E8 1F	7	0x09	0xFF	Integration length row4, low byte
	Set int_len 16'384/4	0x EA 3F	0x E9 FF	7	0x0A	0x3F	Integration length row5, high byte
		0x EB FF	0x EA 3F	7	0x0B	0xFF	Integration length row5, low byte
	Set int_len 16'384/2	0x EC 7F	0x EB FF	7	0x0C	0x7F	Integration length row6, high byte
		0x ED FF	0x EC 7F	7	0x0D	0xFF	Integration length row6, low byte
	Set int_len 16'384	0x EE FF	0x ED FF	7	0x0E	0xFF	Integration length row7, high byte
	0x EF FF	0x EE FF	7	0x0F	0xFF	Integration length row7, low byte	
NOP	0x 00 00	0x EF FF	7				
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- repeat for 4 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 84				Data ready – or alternatively DATA_RDY pin
	4 bytes available for readout = readout of a double-row						
	READ data 1	0x 34 00	0x 00 00	2	0x14		Readout double-row, uses embedded data format
	READ data 2	0x 34 00	0x 34 ..	2	0x14		MSByte0 (row 3)
	READ data 3	0x 34 00	0x 34 ..	2	0x14		LSByte0 (row 3)
	READ data 4	0x 34 00	0x 34 ..	2	0x14		MSByte1 (row 4)
	NOP	0x 00 00	0x 34 ..				LSByte1 (row 4)
	Next row	- repeat 3x "Read row" for next 3 double-rows					
Next DCSx	- repeat 3x "Read frame DCSx" for next 3 frames						
End measurement							

Table 37: Basic example of UHD mode

7.2.5. LNH mode: Low Noise High dynamic range-finder, sensitive (4 int. times, each sum of 4 binned pixels)

Image acquisition				Data readout																																																																																																																																																																																	
<table border="1"> <tr> <td colspan="8">Pixel order columns</td> <td colspan="2">Acquisition per pixel on row</td> </tr> <tr> <td colspan="8">0 1 2 3 4 5 6 7</td> <td colspan="2"></td> </tr> <tr> <td rowspan="8">Pixel order rows</td> <td>0</td><td colspan="4">[Blue]</td><td colspan="4">[Blue]</td> <td>t_{INT_ROW0}</td><td>DCSx</td> </tr> <tr> <td>1</td><td colspan="4">[Blue]</td><td colspan="4">[Blue]</td> <td>t_{INT_ROW1}</td><td>DCSx</td> </tr> <tr> <td>2</td><td colspan="4">[Red]</td><td colspan="4">[Red]</td> <td>t_{INT_ROW2}</td><td>DCSx</td> </tr> <tr> <td>3</td><td colspan="4">[Red]</td><td colspan="4">[Red]</td> <td>t_{INT_ROW3}</td><td>DCSx</td> </tr> <tr> <td>4</td><td colspan="4">[Brown]</td><td colspan="4">[Brown]</td> <td>t_{INT_ROW4}</td><td>DCSx</td> </tr> <tr> <td>5</td><td colspan="4">[Brown]</td><td colspan="4">[Brown]</td> <td>t_{INT_ROW5}</td><td>DCSx</td> </tr> <tr> <td>6</td><td colspan="4">[Green]</td><td colspan="4">[Green]</td> <td>t_{INT_ROW6}</td><td>DCSx</td> </tr> <tr> <td>7</td><td colspan="4">[Green]</td><td colspan="4">[Green]</td> <td>t_{INT_ROW7}</td><td>DCSx</td> </tr> </table>				Pixel order columns								Acquisition per pixel on row		0 1 2 3 4 5 6 7										Pixel order rows	0	[Blue]				[Blue]				t_{INT_ROW0}	DCSx	1	[Blue]				[Blue]				t_{INT_ROW1}	DCSx	2	[Red]				[Red]				t_{INT_ROW2}	DCSx	3	[Red]				[Red]				t_{INT_ROW3}	DCSx	4	[Brown]				[Brown]				t_{INT_ROW4}	DCSx	5	[Brown]				[Brown]				t_{INT_ROW5}	DCSx	6	[Green]				[Green]				t_{INT_ROW6}	DCSx	7	[Green]				[Green]				t_{INT_ROW7}	DCSx	<table border="1"> <tr> <td colspan="8">Readout order columns</td> <td colspan="2">Readout per pixel on row</td> </tr> <tr> <td colspan="8">0</td> <td colspan="2"></td> </tr> <tr> <td rowspan="4">Readout order rows</td> <td>2</td><td colspan="4">[Blue]</td><td colspan="4">Σ</td> <td>t_{INT_A}</td><td>DCSx</td> </tr> <tr> <td>0</td><td colspan="4">[Red]</td><td colspan="4">Σ</td> <td>t_{INT_B}</td><td>DCSx</td> </tr> <tr> <td>1</td><td colspan="4">[Brown]</td><td colspan="4">Σ</td> <td>t_{INT_C}</td><td>DCSx</td> </tr> <tr> <td>3</td><td colspan="4">[Green]</td><td colspan="4">Σ</td> <td>t_{INT_D}</td><td>DCSx</td> </tr> </table>				Readout order columns								Readout per pixel on row		0										Readout order rows	2	[Blue]				Σ				t_{INT_A}	DCSx	0	[Red]				Σ				t_{INT_B}	DCSx	1	[Brown]				Σ				t_{INT_C}	DCSx	3	[Green]				Σ				t_{INT_D}	DCSx
Pixel order columns								Acquisition per pixel on row																																																																																																																																																																													
0 1 2 3 4 5 6 7																																																																																																																																																																																					
Pixel order rows	0	[Blue]				[Blue]				t_{INT_ROW0}	DCSx																																																																																																																																																																										
	1	[Blue]				[Blue]				t_{INT_ROW1}	DCSx																																																																																																																																																																										
	2	[Red]				[Red]				t_{INT_ROW2}	DCSx																																																																																																																																																																										
	3	[Red]				[Red]				t_{INT_ROW3}	DCSx																																																																																																																																																																										
	4	[Brown]				[Brown]				t_{INT_ROW4}	DCSx																																																																																																																																																																										
	5	[Brown]				[Brown]				t_{INT_ROW5}	DCSx																																																																																																																																																																										
	6	[Green]				[Green]				t_{INT_ROW6}	DCSx																																																																																																																																																																										
	7	[Green]				[Green]				t_{INT_ROW7}	DCSx																																																																																																																																																																										
Readout order columns								Readout per pixel on row																																																																																																																																																																													
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Readout order rows	2	[Blue]				Σ				t_{INT_A}	DCSx																																																																																																																																																																										
	0	[Red]				Σ				t_{INT_B}	DCSx																																																																																																																																																																										
	1	[Brown]				Σ				t_{INT_C}	DCSx																																																																																																																																																																										
	3	[Green]				Σ				t_{INT_D}	DCSx																																																																																																																																																																										
<p>Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length row P7[0x00] ... P7[0x0F]</p> <p>$t_{INT_A} = t_{INT_ROW0} = t_{INT_ROW1} / t_{INT_B} = t_{INT_ROW2} = t_{INT_ROW3}$ $t_{INT_C} = t_{INT_ROW4} = t_{INT_ROW5} / t_{INT_D} = t_{INT_ROW6} = t_{INT_ROW7}$</p>																																																																																																																																																																																					
Figure 37: Pixel-field organization image acquisition					Figure 38: Pixel-field organization data readout																																																																																																																																																																																
No. of pixels / pixel size	16 pcs / 40 x 40 μm				No. of pixels / pixel size	4 pcs / 160 x 40 μm																																																																																																																																																																															
Photosensitive area	160 x 160 μm				Data reduction on-chip	Digital sum of 4 pixels																																																																																																																																																																															
Sensitivity increase (refer to the note of Table 13)	4x with binned pixels				Noise reduction	2x																																																																																																																																																																															
Integration times per frame	4x t_{INT}				Output data format	14 bit: ± 8'191 LSB																																																																																																																																																																															
Dynamic distance range increase	4x for range in dB				SPI transmission per frame	4 pixel in 8 words																																																																																																																																																																															
DCS per frame	1x DCSx				TOF image rate @ 4 DCS, 50 μs int. time	up to 1'724 TOF images / sec.																																																																																																																																																																															

Table 38: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3D	0x38	0x33
2 DCS	DCS 0, 1	0x34	0x3D	0x18	
	DCS 2, 3	0x32	0x33		
1 DCS rolling	DCS 0	0x34	Not used	0x08	
	DCS 1	0x31			
	DCS 2	0x32			
	DCS 3	0x33			

Table 39: Operating mode selection

Integration time setting: Follow Chapter 7.5.2, Multiple integration times per frame.

Data readout: 4 pixel / frame with 8 SPI accesses

The data readout is 14 bit/pixel. It starts in the centre of the vertical axis, has 1 pixel per row and follows Table 52 and Table 41. The application must rearrange the pixels according the pixel-field orientation.

4 pixel sum readout: Read 2x register P2[0x14] per pixel															
1 st SPI data byte: MSByte								2 nd SPI data byte: LSByte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SUM_DATA[13:0]														OU	SA

Table 40: Pixel data SPI readout

1 st read	2 nd read	3 rd read	4 th read
Pixel row 2	Pixel row 4	Pixel row 0	Pixel row 6
t _{INT_B}	t _{INT_C}	t _{INT_A}	t _{INT_D}

Table 41: SPI double-row readout order; refer to Figure 38, based on even pixel-field coordinates Figure 37

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 1F FF	SA
ADC overflow	0x 1F FE	OU
ADC underflow	0x 20 00	OU
Pixel data	0x 20 01 < ... < 0x 1F FD	[15:2]

Table 42: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 38	0x 84 00	4	0x12	0x38	
	Set LNH mode	0x 55 33	0x 52 38	4	0x15	0x33	Set 4 DCS Low-Noise High-dynamic range mode
	NOP	0x 00 00	0x 55 33				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set INTM of max. int. time e.g. 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte. Same multiplier for all integration length registers
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
	Page select	0x 87 00	0x 41 01	7			
	Set int_len 16^384/64	0x E0 03	0x 87 00	7	0x00	0x03	Integration length row0, high byte
		0x E1 FF	0x E0 03	7	0x01	0xFF	Integration length row0, low byte
		0x E2 03	0x E1 FF	7	0x02	0x03	Integration length row1, high byte
		0x E3 FF	0x E2 03	7	0x03	0xFF	Integration length row1, low byte
	Set int_len 16^384/16	0x E4 0F	0x E3 FF	7	0x04	0x0F	Integration length row2, high byte
		0x E5 FF	0x E4 0F	7	0x05	0xFF	Integration length row2, low byte
		0x E6 0F	0x E5 FF	7	0x06	0x0F	Integration length row3, high byte
		0x E7 FF	0x E6 0F	7	0x07	0xFF	Integration length row3, low byte
	Set int_len 16^384/4	0x E8 3F	0x E7 FF	7	0x08	0x3F	Integration length row4, high byte
		0x E9 FF	0x E8 3F	7	0x09	0xFF	Integration length row4, low byte
		0x EA 3F	0x E9 FF	7	0x0A	0x3F	Integration length row5, high byte
		0x EB FF	0x EA 3F	7	0x0B	0xFF	Integration length row5, low byte
	Set int_len 16^384	0x EC FF	0x EB FF	7	0x0C	0xFF	Integration length row6, high byte
		0x ED FF	0x EC FF	7	0x0D	0xFF	Integration length row6, low byte
		0x EE FF	0x ED FF	7	0x0E	0xFF	Integration length row7, high byte
		0x EF FF	0x EE FF	7	0x0F	0xFF	Integration length row7, low byte
	NOP	0x 00 00	0x EF FF	7			
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- repeat for 2 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						Wait for end of exposure. Refer to imaging timing
	Read STATUS	0x 35 00	0x 35 00	2	0x15		
	NOP	0x 00 00	0x 35 84				Data ready – or alternatively DATA_RDY pin
							4 bytes available for readout = readout of a double-row
	READ data 1	0x 34 00	0x 00 00	2	0x14		Readout double-row, uses embedded data format
	READ data 2	0x 34 00	0x 34 ..	2	0x14		MSByte0 (row 1)
	READ data 3	0x 34 00	0x 34 ..	2	0x14		LSByte0 (row 1)
	READ data 4	0x 34 00	0x 34 ..	2	0x14		MSByte1 (row 2)
	NOP	0x 00 00	0x 34 ..				LSByte1 (row 2)
Next row	- repeat 1x "Read row" for next double-rows						
Next DCSx	- repeat 3x "Read frame DCSx" for next 3 frames						
End measurement							

Table 43: Basic example of LNH mode

7.2.6. RBH mode: Reduced motion-Blur HDR range-finder, sens., low noise (2 DCS, 2 int. times, each sum of 4 bin. pixels)

Image acquisition				Data readout			
<p>Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length row P7[0x00] ... P7[0x0F]</p> <p>$t_{INT_A} = t_{INT_ROW0} = t_{INT_ROW1} = t_{INT_ROW2} = t_{INT_ROW3}$ $t_{INT_B} = t_{INT_ROW4} = t_{INT_ROW5} = t_{INT_ROW6} = t_{INT_ROW7}$</p>							
Figure 39: Pixel-field organization image acquisition				Figure 40: Pixel-field organization data readout			
No. of pixels / pixel size	16 pcs / 40 x 40 μ m			No. of pixels / pixel size	16 pcs / 40 x 40 μ m		
Photosensitive area	160 x 160 μ m			Data reduction on-chip	No		
Sensitivity increase (refer to the note of Table 13)	4x with binned pixels			Noise reduction	- On-chip: no - 2x with external sum of 4 pixels per row		
Integration times per frame	2x t_{INT}			Output data format	12 bit: \pm 2'047 LSB		
Dynamic distance range increase	2x for range in dB			SPI transmission per frame	16 pixel in 24 words		
DCS per frame	2x DCSx (Motion-blur reduction)			TOF image rate @ 4 DCS, 50 μ s int. time	up to 3'268 TOF images / sec.		

Table 44: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3E	0x1A	0x37
2 DCS	DCS 0, 1	0x34	Not used	0x0A	
	DCS 2, 3	0x3E			

Table 45: Operating mode selection

Integration time setting: Follow Chapter 7.5.2, Multiple integration times per frame.

Data readout: 16 pixel / frame with 24 SPI accesses.

The data readout is 12 bit/pixel. It starts in the centre of the vertical axis, uses a 2 pixel packed data format (pixel pair). It follows Table 46 and Table 47. The application must rearrange the pixels according the pixel-field orientation. The readout sequence is: 3 SPI readouts / pixel pair, 2 pair readouts / row, 4 row readouts / frame = 24 SPI readouts in total.

Important:

The sum of the 4 equal DCS values per row should be used in the application. The data format increases to 14 bit and reduces the noise furthermore by factor 2.

No sum readout: A pair of even and odd column pixels are packed into 3 SPI data bytes. Read 3x register P2[0x0C] per pixel pair																							
1 st SPI data byte: MSByte							2 nd SPI data byte							3 rd SPI data byte: LSByte									
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PIXEL_EVEN[11:4]							PIXEL_EVEN[3:0]				PIXEL_ODD[3:0]			PIXEL_ODD[11:4]									

Table 46: Pixel data SPI readout: Pixel pair read; refer to Figure 40

	Acquisition	1 st pair read / row	2 nd pair read / row
1 st row read	t _{INT_A} / DCS1	Pixels row 2 / column 0 & 2	Pixels row 2 / column 4 & 6
2 nd row read	t _{INT_B} / DCS0	Pixels row 4 / column 0 & 2	Pixels row 4 / column 4 & 6
3 rd row read	t _{INT_A} / DCS0	Pixels row 0 / column 0 & 2	Pixels row 0 / column 4 & 6
4 th row read	t _{INT_B} / DCS1	Pixels row 6 / column 0 & 2	Pixels row 6 / column 4 & 6

Table 47: Pixel-field SPI double-row readout order; refer to Figure 40, based on even pixel-field coordinates Figure 39

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 07 FF	Read register P2[0x0D] and P2[0x0E] ²
ADC overflow	0x 07 FE	Read register P2[0x10] and P2[0x11] ²
ADC underflow	0x 08 00	Read register P2[0x12] and P2[0x13] ²
Valid pixel data	0x 08 01 < ... < 0x 07 FD	[11:0]

Table 48: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Note 2: More details can be found in the corresponding register description.

Action	Command	MOSI	MISO	Page	Reg	Value	Comment	
Power up	NOP	0x 00 00	0x ...				After startup	
	- repeat until IDLE:							
	NOP	0x 00 00	0x 00 00				IDLE: ready for communication	
- load sequencer program								
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1	
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00		
	Page select	0x 85 00	0x 5A 00	5			Page 5	
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00		
	NOP	0x 00 00	0x 4B 00				optional	
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4	
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F		
	Page select	0x 85 00	0x 48 1F	5			Page 5	
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01		
	Page select	0x 86 00	0x 4E 01	6			Page 6	
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62		
	NOP	0x 00 00	0x51 62				optional	
Set mode	Page select	0x 81 00	0x 00 00	1			Page 1	
	Select DCS	0x 45 3E	0x 81 00	1	0x05	0x3E	Set DCS acquisition for RBH mode. For other modes, set back to value before change e.g. 0x34 for 4 DCS.	
	Page select	0x 84 00	0x 45 3E	4			Page 4	
	Set modulation selection	0x 52 1A	0x 84 00	4	0x12	0x1A		
	Set RBH mode	0x 55 37	0x 52 1A	4	0x15	0x37	Set 4 DCS Reduced motion-Blur High-dynamic range mode	
	NOP	0x 00 00	0x 55 37					
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected	
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	is also integration time base	
	NOP	0x 00 00	0x 45 01				optional	
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5	
	Set INTM of max. int. time e.g. 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte. Same multiplier for all integration length registers	
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)	
	Page select	0x 87 00	0x 41 01	7				
	Set int_len 16384/10	0x E0 19	0x 87 00	7	0x00	0x19	Integration length row0, high byte	
		0x E1 99	0x E0 19	7	0x01	0x99	Integration length row0, low byte	
		0x E2 19	0x E1 99	7	0x02	0x19	Integration length row1, high byte	
		0x E3 99	0x E2 19	7	0x03	0x99	Integration length row1, low byte	
		0x E4 19	0x E3 99	7	0x04	0x19	Integration length row2, high byte	
		0x E5 99	0x E4 19	7	0x05	0x99	Integration length row2, low byte	
		0x E6 19	0x E5 99	7	0x06	0x19	Integration length row3, high byte	
		0x E7 99	0x E6 19	7	0x07	0x99	Integration length row3, low byte	
	Set int_len 16384	0x E8 FF	0x E7 99	7	0x08	0xFF	Integration length row4, high byte	
		0x E9 FF	0x E8 FF	7	0x09	0xFF	Integration length row4, low byte	
		0x EA FF	0x E9 FF	7	0x0A	0xFF	Integration length row5, high byte	
		0x EB FF	0x EA FF	7	0x0B	0xFF	Integration length row5, low byte	
		0x EC FF	0x EB FF	7	0x0C	0xFF	Integration length row6, high byte	
		0x ED FF	0x EC FF	7	0x0D	0xFF	Integration length row6, low byte	
		0x EE FF	0x ED FF	7	0x0E	0xFF	Integration length row7, high byte	
		0x EF FF	0x EE FF	7	0x0F	0xFF	Integration length row7, low byte	
	NOP	0x 00 00	0x EF FF	7				
	Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
		Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
NOP		0x 00 00	0x 58 01				optional	
Read frame DCSx	- repeat for DCS0 ... DCS3:							
Read row	- repeat for 2 double-rows per frame:							
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected	
	Read STATUS	0x 35 00	0x 82 00	2	0x15			
	- repeat until DATA_RDY:							
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing	
	NOP	0x 00 00	0x 35 8C				Data ready -- or alternatively DATA_RDY pin	
	12 bytes available for readout = readout of a double-row							
	READ data 1	0x 2C 00	0x 00 00	2	0x0C		Readout double-row, uses embedded data format	
	READ data 2	0x 2C 00	0x 2C ..	2	0x0C		MSByte0 (Row 1, pixel 0)	
	READ data 3	0x 2C 00	0x 2C ..	2	0x0C		LSNibble0 LSNibble1	
	READ data 4	0x 2C 00	0x 2C ..	2	0x0C		MSByte1 (Row 1, pixel 1)	
	READ data 5	0x 2C 00	0x 2C ..	2	0x0C		MSByte2 (Row 1, pixel 2)	
	
	READ data 10	0x 2C 00	0x 2C ..	2	0x0C		MSByte5 (Row 2, pixel 1)	
	READ data 11	0x 2C 00	0x 2C ..	2	0x0C		MSByte6 (Row 2, pixel 2)	
READ data 12	0x 2C 00	0x 2C ..	2	0x0C		LSNibble6 LSNibble7		
NOP	0x 00 00	0x 2C ..				MSByte7 (Row 2, pixel 3)		
Next row	- repeat 1x "Read row" for next double-row							
Next DCSx	- repeat 1x "Read frame DCSx" for next 1 frames							
End measurement.								

Table 49: Basic example of RBH mode

7.2.7. NBF mode: No motion-Blur Fast range-finder, low noise (4 DCS, each sum twice of 8 pixels)

Image acquisition				Data readout			
Pixel order columns		Acquisition per pixel on row		Readout order columns		Readout per pixel on row	
0 1 2 3 4 5 6 7				0			
Pixel order rows	0	Blue	t_{INT} DCS0	Readout order rows	6	Blue Σ	t_{INT} DCS0
	1	Blue	t_{INT} DCS0		4	Blue Σ	t_{INT} DCS0
	2	Red	t_{INT} DCS1		2	Red Σ	t_{INT} DCS1
	3	Red	t_{INT} DCS1		0	Red Σ	t_{INT} DCS1
	4	Brown	t_{INT} DCS2		1	Brown Σ	t_{INT} DCS2
	5	Brown	t_{INT} DCS2		3	Brown Σ	t_{INT} DCS2
	6	Green	t_{INT} DCS3		5	Green Σ	t_{INT} DCS3
	7	Green	t_{INT} DCS3		7	Green Σ	t_{INT} DCS3
Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length P5[0x02], P5[0x03]							
Figure 41: Pixel-field organization image acquisition				Figure 42: Pixel-field organization data readout			
No. of pixels / pixel size	64 pcs / 20 x 20 μm			No. of pixels / pixel size	8 pcs / 160 x 20 μm		
Photosensitive area	160 x 160 μm			Data reduction on-chip	Digital sum of 8 pixels		
Sensitivity increase	no			Noise reduction	- On-chip: 2.8x - 4x with external sum of corresponding two pixels		
Integration times per frame	1x t_{INT}			Output data format	15 bit: $\pm 16'383$ LSB		
Dynamic distance range increase	no			SPI transmission per frame	8 pixel in 16 words		
DCS per frame	4x DCSx (no motion-blur)			TOF image rate @ 4 DCS, 50 μs int. time	up to 4'188 TOF images / sec.		

Table 50: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P1[0x02]	P1[0x05]	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	DCS selection 1 st frame	DCS selection 2 nd frame	Modulation selection	Readout mode
4 DCS	DCS 0, 1, 2, 3	0x34	0x3E	0x03	0x2F

Table 51: Operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 8 pixel / frame with 16 SPI accesses

The data readout is 15 bit/pixel. It starts in the centre of the vertical axis, has 1 pixel per row and follows Table 52 and Table 41. The application must rearrange the pixels according the pixel-field orientation.

Important:

The sum of the equal DCS pairs should be used in the application. The data format increases to 16 bit and reduces the noise furthermore by factor 1.4.

8 pixel sum readout: Read 2x register P2[0x14] per pixel															
1 st SPI data byte: MSByte								2 nd SPI data byte: LSByte							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SUM_DATA[14:0]															SA

Table 52: Pixel data SPI readout

1 st read	2 nd read	3 rd read	4 th read	5 th read	6 th read	7 th read	8 th read
Pixel row 3	Pixel row 4	Pixel row 2	Pixel row 5	Pixel row 1	Pixel row 6	Pixel row 0	Pixel row 7
DCS1	DCS2	DCS1	DCS2	DCS0	DCS3	DCS0	DCS3

Table 53: SPI double-row readout order; refer to Figure 42

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 3F FF	SA
ADC overflow	0x 3F FE	n/a
ADC underflow	0x 40 00	n/a
Valid pixel data	0x 40 01 < ... < 0x 3F FD	[15:1]

Table 54: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x .. .				After startup
	- repeat until IDLE:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1 (all chip versions)	Page select	0x 81 00	0x 00 00	1			Page 1
	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2 (only for WAFER ID <13)	Page select	0x 84 00	0x 00 00	4			Page 4
	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 81 00	0x 00 00	1			Page 1
	Set DCS select 2 nd frame	0x 45 3E	0x 81 00	1	0x05	0x3E	
	Page select	0x 84 00	0x 45 3E	4			Page 4
	Set modulation selection	0x 52 03	0x 84 00	4	0x12	0x03	
	Set NBF mode	0x 55 2F	0x 52 03	4	0x15	0x2F	Set 4 DCS No motion-Blur Fast mode
	NOP	0x 00 00	0x 55 2F				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx	- repeat for DCS0 ... DCS3:						
Read row	- repeat for 4 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 84				Data ready – or alternatively DATA_RDY pin
	4 bytes available for readout = readout of a double-row						
	READ data 1	0x 34 00	0x 00 00	2	0x14		Readout double-row, uses embedded data format
	READ data 2	0x 34 00	0x 34 ..	2	0x14		MSByte0 (row 3)
	READ data 3	0x 34 00	0x 34 ..	2	0x14		LSByte0 (row 3)
	READ data 4	0x 34 00	0x 34 ..	2	0x14		MSByte1 (row 4)
	NOP	0x 00 00	0x 34 ..				LSByte1 (row 4)
	Next row	- repeat 3x "Read row" for next 3 double-rows					
End measurement							

Table 55: Basic example of NBF mode

7.3. Grayscale imager modes

7.3.1. GIM mode: 8x8 pixel Grayscale IMager

Image acquisition				Data readout			
<p>Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length P5[0x02], P5[0x03]</p>							
Figure 43: Pixel-field organization image acquisition				Figure 44: Pixel-field organization data readout			
No. of pixels / pixel size	64 pcs / 20 x 20 μm			No. of pixels / pixel size	64 pcs / 20 x 20 μm		
Photosensitive area	160 x 160 μm			Data reduction on-chip	no		
Sensitivity increase	no, basic sensitivity			Noise reduction	no		
Integration times per frame	1x t _{INT}			Output data format	12 bit: ± 2 ⁰⁴⁷ LSB, effective 0 ... +2 ⁰⁴⁷ LSB, small negative numbers can occur		
Dynamic distance range increase	---			SPI transmission per frame	64 pixels in 96 words		
DCS per frame	1x DCSx			Image rate @ 50 μs int. time	up to 3'865 TOF images / sec.		

Table 56: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	Modulation selection	Readout mode
Grayscale	1 frame	0xC0	0x23

Table 57: Operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 64 pixel / frame with 96 SPI accesses

The data readout is 12 bit/pixel. It starts in the centre of the vertical axis and uses a 2 pixel packed data format (pixel pair). It follows Table 58 and Table 59. The application must rearrange the pixels according the pixel-field orientation.

The readout sequence is: 3 SPI readouts / pixel pair, 4 pair readouts / row, 8 row readouts / frame = 96 SPI readouts in total.

No sum readout: A pair of even and odd column pixels are packed into 3 SPI data bytes. Read 3x register P2[0x0C] per pixel pair																							
1 st SPI data byte: MSByte							2 nd SPI data byte							3 rd SPI data byte: LSByte									
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PIXEL_EVEN[11:4]							PIXEL_EVEN[3:0]				PIXEL_ODD[3:0]			PIXEL_ODD[11:4]									

Table 58: Pixel data SPI readout: Pixel pair read; refer to Figure 44

	1 st pair read / row	2 nd pair read / row	3 rd pair read / row	4 th pair read / row
1 st row read	Pixels row 3 / column 0 & 1	Pixels row 3 / column 2 & 3	Pixels row 3 / column 4 & 5	Pixels row 3 / column 6 & 7
2 nd row read	Pixels row 4 / column 0 & 1	Pixels row 4 / column 2 & 3	Pixels row 4 / column 4 & 5	Pixels row 4 / column 6 & 7
3 rd row read	Pixels row 2 / column 0 & 1	Pixels row 2 / column 2 & 3	Pixels row 2 / column 4 & 5	Pixels row 2 / column 6 & 7
4 th row read	Pixels row 5 / column 0 & 1	Pixels row 5 / column 2 & 3	Pixels row 5 / column 4 & 5	Pixels row 5 / column 6 & 7
...
7 th row read	Pixels row 0 / column 0 & 1	Pixels row 0 / column 2 & 3	Pixels row 0 / column 4 & 5	Pixels row 0 / column 6 & 7
8 th row read	Pixels row 7 / column 0 & 1	Pixels row 7 / column 2 & 3	Pixels row 7 / column 4 & 5	Pixels row 7 / column 6 & 7

Table 59: Pixel-field SPI double-row readout order; refer to Figure 44, based on pixel-field coordinates Figure 43

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 07 FF	Read register P2[0x0D] and P2[0x0E] ²
ADC overflow	0x 07 FE	Read register P2[0x10] and P2[0x11] ²
ADC underflow	0x 08 00	Read register P2[0x12] and P2[0x13] ²
Valid pixel data	0x 08 01 < ... < 0x 07 FD	[11:0]

Table 60: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Note 2: More details can be found in the corresponding register description.

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1	Page select	0x 81 00	0x 00 00	1			Page 1
(all chip versions)	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2	Page select	0x 84 00	0x 00 00	4			Page 4
(only for WAFER ID <13)	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 C0	0x 84 00	4	0x12	0xC0	
	Set GMI mode	0x 55 23	0x 52 C0	4	0x15	0x23	Set 8x8 pixel Grayscale IMager mode mode
	NOP	0x 00 00	0x 55 23				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
Sets integration time base	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx							
Read row	- repeat for 4 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 98				Data ready – or alternatively DATA_RDY pin
	24 bytes available for readout = readout of a double-row						
	- repeat until:						
	Readout double-row: Repeat this procedure 4 times per frame						
	READ data 1	0x 2C 00	0x 00 00	2	0x0C		Readout uses embedded data format
	READ data 2	0x 2C 00	0x 2C ..	2	0x0C		MSByte0 (Row 3, pixel 0)
	READ data 3	0x 2C 00	0x 2C ..	2	0x0C		LSNibble0 LSNibble1
	READ data 4	0x 2C 00	0x 2C ..	2	0x0C		MSByte1 (Row 3, pixel 1)
	READ data 5	0x 2C 00	0x 2C ..	2	0x0C		MSByte2 (Row 3, pixel 2)

	READ data 22	0x 2C 00	0x 2C ..	2	0x0C		MSByte13 (Row 4, pixel 5)
	READ data 23	0x 2C 00	0x 2C ..	2	0x0C		MSByte14 (Row 4, pixel 6)
READ data 24	0x 2C 00	0x 2C ..	2	0x0C		LSNibble14 LSNibble15	
NOP	0x 00 00	0x 2C ..				MSByte15 (Row 4, pixel 7)	
Next row	- repeat 3x "Read row" for next 3 double-rows						
End measurement							

Table 61: Basic example of GIM mode

7.3.2. GBI mode: 4x4 pixel Grayscale Binned pixel Imager

Image acquisition				Data readout			
<p>Integration time setting: Uses integration time multiplier P5[0x00], P5[0x01] and integration length P5[0x02], P5[0x03]</p>							
Figure 45: Pixel-field organization image acquisition				Figure 46: Pixel-field organization data readout			
No. of pixels / pixel size	16 pcs / 40 x 40 μm binned			No. of pixels / pixel size	16 pcs / 20 x 20 μm		
Photosensitive area	160 x 160 μm			Data reduction on-chip	no		
Sensitivity increase (refer to the note of Table 13)	4x with binned pixels			Noise reduction	no		
Integration times per frame	1x t_{INT}			Output data format	12 bit: $\pm 2^{047}$ LSB, effective 0 ... $+2^{047}$ LSB, small negative numbers can occur		
Dynamic distance range increase	---			SPI transmission per frame	16 pixels in 24 words		
DCS per frame	1x DCSx			Image rate @ 50 μs int. time	up to 6'536 TOF images / sec.		

Table 62: Operating mode specification

Operating mode selection: Depends on the number of DCS frames per SHUTTER stimulation:

	Register	P4[0x12]	P4[0x15]
Mode	DCS / SHUTTER	Modulation selection	Readout mode
Grayscale	1 frame	0xC0	0x37

Table 63: Operating mode selection

Integration time setting: Follow Chapter 7.5.1, Single integration time per frame.

Data readout: 16 pixel / frame with 24 SPI accesses

The data readout is 12 bit/pixel. It starts in the centre of the vertical axis and uses a 2 pixel packed data format (pixel pair). It follows Table 64 and Table 65. The application must rearrange the pixels according the pixel-field orientation.

The readout sequence is: 3 SPI readouts / pixel pair, 2 pair readouts / row, 4 row readouts / frame = 24 SPI readouts in total.

No sum readout: A pair of even and odd column pixels are packed into 3 SPI data bytes. Read 3x register P2[0x0C] per pixel pair																							
1 st SPI data byte: MSByte							2 nd SPI data byte							3 rd SPI data byte: LSByte									
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PIXEL_EVEN[11:4]							PIXEL_EVEN[3:0]			PIXEL_ODD[3:0]				PIXEL_ODD[11:4]									

Table 64: Pixel data SPI readout: Pixel pair read; refer to Figure 46

	1 st pair read / row	2 nd pair read / row
1 st row read	Pixels row 2 / column 0 & 2	Pixels row 2 / column 4 & 6
2 nd row read	Pixels row 4 / column 0 & 2	Pixels row 4 / column 4 & 6
3 rd row read	Pixels row 0 / column 0 & 2	Pixels row 0 / column 4 & 6
4 th row read	Pixels row 6 / column 0 & 2	Pixels row 6 / column 4 & 6

Table 65: Pixel-field SPI double-row readout order; refer to Figure 46, based on even pixel-field coordinates Figure 45

Validity parameter	Embedded data ¹	Data bit
Pixel saturation	0x 07 FF	Read register P2[0x0D] and P2[0x0E] ²
ADC overflow	0x 07 FE	Read register P2[0x10] and P2[0x11] ²
ADC underflow	0x 08 00	Read register P2[0x12] and P2[0x13] ²
Valid pixel data	0x 08 01 < ... < 0x 07 FD	[11:0]

Table 66: Data validity table

Note 1: Default is embedded data format. Can be switched off by bit 6 of the register P4[0x15].

Note 2: More details can be found in the corresponding register description.

Action	Command	MOSI	MISO	Page	Reg	Value	Comment
Power up	NOP	0x 00 00	0x ...				After startup
	- repeat until:						
	NOP	0x 00 00	0x 00 00				IDLE; ready for communication
	- load sequencer program						
Adjust default settings 1	Page select	0x 81 00	0x 00 00	1			Page 1
(all chip versions)	Adjust 1	0x 5A 00	0x 81 00	1	0x1A	0x00	
	Page select	0x 85 00	0x 5A 00	5			Page 5
	Adjust 2	0x 4B 00	0x 85 00	5	0x0B	0x00	
	NOP	0x 00 00	0x 4B 00				optional
Adjust default settings 2	Page select	0x 84 00	0x 00 00	4			Page 4
(only for WAFER ID <13)	Adjust 3	0x 48 1F	0x 84 00	4	0x08	0x1F	
	Page select	0x 85 00	0x 48 1F	5			Page 5
	Adjust 4	0x 4E 01	0x 85 00	5	0x0E	0x01	
	Page select	0x 86 00	0x 4E 01	6			Page 6
	Adjust 5	0x51 62	0x 86 00	6	0x11	0x62	
	NOP	0x 00 00	0x51 62				optional
Set mode	Page select	0x 84 00	0x 00 00	4			Page 4
	Set modulation selection	0x 52 C0	0x 84 00	4	0x12	0xC0	
	Set GBI mode	0x 55 37	0x 52 C0	4	0x15	0x37	Set 4x4 pixel Grayscale Binned pixel Imager mode
	NOP	0x 00 00	0x 55 37				optional
Set modulation frequency	Page select	0x 84 00	0x 00 00	4			optional, because page 4 is already selected
Sets integration time base	Set mod. freq. to 10MHz	0x 45 01	0x 84 00	4	0x05	0x01	Is also integration time base
	NOP	0x 00 00	0x 45 01				optional
Set integration time	Page select	0x 85 00	0x 00 00	5			Page 5
	Set int. time 1.6384ms	0x 40 00	0x 85 00	5	0x00	0x00	Integration time multiplier, high byte
		0x 41 01	0x 40 00	5	0x01	0x01	Integration time multiplier, low byte (lowest number = 1)
		0x 42 FF	0x 41 01	5	0x02	0xFF	Integration length, high byte
		0x 43 FF	0x 42 FF	5	0x03	0xFF	Integration length, low byte
	NOP	0x 00 00	0x 43 FF				optional
Start measurement	Page select	0x 82 00	0x 00 00	2			Page 2
	Set TRIGGER	0x 58 01	0x 82 00	2	0x18	0x01	Starts measurement
	NOP	0x 00 00	0x 58 01				optional
Read frame DCSx							
Read row	- repeat for 2 double-rows per frame:						
	Page select	0x 82 00	0x 00 00	2			optional, because page 2 is already selected
	Read STATUS	0x 35 00	0x 82 00	2	0x15		
	- repeat until DATA_RDY:						
	Read STATUS	0x 35 00	0x 35 00	2	0x15		Wait for end of exposure. Refer to imaging timing
	NOP	0x 00 00	0x 35 8C				Data ready – or alternatively DATA_RDY pin
	12 bytes available for readout = readout of a double-row						
	READ data 1	0x 2C 00	0x 00 00	2	0x0C		Readout double-row, uses embedded data format
	READ data 2	0x 2C 00	0x 2C ..	2	0x0C		MSByte0 (Row 1, pixel 0)
	READ data 3	0x 2C 00	0x 2C ..	2	0x0C		LSNibble0 LSNibble1
	READ data 4	0x 2C 00	0x 2C ..	2	0x0C		MSByte1 (Row 1, pixel 1)
	READ data 5	0x 2C 00	0x 2C ..	2	0x0C		MSByte2 (Row 1, pixel 2)

	READ data 10	0x 2C 00	0x 2C ..	2	0x0C		MSByte5 (Row 2, pixel 1)
	READ data 11	0x 2C 00	0x 2C ..	2	0x0C		MSByte6 (Row 2, pixel 2)
READ data 12	0x 2C 00	0x 2C ..	2	0x0C		LSNibble6 LSNibble7	
NOP	0x 00 00	0x 2C ..				MSByte7 (Row 2, pixel 3)	
Next row	- repeat "Read row" for next double-row						
End measurement							

Table 67: Basic example of GBI mode

7.3.3. Alternative grayscale modes

Beside the before listed two grayscale modes, for enhanced applications, it is possible to switch all listed TOF modes into grayscale functionality with the corresponding output data format:

1. Select the required TOF mode, e.g. ULN.
2. Read register P4[0x12] and store the value as "TOF settings".
3. Afterwards, switch in the DCS mode selection register P4[0x12] the designated bits from TOF to grayscale mode:
 - bit 4 and 5 = 0: Select grayscale
 - bit 6 and 7 = 11: Select grayscale
4. The chip runs now in the equivalent grayscale mode, if a SHUTTER applies.
5. The grayscale data readout follows the same rules as for the corresponding TOF mode.
6. SHUTTER applies only for 1 integration time (1x DCS or grayscale).
7. Switch back to TOF mode
Reload the register P4[0x12] with the value "TOF settings".

7.4. Imaging timing and frame rates

The 8x8 pixel TIM mode is used as per datasheet unless otherwise stated for simplifying the documentation. The settings used are: SPI clock 16 MHz, single measurement control, basic data readout, including 2x reading DATA_RDY, without reading validity or quality data.

The sequence of how images are acquired and read out is shown in the Figure 47 and Figure 48.

Note: Depending on the selected mode, data readout by SPI takes place in parallel to the next double-row conversion.

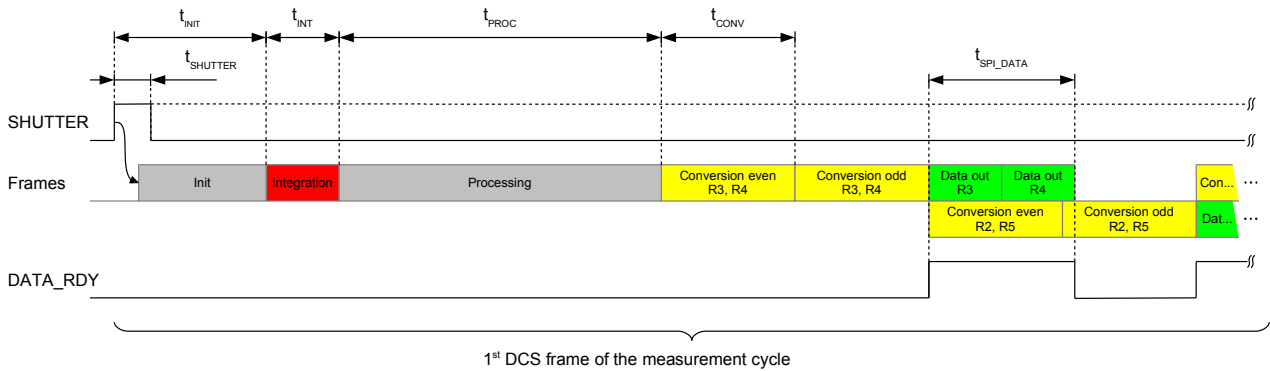


Figure 47: Frame timing: Start

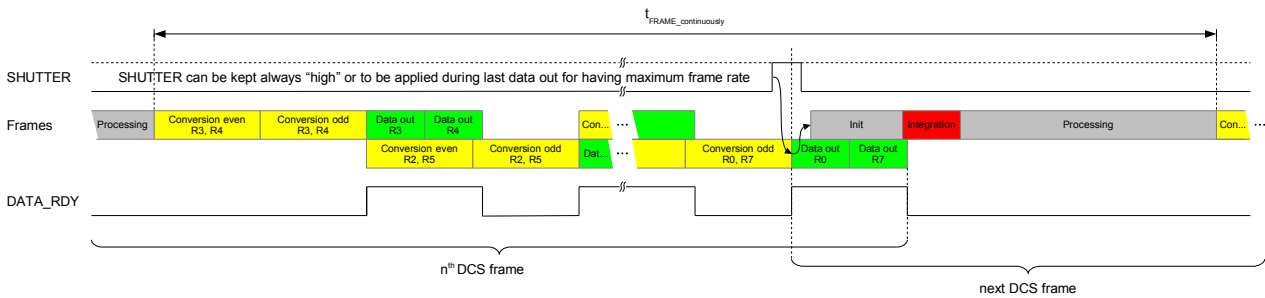


Figure 48: Frame timing: Inter-frame, end-of-frame and start-next-frame

Symbol	Parameter	Typ.	Units
$t_{SHUTTER}$	SHUTTER is auto-cleared after propagation by SPI	---	ns
t_{INIT}	Init: Delay from the rising edge of SHUTTER signal to the 1 st LED pulse	18	μ s
t_{INT}	Image acquisition (integration time)	---	
t_{PROC}	Delay from the last LED pulse until the 1 st row conversion	38.75	μ s
t_{CONV}	Conversion time of a half row (even or odd columns) for a pixel pair (rows from top and bottom half of pixel-field)	15.625	μ s
t_{DATA_RDY}	Valid data available for readout by SPI e.g for SPI clock 16MHz, 2x 8pixel with 12bit incl. 2x read DATA_RDY	26	μ s

Table 68: Frame timing parameters

Ab-brev.	Description	SPI:	Chip:	Chip:	Chip:	SPI:	S + C:	Read	Exp.:	Frame:	Frame rate [fps]			Features		
		t _{SHUTTER} [μs]	t _{INIT} [μs]	t _{PROC} [μs]	t _{CONV_TOT} [μs]	t _{LAST_DATA} [μs]	t _{PROC_TOT} [μs]	out [Bit]	t _{INT} [μs]	t _{FRAME} [μs]	1 DCS rolling	2 DCS	4 DCS	Bin	Sum	Int. times
TIM	8x8 pixel 3D TOF imager	1.00	18.00	38.75	125.00	26.00	209	12	50	258.8	3'865	1'932	966	---	---	1
ULN	Ultra low noise range-finder	1.00	18.00	38.75	125.00	5.00	188	18	50	237.8	4'206	2'103	1'052	---	64 p	1
UFS	Ultra fast & sens. range-finder	1.00	18.00	38.75	15.63	4.00	77	14	50	127.4	7'851	3'925	1'963	4 p	4 p	1
UHD	Ultra HDR range-finder	1.00	18.00	38.75	125.00	6.00	189	15	50	238.8	4'188	2'094	1'047	---	8 p	max. 8
LNH	Low noise HDR range-finder	1.00	18.00	38.75	31.25	6.00	95	14	50	145.0	6'897	3'448	1'724	4 p	4 p	max. 4
RBH	Red. blur HDR range-finder	1.00	18.00	38.75	31.25	14.00	103	12	50	153.0		6'536	3'268	4 p	---	max. 2
NBF	No motion-blur range-finder	1.00	18.00	38.75	125.00	6.00	189	15	50	238.8			4'188	---	8 p	1
GIM	8x8 pixel grayscale imager	1.00	18.00	38.75	125.00	26.00	209	12	50	258.8	3'865			---	---	1
GBI	4x4 pixel grayscale imager	1.00	18.00	38.75	31.25	14.00	103	12	50	153.0	6'536			4 p	---	1

Table 69: Overview of max. frame rates per mode with **same integration time** (single measurement control, data readout only)

Ab-brev.	Description	SPI:	Chip:	Chip:	Chip:	SPI:	S + C:	Read	Exp.:	Frame:	Frame rate [fps]			Features		
		t _{SHUTTER} [μs]	t _{INIT} [μs]	t _{PROC} [μs]	t _{CONV_TOT} [μs]	t _{LAST_DATA} [μs]	t _{PROC_TOT} [μs]	out [Bit]	t _{INT} [μs]	t _{FRAME} [μs]	1 DCS rolling	2 DCS	4 DCS	Bin	Sum	Int. times
TIM	8x8 pixel 3D TOF imager	1.00	18.00	38.75	125.00	26.00	209	12	64	272.8	3'666	1'833	917	---	---	1
ULN	Ultra low noise range-finder	1.00	18.00	38.75	125.00	5.00	188	18	1	188.8	5'298	2'649	1'325	---	64 p	1
UFS	Ultra fast & sens. range-finder	1.00	18.00	38.75	15.63	4.00	77	14	4	81.4	12'289	6'144	3'072	4 p	4 p	1
UHD	Ultra HDR range-finder	1.00	18.00	38.75	125.00	6.00	189	15	8	196.8	5'083	2'541	1'271	---	8 p	max. 8
LNH	Low noise HDR range-finder	1.00	18.00	38.75	31.25	6.00	95	14	4	99.0	10'101	5'051	2'525	4 p	4 p	max. 4
RBH	Red. blur HDR range-finder	1.00	18.00	38.75	31.25	14.00	103	12	16	119.0		8'403	4'202	4 p	---	max. 2
NBF	No motion-blur range-finder	1.00	18.00	38.75	125.00	6.00	189	15	4	192.8			5'188	---	8 p	1
GIM	8x8 pixel grayscale imager	1.00	18.00	38.75	125.00	26.00	209	12	64	272.8	3'666			---	---	1
GBI	4x4 pixel grayscale imager	1.00	18.00	38.75	31.25	14.00	103	12	16	119.0	8'403			4 p	---	1

Table 70: Overview of max. frame rates **to achieve the equal distance noise (TOF amplitude) with same emitting illumination power for all modes** (single measurement control, data readout only)

7.4.1. Single measurement control

The selected measurement mode (4x DCS, 2x DCS, grayscale, ...) defines how many frames the chip performs by the stimulation of one SHUTTER (register. P2[0x18], bit 0) in one measurement cycle. The SHUTTER is auto-cleared after propagation. During the measurement cycle, the next frame acquisition starts immediately after last data readout on the SPI interface until all frames are performed.

7.4.2. Continuous measurement control (auto-run)

The epc611 runs in non-stop measurement mode as long as the shutter control register P2[0x18], bit 1 is set or the SHUTTER is applied during the readout of the last row pair of the last frame. The chip starts immediately next measurement cycle if the actual one is terminated (Figure 51). Trigger signals not active during the readout of the last row pair of the last frame are ignored.

7.5. Integration time setting

The integration time is the active frame acquisition period (see Figure 47).

- The integration time, illumination intensity and object reflectivity define the effective distance achievable which the complete camera system can see.
- In applications with moving objects or cameras, this time should be kept very short to reduce motion-blur effects as much as possible.
- Short integration times e.g. < 1 ms also reduce effects of signal distortion such as ambient-light, dark current, etc. and can simplify the compensation.

The integration time setting depends on the operating mode: single or multiple integration times per frame.

7.5.1. Single integration time per frame

The values of the integration length P5[0x02], P5[0x03], integration length multiplier P5[0x00], P5[0x01] and f_{mod_clk} (register P4[0x05]) define the integration time. Whereas using on-chip modulation clock, f_{mod_clk} sets the time-base, integration length is the integration time counter and the integration length multiplier defines the number of repetition cycles.

$$\text{Integration time} = \text{integration length multiplier} * (\text{Integration length} + 1) * (1 / f_{mod_clk})$$

Boundaries:

- The integration length multiplier should be kept as low as possible. Valid range = 1 ... 1'023d.
- Integration length + 1 should be evenly divisible by 4. Valid range = 7 ... 65'535d.

Table 72 lists some useful integration time settings.

Integration time	Integration length multiplier P5[0x00], P5[0x01]		Integration length P5[0x02], P5[0x03]	
	[DEC]	[HEX]	[DEC]	[HEX]
1.60 μs	1d	0x0001	63d	0x003F
12.8 μs	1d	0x0001	511d	0x01FF
102.4 μs	1d	0x0001	4'095d	0x0FFF
819.20 μs	1d	0x0001	32'767d	0x7FFF
1.6384 ms	1d	0x0001	65'535d	0xFFFF

Table 71: Typical TOF and grayscale integration times for 10MHz on-chip modulation frequency (modulation clock = 40MHz)

7.5.2. Multiple integration times per frame

Operation modes with multiple integration times use the registers integration length rows P7[0x00] ... P7[0x0F] instead of the integration length.

$$\text{Integration time} = \text{integration length multiplier} * (\text{integration length row} + 1) * (1 / f_{\text{mod_clk}})$$

Additional boundaries:

- The integration length multiplier is active for all integration length row registers.
- Integration length row + 1 should be evenly divisible by 4. Valid range = 7 ... 65'535d.
- Integration length row(X) integration length row(X+1),
e.g integration length row0 integration length row1 integration length row2, etc. ...
- Each of the 8 integration length row registers must be set according to the definition given in the operating mode being used.

Input data

Parameter	Unit	Value
Time base setting		
LED mod. frequency	MHz	10.0

Amplitude normalized to 20μm pixel		
Min. TOF amplitude	LSB	800
Max. TOF amplitude	LSB	2'000
Target for longest integration time		
Integration time for - min. TOF amplitude - furthest object - lowest reflectivity - preferred < 1'000μs	μs	1'000

Result of system parameters

Parameter	Unit	Value
Modulation clock	MHz	40.0
Mod. clock period	ns	25.0
Unambiguity range	m	15.0
TOF amplitude ratio	1:	2.5
	dB	8.0
Max. int. time counter	#	40'000

Result of integration times and register parameters

Multiplier	Counter	Final integration time		Register values		Registers used in operating mode:			
		μs	Ratio	Dec	Hex	others	UHD	LNH	RBH
Register address						P5[0x00], P5[0x01]	P5[0x00], P5[0x01]	P5[0x00], P5[0x01]	P5[0x00], P5[0x01]
Repetition counts	1			1	0001	Int. length multiplier	Int. length multiplier	Int. length multiplier	Int. length multiplier
Int. length	Counter	μs	Ratio	Dec	Hex				
Register address						P5[0x02], P5[0x03]	P7[0x00] – P7[0x0F]	P7[0x00] – P7[0x0F]	P7[0x00] – P7[0x0F]
Int. time 1 (max.)	40'000	1'000.0		39'999	9C3F	Integration length	Int_len_row7	Int_len_row7, 6	Int_len_row7 ...4
Int. time 2	16'000	400.0	2.50	15'999	3E7F		Int_len_row6	Int_len_row5, 4	Int_len_row3 ...0
Int. time 3	6'400	160.0	2.50	6'399	18FF		Int_len_row5	Int_len_row3, 2	
Int. time 4	2'560	64.0	2.50	2'559	09FF		Int_len_row4	Int_len_row1, 0	
Int. time 5	1'024	25.6	2.50	1'023	03FF		Int_len_row3		
Int. time 6	408	10.2	2.51	407	0197		Int_len_row2		
Int. time 7	160	4.0	2.55	159	009F		Int_len_row1		
Int. time 8	64	1.6	2.50	63	003F		Int_len_row0		

Table 72: Example of integration time settings with on-chip modulation clock

7.6. Distance measurement (3D TOF)

The epc611's default modulation mode is based on the sinusoidal TOF modulation theory, but effectively uses a square-wave modulated signal with a duty-cycle of 50% for the illumination. After reset, all internal register values are default set to operate the chip at 4MHz XTAL/external clock input, multiplied up to 40 MHz at the PLL output, clocks the modulator with 40 MHz modulation clock (mod_clk), modulates LED/LD with 10 MHz and acquires 4 successive DCS frames (0 ... 3) using 51.2 μs integration time.

The distance measurement mode uses the on-chip LED driver and the external IR-LED/LD to provide modulated light on the target. Modulation control signals to the LED driver are provided by a programmable modulator. The modulator generates all signals to modulate the external IR-LED/LD and all demodulation signals to the pixel-field simultaneously. TOF and grayscale mode with all the variants are generated here.

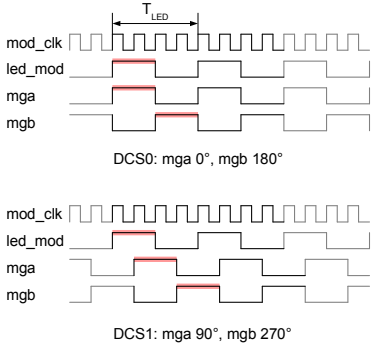


Figure 49: 4 DCSx modulation/demodulation waveforms

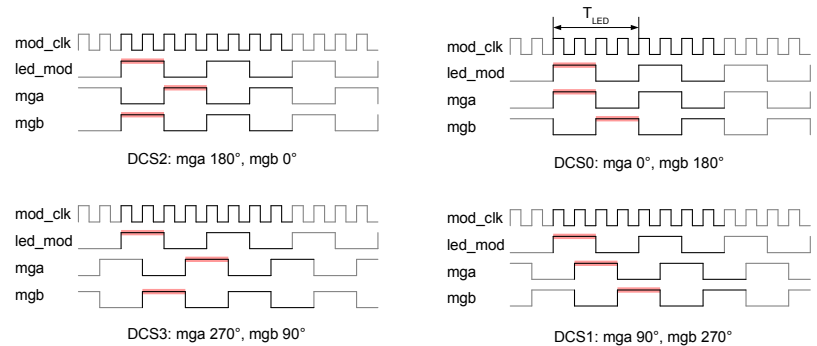


Figure 50: 2 DCSx mod./demod. waveforms

The modulation table registers control the modulation (refer to Table 87). The registers can be updated via SPI interface between frame acquisitions. The application must ensure that the last frame's integration phase is completed before modifying on-the-fly these registers. This time can be detected by the application by waiting for the DATA_RDY signal. This procedure allows to run continuously the maximum frame rate.

With the application of the SHUTTER via SPI, the chip performs the required number of successive DCS acquisitions. Each one of the 4 DCS frame types has a different phase relation between modulation (led_mod) and demodulation (mga, mgb) signals which makes phase-to-distance calculation possible. In the case of DCS0, led_mod is phase-shifted by 0° and 180° with respect to mga and mgb, respectively. In the case of DCS1, led_mod is phase-shifted by 90° and 270°. For DCS2, the phase-shifts are 180° and 0° and for DCS3, the phase-shifts are 270° and 90° (see Figure 49). Note that for DCS2 and DCS3, the demodulation signals mga and mgb are simply swapped with respect to DCS0 and DCS1 respectively.

By programming the “Number of DCS readouts” for 2x DCS (see register P4[0x12]), SHUTTER initiates 2 successive DCS frame acquisitions (see Figure 50). This mode allows distance acquisition by using two DCSs only and thus a doubled frame rate. However, this results at the cost of a lower distance measurement accuracy and a 40% higher distance noise.

7.7. Distance calculation algorithm

The use of the trigonometric atan2 definition for vectors (x, y) in the Cartesian coordinate system $\phi = \text{atan2}(x, y) = \text{atan2}(y/x)$ guarantees a continuous distance calculation algorithm in the range of phases between $-\pi \dots +\pi$. The TOF system uses the range from 0°... 360° which corresponds to the distance from 0m up to the unambiguity distance (refer to Figure 51 and Figure 52).

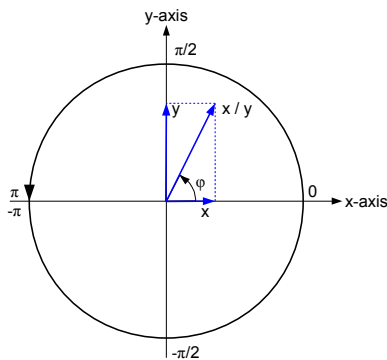


Figure 51: Continuous atan2 representation for the range $-\pi \dots +\pi$

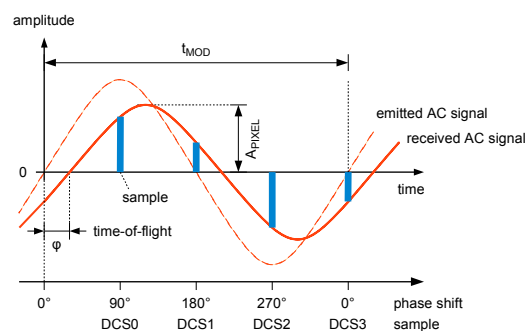


Figure 52: Sampling of the received waveform

In general, the distance is calculated by using the 4 DCSs, also called π -delay matching, which cancels pixels offsets leading to distance errors:

$$[1] \quad D_{\text{TOF}} [\text{m}] = \frac{c}{2} \cdot \frac{1}{2\pi f_{\text{LED}}} \cdot \left[\pi + \text{atan2} \left(\frac{\text{DCS3} - \text{DCS1}}{\text{DCS2} - \text{DCS0}} \right) \right] + D_{\text{OFFSET}}$$

The measured data is always valid over the 360° phase-shift. Due to the distance offset adjustment D_{OFFSET} , the correction of the distance roll-over effect at zero and unambiguity distance is necessary to ensure all the time correct distance values D :

- if $D_{\text{TOF}} > D_{\text{Unambiguity}}$: $D = D_{\text{TOF}} - D_{\text{Unambiguity}}$
- if $D_{\text{TOF}} < 0$: $D = D_{\text{TOF}} + D_{\text{Unambiguity}}$
- else: $D = D_{\text{TOF}}$

If greater distance errors can be tolerated but a high frame rate is needed, the distance calculation also works with only 2 DCSs:

$$[2] \quad D_{\text{TOF}} [\text{m}] = \frac{c}{2} \cdot \frac{1}{2\pi f_{\text{LED}}} \cdot \left[\pi + \text{atan2} \left(\frac{-\text{DCS1}}{-\text{DCS0}} \right) \right]$$

The following terms are used in the formulas above:

D_{TOF}	Distance in meters [m]
c	Speed of light (299'792'458 m/s)
f_{LED}	LED/LD modulation frequency e.g. 10 MHz
$\text{DCS0} - \text{DCS3}$	Sampling values [LSB]
φ	Phase-shift caused by the time-of-flight [rad]
D_{OFFSET}	Offset compensation [m]
$D_{\text{Unambiguity}}$	Unambiguity distance [m]

7.8. Unambiguity range versus time base setting

Due to continuous modulation, roll-over can be observed if the distance to the object is longer than the length of one modulation cycle (one period, 2π). This roll-over distance is called the unambiguity range and can be calculated as follows:

$$[3] \quad D_{\text{Unambiguity}} [\text{m}] = \frac{c}{2} \cdot \frac{1}{f_{\text{LED}}}$$

The effective operating range is the maximum distance corresponding to the maximum time-of-flight within one cycle of the modulation being used: It is one period of f_{LED} . Objects inside this area are detected unambiguously.

The unambiguity range defines the repetition distance. Objects outside of the effective operating range can still be detected if they are of very high reflectivity (remission). As a result, strongly reflected signals coming from outside of this range may interfere with the measurement.

The operating range, the unambiguity distance, the time base for the integration time and the resolution of the distance signal are defined by the modulation clock mod_clk . For the epc611, this corresponds to a maximum default operating range of 7.5m @ $\text{mod_clk} = 80\text{MHz}$. Depending on the application, it may be necessary to adapt these parameters to other values. It can be done by a change of the modulation clock. Table 73 lists as an example some values of the modulation clocks in function of the operating ranges, the unambiguity distances, of the distance resolutions and of the multipliers of the integration time base.

Unambiguity distance	Integration time multiplied by	Distance resolution ²	Modulation clock	Modulation clock divider	LED modulation frequency
			f_{MOD}	Register P4[0x05]	f_{LED}
[m]	[#]	[cm]	[MHz]	[#]	[MHz]
7.5	1	0.25	80	0	20
15 ¹	2 ¹	0.50	40	1 ¹	10
30	4	1.00	20	3	5
60	8	2.00	10	7	2.5
120	16	4.00	5	15	1.25

Table 73: Unambiguity range versus on-chip modulation clock

Notes:

- ¹ Default values
- ² This example is based on a user's distance scaling for the unambiguity distance (phase angle 2 Pi) corresponding to 3'000 LSB, e.g. @ 10 MHz correspond 3'000 LSB to 15 m unambiguity distance. User should choose the appropriate scaling for his application depending of the operation mode.
- ³ Using external modulation clock EXTMOD: Follow Chapter 6.5.2.

7.9. Quality of the measurement

The DCS values contain not only the distance information but also the quality and the validity (confidence level) of the received optical signal. The higher the signal amplitude of the received signal, the better and more precise the distance measurement. Each distance measurement of every pixel has its own validity and quality.

The primary quality indicator for the measured distance data is the amplitude of the received modulated light A_{TOF} . The amplitude is in direct relationship to the distance noise (refer to the corresponding graph of the operation mode e.g. Figure 28). The amplitude can be calculated as follows:

$$[4] \quad A_{\text{TOF}} = \frac{\sqrt{(\text{DCS2} - \text{DCS0})^2 + (\text{DCS3} - \text{DCS1})^2}}{2}$$

Amplitude A_{TOF}	Classification	Action
< 1 %	Weak illumination	Objects can be detected but distance measurement is not possible. Increase the integration time for the next measurement.
1 ... 5 %	Useful amplitude for measurement	High distance noise, increase the integration time
5 ... 99 %	Good signal strength	No action necessary
> 99%	Overexposed	Decrease integration time for the next measurement.

Table 74: Signal amplitude versus classification

Note:

The amplitude value is the feedback parameter that is used to set the integration time for the next measurement. Generally, the higher the received signal, the better and more precise the distance measurement. However, it is good practice to control the integration time so that an amplitude value between 10 ... 75% is achieved. Higher values will only slow down the acquisition rate due to longer integration times, but do not significantly improve signal-to-noise ratio.

The quality indicator for the distance noise is the ratio of ambient-light E_{BW} to the peak-to-peak value of modulated light E_{TOF} (AMR). This value may be calculated and used additionally to the above amplitude value if the respective application is subject to intense ambient-light. The peak-to-peak irradiance E_{TOF} of the modulated signal at the surface of a pixel can be calculated using the AC sensitivity S_{TOF} , the integration time $t_{INT-TOF}$ used, the reference integration time $t_{INT-REF-TOF}$ and the peak-to-peak amplitude A_{TOF} of the received modulated signal in the following way:

$$[5] \quad E_{TOF} = S_{TOF} \cdot \frac{t_{INT-REF-TOF}}{t_{INT-TOF}} \cdot A_{TOF} \quad \text{e.g.} \quad E_{TOF} = 0.60 \frac{\text{nW/mm}^2}{\text{LSB}} \cdot \frac{100 \mu\text{s}}{250 \mu\text{s}} \cdot 1'000 \text{ LSB} = 0.24 \mu\text{W/mm}^2$$

The formula to calculate the "Ratio of Ambient-light / Modulated light" (AMR) quality indicator is:

$$[6] \quad \text{AMR}[\text{dB}] = 20 \cdot \log\left(\frac{E_{BW}}{E_{TOF}}\right) \quad \text{e.g.} \quad \text{AMR}[\text{dB}] = 20 \cdot \log\left(\frac{15.6 \mu\text{W/mm}^2}{0.24 \mu\text{W/mm}^2}\right) = 36\text{dB}$$

To obtain the E_{BW} , please refer to Chapter 7.10. Grayscale imaging / ambient-light measurement. This ratio is one of the influencing factors regarding the distance noise.

AMR value	Classification	Action
< 60 dB	excellent	No action necessary.
< 70 dB	sufficient	If a lower noise level is needed, perform the next measurement with a shorter integration time or with an increased illumination power.
> 70 dB	weak	Perform the next measurement with a shorter integration time or with an increased illumination power.

Table 75: Classification ratio ambient-light to modulated light (AMR) versus distance noise

There are also validity indicators delivered by the chip following a measurement. These will help to detect saturated or non-illuminated pixels as a result of too much/little illumination or too long/short integration time.

Table 76 shows a quality decision matrix as a summary of the validity and quality parameters for the distance measurement.

Step	Indicator	Pixel saturation: too much amb.-light or too bright illu.	Too bright illumination	No object detected	Too much ambient-light	Object detected
1	SAT flag	Set				
2	DCSx		> +99% or < -99%	all of them -1% ... +1%		
3	TOF amplitude		> 99%	< 1%		5% ... 99%
4	AMR: Ratio amb. to mod. light				> 70 dB	< 60 dB
5	Action	Decrease int. time	Decrease int. time	Increase int. time	Decrease int. time	Use distance data

Table 76: Validity (V) and quality (Q) decision matrix (see also Figure 53)

Accurate and reliable distance information can only be provided if the validity and the necessary quality levels of the measured data are given. The generic validity and quality of the data is independent of any correction or compensation algorithms. It is only based on the complete epc611 camera system with chip, lens, illumination and environmental conditions.

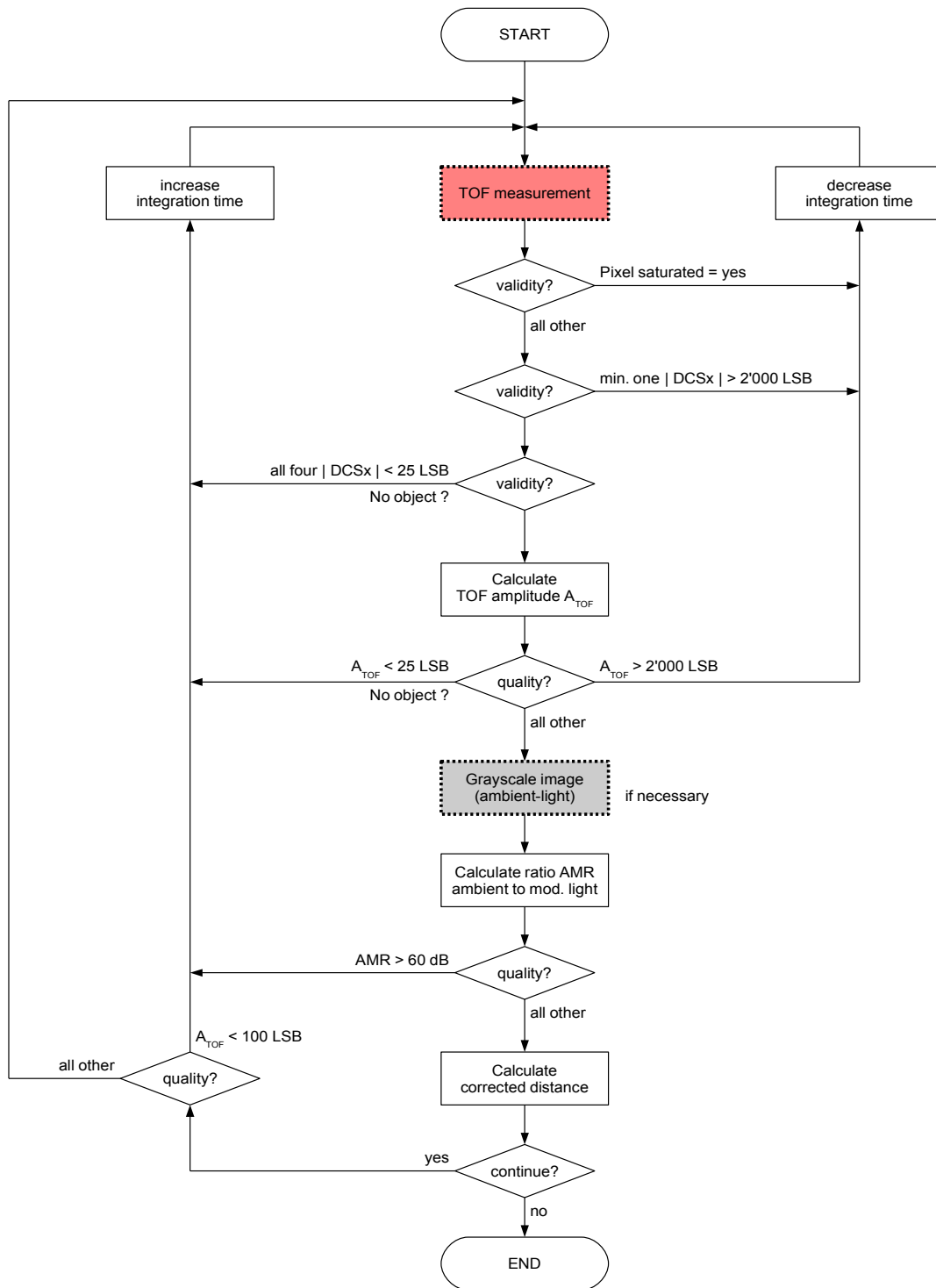


Figure 53: Generic validity and quality flow chart for a single pixel

For possible correction and compensation algorithms, refer to the AN 10 Application Note which is available on the Website www.espros.com.

7.10. Grayscale imaging / ambient-light measurement

The grayscale mode allows the use of the epc611 as a grayscale imager. This mode can be used either without LED/LD illumination for ambient-light measurements or with LED/LD for active illumination of the scenery. The grayscale measurement uses regular DCS measurement but with DCS0 only. It is performed with differential readout using MGA only (refer to Figure 20) which remains on during the entire integration time. Data output format is signed integer 12 bit: $\pm 2'047$ LSB. Effective data range is 0 ... $+2'047$ LSB. Due to system noise around zero, the readout can show small negative numbers.

The saturation flag status is invalid in this mode.

Due to the fact that distance measurement results can be influenced by ambient-light, the grayscale measurement without illumination can thereof be used as an important quality and correction parameter for the distance measurement.

The irradiance E_{BW} of the grayscale signal at the surface of a pixel can be calculated from the DC sensitivity S_{BW} , the used integration time t_{INT-BW} , the reference integration time $t_{INT-REF-BW}$ and the amplitude of DCS0 of the grayscale signal as follows:

$$[7] \quad E_{BW} = S_{BW} \cdot \frac{t_{INT-REF-BW}}{t_{INT-BW}} \cdot DCS0 \quad \text{e.g.} \quad E_{BW} = 0.25 \frac{\text{nW/mm}^2}{\text{LSB}} \cdot \frac{100 \mu\text{s}}{1.6 \mu\text{s}} \cdot 1'000 \text{ LSB} = 15.6 \mu\text{W/mm}^2$$

7.11. Calibration and compensation of TOF cameras

This modern TOF sensor chip offers a fully digital interface to the control circuitry of a TOF camera. First-time users naturally expect straight forward implementation and digital accuracy of the measured signals. However, often tremendous disillusion follows because many physical effects are influencing the final performance of 3D TOF cameras.

3D TOF cameras capture images by utilizing the time-of-flight measurement of photons. Photons are emitted by high frequency modulated LEDs or laserdiodes, which are part of the camera. These are then scattered by objects in the scenery, before and finally, some of the emitted photons are reflected back to the camera and captured in so-called demodulation pixels. This time-of-flight happens in an incredibly short period of time, as it takes place with 300'000 km/s or 30 cm/ns. To achieve a centimeter distance resolution and accuracy, 30 ps time measurement accuracy has to be achieved. This is a very tough requirement, as may be a lot of pixels need to provide such accurate measurement several dozen times per second at the same time. Small and inherent differences in the connection and arrangement of transistors within the TOF chip, temperature differences and changes, as well as irradiance signal strength and, last but not least, ambient-light change lead to measurement errors in the tens of centimeters:

---> Calibration and compensation is essential to reach the goal.

To support users, AN10 "Calibration and Compensation" Application Note can be downloaded from the Website www.espros.com in the section Downloads. This paper describes the error sources in 3D TOF sensor chips, a simple way to implement a calibration procedure and how to compensate them at camera level.

Other documents which can be helpful to achieve a successful chip implementation are listed in Chapter 14.2, Related documents.

7.12. Noise reduction and signal filtering

Regardless of which measurement process applies, distance noise is one of the major challenging factors of 3D TOF imaging. This limits to distinguish the depth of small objects or fine contours. It is called temporal noise and varies from measurement to measurement. Since this noise is a statistical value, its effect can be reduced by filtering.

However, a simple averaging with a FIR filter is not suitable for many applications because of the very long time lag to get a filtered result. Using filtering based on the theory of Rudolf E. Kalman, noise can be reduced significantly without losing system responsivity. Figure 54 shows the resulting effect of such a Kalman filter.

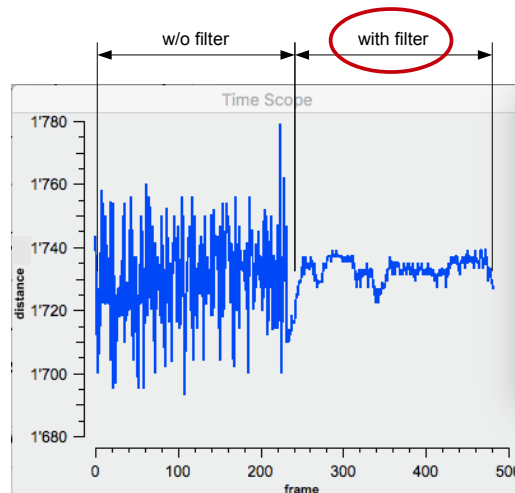


Figure 54: Effect of the static Kalman filter on distance noise (Distance in mm)

Left side: The frames 0 to 240 have been acquired without filtering at all. The distance noise is approx. 12 cmpp (1 sigma = 2.5 cm). Right side: Frames 240 to 500 are processed with the Kalman filter. The distance noise is reduced to approx. 2 cmpp (1 sigma = 0.5 cm). The signal amplitude was quite low in both cases, approx. 250 LSB.

To support users, AN12 "TOF data improvement toolbox" Application Note can be downloaded from the Website www.espros.com in the section Downloads. This paper describes background and implementation of two Kalman filter algorithms in 3D TOF cameras.

8. Temperature sensor

The temperature sensor is located near the pixel-field. It is factory-calibrated at 27°C (offset). The temperature value can be accessed in registers P2[0x0A] and P2[0x0B] after taking the following “temperature/grayscale image” for temperature reading. The procedure described below takes a grayscale image with 2.5 times lower sensitivity compared to the regular grayscale modes described in Chapters 7.3.1., 7.3.2. and 7.10.. Most applications need grayscale (or ambient-light) pictures for background-light compensation. By reading the temperature, a grayscale image can be read at the same time.

The temperature register is cleared on the beginning of each frame. To ensure correct values, read the register after applying the necessary double-row read cycles depending on the operation mode according Table 77.

Mode	Min. waiting time	Reading value	Accuracy
	Double-row read cycles per frame	Register P2[0x0A], P2[0x0B]	
UFS	1	Temperature /4	No offset compensation
LNH, RBH, GBI	2	Temperature /2	Partly offset compensated
all others	4	Temperature (14 bit)	Most accurate

Table 77: Waiting time and data output for the temperature reading versus operating modes

8.1. Initialization

Upon power-up or after a RESET:

```
define X, Y, M, C, Z,           # Define required variables
    TH, TL, Temp               # Define required variables, only for temperature reading

X = RD @P6[0x13]              # Save register 0xD3
Y = RD @P6[0x15]              # Save register 0xD5

C = RD @P6[0x19]              # Read sensor factory calibration
Z = C/4.7-0x12B               # Normalized calibration value for temperature formula
```

The calibration value (factory setting) is stored in the EEPROM of the chip. If it is accidentally overwritten, it can be reloaded by applying a reset or a power-up.

8.2. Read-out during runtime

1. Set the integration time for the grayscale imaging the regular way. Note: The sensitivity is 2.5 times lower than in the regular grayscale mode.
2. Acquire a grayscale image, perform the temperature readout and the temperature calculation. The grayscale image will be acquired with the following procedure and stores the temperature value into the registers P2[0x0A] and P2[0x0B] .

```
M = RD @P4[0x12]              # Save mode register, control no. of DCS

WR @P6[0x13] = X OR 0x60      # Set bits b5 and b6
WR @P6[0x15] = Y AND 0x0F     # Clear bits b4 and b5

# Image acquisition
WR @P4[0x12] = 0xC0           # Change mode to grayscale
WR @P2[0x18] = 0x01           # Trigger image acquisition

# After data readout
TH = RD @P2[0x0A]             # Read temperature sensor high register
                                # Refer to Table 76, "all others - most accurate"
TL = RD @P2[0x0B]             # Read temperature sensor low register
                                # Refer to Table 76, "all others - most accurate"

# Switch back to normal image acquisition...
WR @P6[0x13] = X              # Restore register 0xD3
WR @P6[0x15] = Y              # Restore register 0xD5
WR @P4[0x12] = M              # Change back to the mode before temperature reading
```

8.3. Calculating temperature in °C

```
Temp = ((TH*0x0100+TL)/4-0x2000)*0.134+Z # Refer to Table 77, "all others - most accurate"
```

Note:

The acquired grayscale image of the temperature/grayscale image can be used. However, the sensitivity during this acquisition was reduced by a factor of 2.5. Thus, if the same sensitivity is needed, the integration time has to be increased by a multiplier of 2.5.

If the temperature reading used for compensation purposes, it is recommended to apply the following temporal filtering algorithm. This prevents the compensation of additional noise caused by the temperature reading noise (digitalization, quantization errors and system noise).

```
k = 0.1 # Kalman gain
y[i-1] = x[0] # Start condition

x[i] = Temp
y[i]=k*x[i]+(1-k)*y[i-1] # Simple Kalman 1 filter
```

x[i]: Current temperature

y[i]: Current temporal filtered temperature

y[i-1]: Previous temporal filtered temperature

9. Application information

To help users to better understand the chip, this chapter lists basic application examples and explains how to do the configuration. Detailed instruction examples can be found in the chapters of the individual modes.

9.1. Example sequence from start-up to frame acquisition

Notes for first-time epc611 chip operation:

1. Chip booting: Apply all the voltages. No special order is mandatory.
If in doubt: Apply V_{DDBS} with a delay. For SPI communication, V_{DDBS} is not necessary.
2. During and after boot-up: Polling on SPI with NOP until chip answers with IDLE (0x00).
3. To ensure memory addressing: SPI uses for the addresses SPI page and SPI address. Refer to Chapter 12.
4. Perform and read as first-time operation the 8x8 pixel grayscale mode GIM. Refer to Chapter 7.3.1 and Table 61.

9.2. 3D TOF distance measurement flow

A 3D TOF distance image, e.g. in TIM mode, is done with different steps according to Figure 55. The SPI interface is used for configuration, mode selection and temperature reading (marked blue in the following figures) and reading the frame data (marked red in the following figures). The sequence starts with the initialization of the epc611 registers with the necessary and correct configuration parameters. Next, the TOF measurement with the expected mode (4 DCS or 2 DCS) will be performed. Depending on the application and the ambient conditions (ambient-light, changing temperature conditions), the TOF measurement needs some compensation. For the purpose of more accurate ambient-light compensation, a grayscale measurement without illumination captures the background-light level. Reading of the on-chip temperature sensor (from time to time) helps to compensate thermal influences caused by the LEDs, the optical filters, the epc611 chip, etc. After the rearrangement of the grayscale image to the correct pixel orientation, the final 3D TOF distance image can be calculated with the necessary compensation.

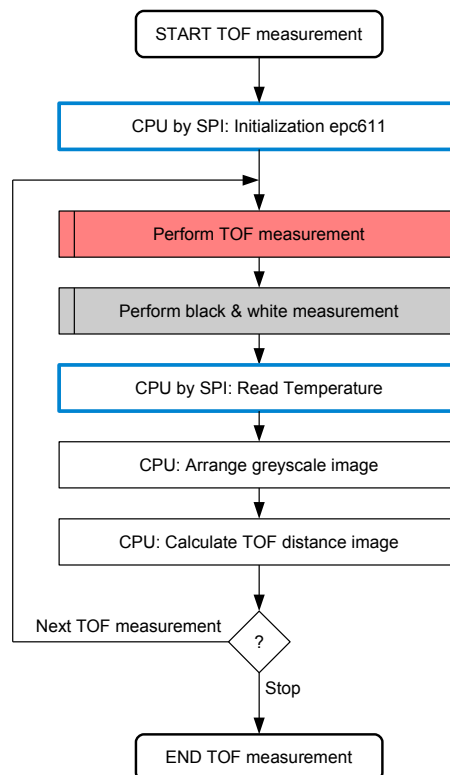


Figure 55: Generic example of the 3D TOF distance measurement flow (example TIM mode)

The process flows for distance measurements and for grayscale images are similar, see Figure 56. The main difference is the mode selection (number of DCS or grayscale) and dependant number of frames, which need to be read out during a process cycle. After mode setting, the cycle will be started by applying the SHUTTER. Once SHUTTER is activated, the epc611 executes the measurement until the end of the sequence autonomous.

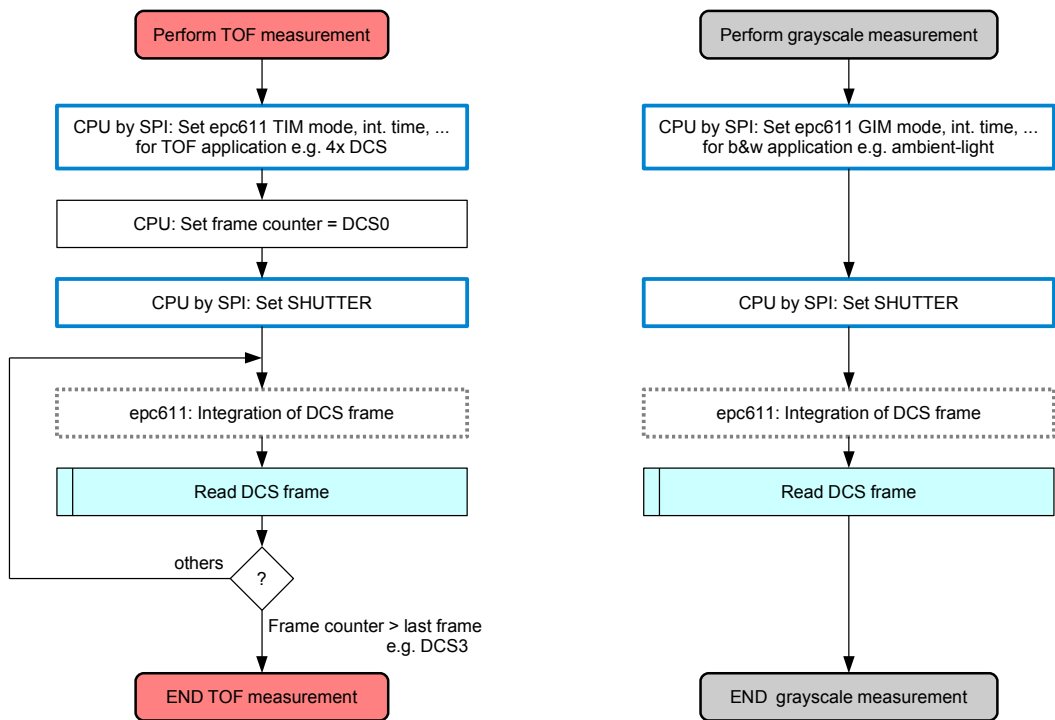


Figure 56: Generic sequences for the distance (TOF) and the grayscale measurement (example TIM mode)

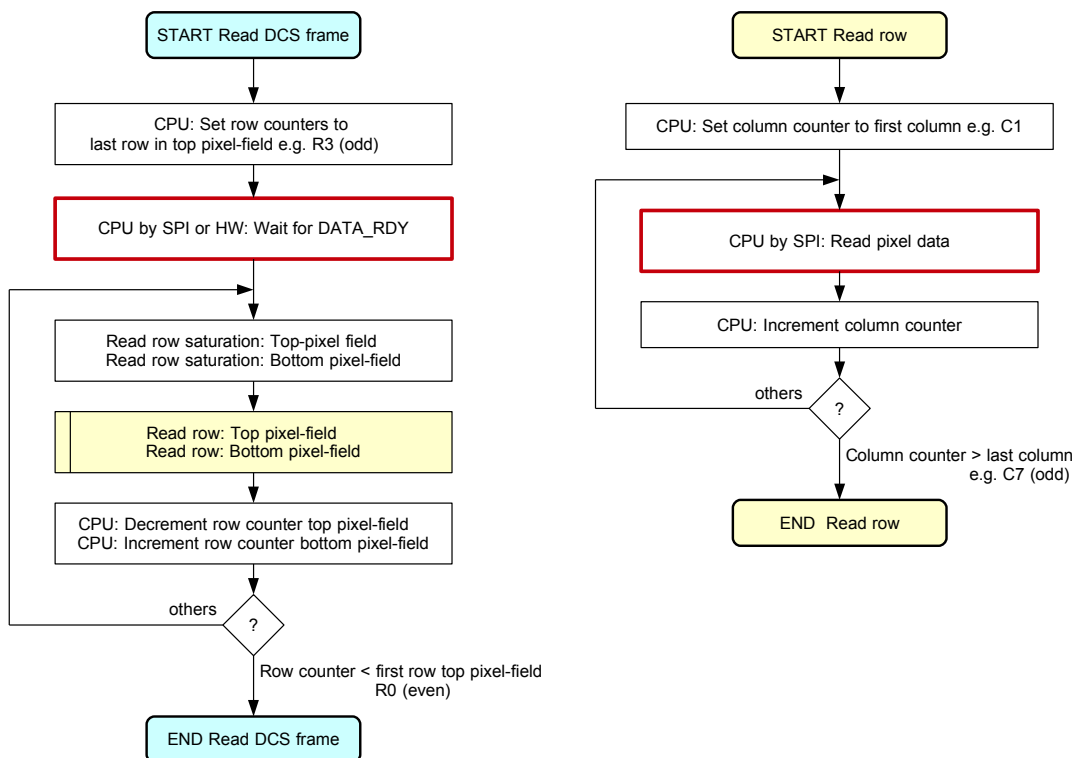


Figure 57: Generic sequences to readout frames and row by row (example TIM mode)

9.3. Rolling DCS frames

In special applications, it is possible to always use the same integration time in continuous distance measurement mode without any grayscale images for ambient-light compensation. Such a set-up allows the distance measurement rate to be enhanced by a factor of 4 by using rolling DCS frames.

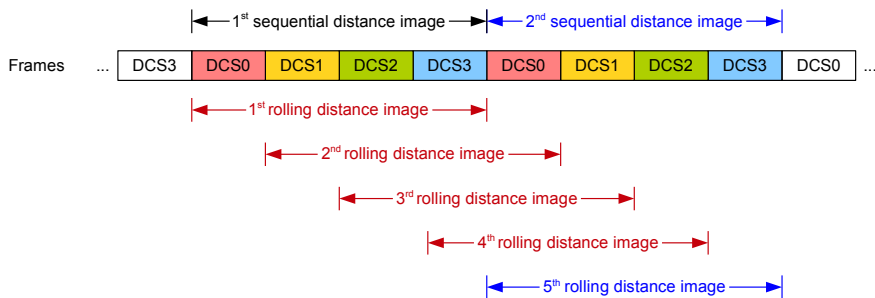


Figure 58: Rolling DCS frames

As shown in Figure 58, with each new DCS frame, the algorithm performs a new distance calculation based on the new and last three DCS frames. Details of the register settings are listed in the individual operation mode descriptions.

9.4. Enhanced rolling DCS frame mode

The epc611 allows individual parameters to be set for each single DCS access. This enables the ability to acquire in time-sequence DCSx frames with different integration times, etc.

The enhanced rolling mode combines all:

The stacking of integration times to enlarge the dynamic range, the acquisition of an ambient-light image for correction and the rolling mode to speed up the frame rate.

The final distance frame acquisition will be in an equidistant time manner, this for 2 or more different integration times.

Select the most reliable distance information out of the acquired integration time distance frames, already compensated each time, and compose the final distance picture.

The example shown here uses two integration times:

50 μ s for detecting short range objects and 2 ms for the long range objects.

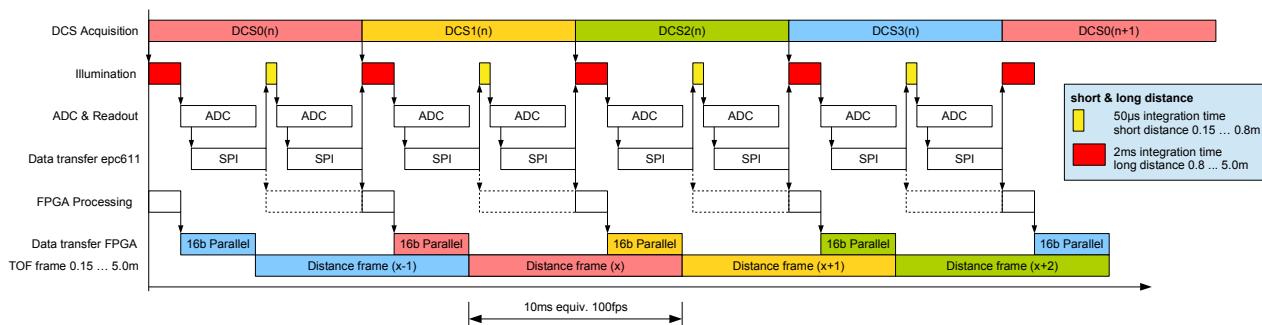


Figure 59: Enhanced rolling mode sequence

Implementation example step by step: Rolling mode using 3 integration times

1. Chose single frame mode by setting register P4[0x12] and P1[0x02].
2. Perform 4 DCS acquisition following next steps:
3. Select DCS0 and acquire 3 DCS0 each with one of the 3 integration times
Integration time t1 > SHUTTER > readout > integration time t2 > SHUTTER > readout > integration time t3 > SHUTTER > readout.
2nd and subsequent acquisitions:
Calculate for each integration time the distance and TOF amplitude image with the last 4 corresponding DCS frames.
Select the most reliable distance information out of the acquired integration time distance frames, already compensated each time, and compose the final distance picture.
4. Select DCS1 and acquire 3 DCS1 each with one of the 3 integration times
Integration time t1 > SHUTTER > readout > integration time t2 > SHUTTER > readout > integration time t3 > SHUTTER > readout
2nd and subsequent acquisitions:
Calculate for each integration time the distance and TOF amplitude image with the last 4 corresponding DCS frames.
Select the most reliable distance information out of the acquired integration time distance frames, already compensated each time, and compose the final distance picture.
5. ... and so on ...

The appropriate register settings P4[0x12] and P1[0x02] are listed in the corresponding mode chapters.

10. Parameter and configuration memory

10.1. Sequencer program

The sequencer program is the executable code of the chip's state-machine. ESPROS' approach is to always achieve optimal chip performance by offering the user the most suited sequencer program code. After each power-up, this program code must be downloaded by the application to the chip via the SPI interface. Refer to Chapter 13.6, Latest version of the sequencer program

IMPORTANT:

Always use the latest sequencer program which corresponds to chip type and version. Incorrect sequencer programs will derate chip performance or even worse, lead to malfunction.

10.2. Data memory map

The epc611 control registers (RAM) are used to control all features of the chip. They are organized as 256x8 bit into 0x00 ... 0xFF address locations. The address space 0x80 ... 0xFF is EEPROM backed-up. EEPROM parameters in this section are stored permanently between the power off/on cycles.

All registers can be accessed through the SPI interface by the application CPU, according to Chapter 11, SPI interface and Chapter 12, Register map. Multiple byte registers are stored in the order MSB first, then LSB.

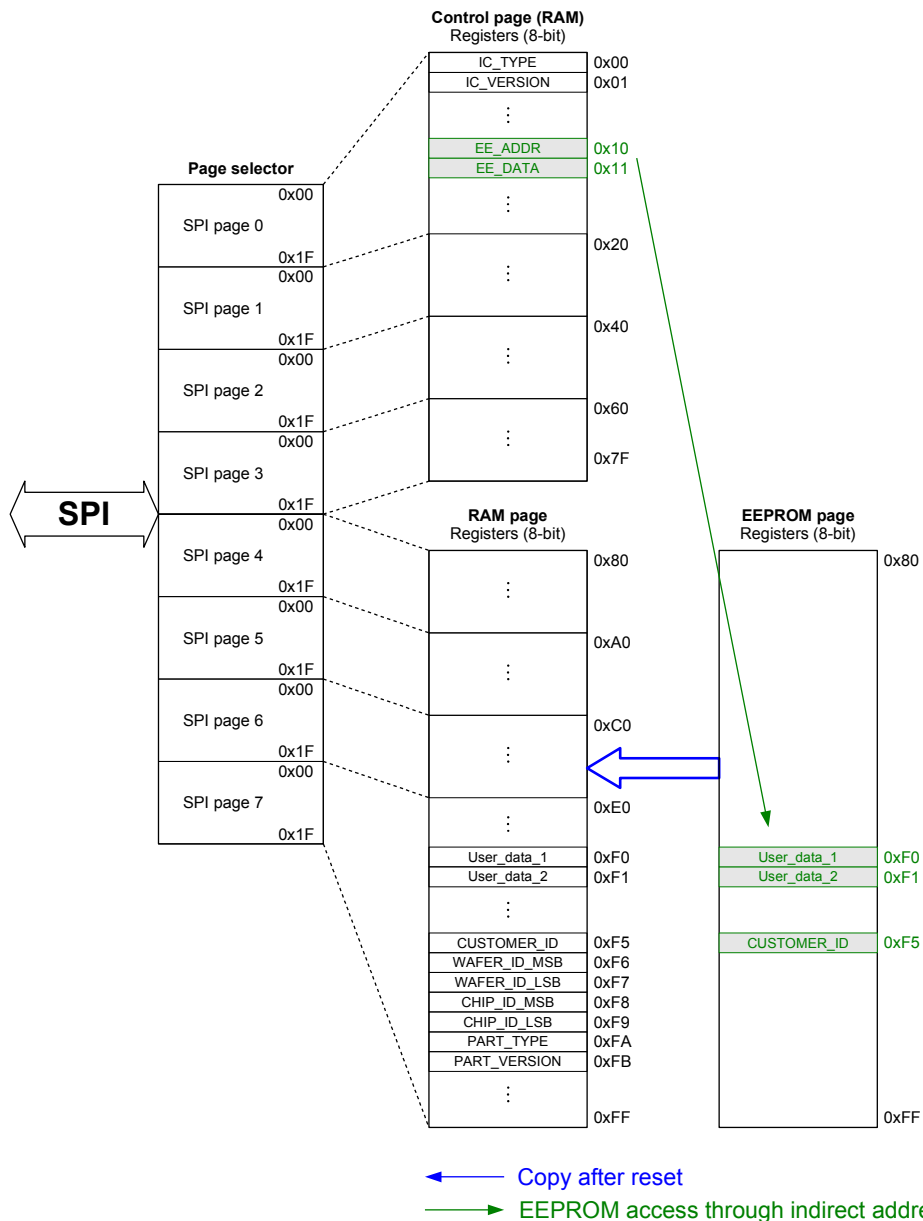


Figure 60: Memory map

10.2.1. Control page

The control page contains R/W accessible registers with default values during startup. The content can be changed via the I²C interface. The changed values are preserved as long as the IC is powered. A reset sets them back to their default values.

10.2.2. RAM page

The RAM page contains R/W accessible registers with EEPROM copied values after startup. The content can be changed via the I²C interface. The changed values are preserved as long as the IC is powered. They are set back to EEPROM values with a reset.

10.2.3. EEPROM page

The embedded 128x8-bit EEPROM stores operation parameters as well as factory-set trimming and calibration values.

11. SPI interface

The external microprocessor (master) communicates with the epc611 chip via the SPI interface. The master sets application-specific chip configurations, triggers the measurements and reads the data. The implemented interface supports single-slave environments only. The SPI lines need to be connected according to Figure 13.

11.1. SPI timing

The 16 bit epc611 SPI works as slave with a transfer rate up to 16 Mbit/s. While data (MOSI) is sent from the microprocessor to the epc611, the result (MISO) of the previous command is sent back according to the SPI protocol in Figure 61.

Designations of the SPI bus signals:

- \overline{nSS} Slave select and resynchronization
- SCLK Serial clock from master for the data transfer
- MOSI Serial data input slave
- MISO Serial data output slave; no tri-state output; only for single user systems

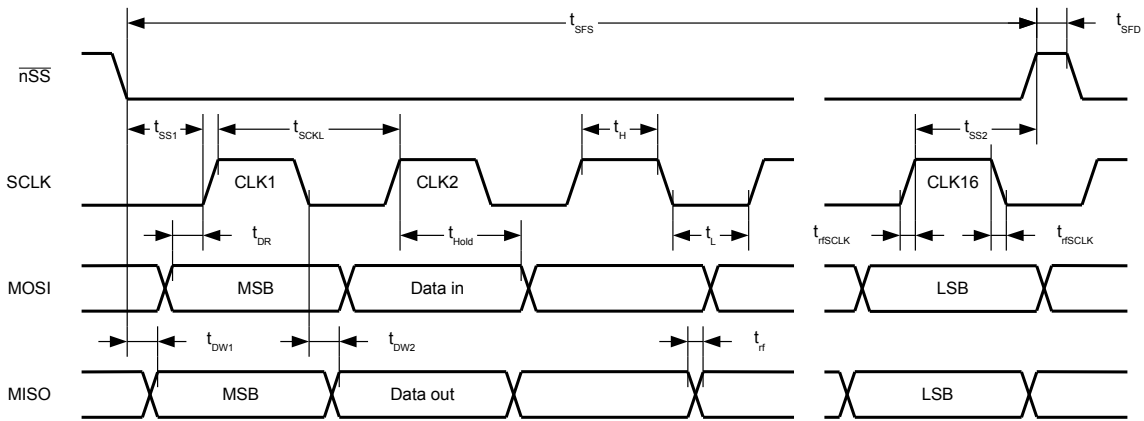


Figure 61: SPI bus timing diagram

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SFS}	Slave selection time for 1 complete data frame (word access)	$15.2 \cdot t_{SCLK}$			
t_{SFD}	Slave deselection time for the data frame synchronization	10			ns
f_{SCLK}	Clock frequency of SCKL			16	MHz
t_{SS1}	Set-up time for the first rising edge of SCKL after the falling edge of \overline{nSS}	15			ns
t_{SS2}	Set-up time for the rising edge of \overline{nSS} after the rising edge of clock 16	15			ns
t_{SCLK}	Cycle time of SCKL = $1/f_{SCLK}$	119			ns
t_H / t_L	HIGH and LOW period of SCKL	15			ns
t_{rSCLK}	Rise or fall time for the SCKL signal			10	ns
t_{DR}	Input data set-up time of MOSI before the rising edge of SCKL	15			ns
t_{Hold}	Input data hold time of MOSI	15			ns
t_{DW1}	Output data of MISO valid after the falling edge of \overline{nSS}			20	ns
t_{DW2}	Output data of MISO valid after the falling edge of SCKL			20	ns
t_r	Rise or fall time for the MOSI and MISO signals			8.5	ns

Table 78: SPI timing

11.2. SPI frame format

The SPI protocol is based on commands and responses. The application (SPI master) sends commands to the epc611 (SPI slave). The epc611 chip performs the requested operations and provides the response in the following SPI frame. Frames are transmitted sequentially with MSB bit first. The SPI master drives the $\overline{\text{nSS}}$ signal LOW while communicating with the slave.

	Command frame on MOSI, 16 bit MSB aligned		Response frame on MISO, 16 bit MSB aligned	
Section	Symbol	Parameter	Symbol	Parameter
ID	CID[2:0]	3 bit command ID	RID[2:0]	3 bit response ID
SPI address ¹	CADDR[4:0]	5 bit address	RADDR[4:0]	5 bit response address
Data	CDATA[7:0]	8 bit data	RDATA[7:0]	8 bit response data

Table 79: SPI command and response format

Note ¹: A memory location is effectively addressed by SPI pages and SPI addresses, according to Figure 60 and Table 83 ff.

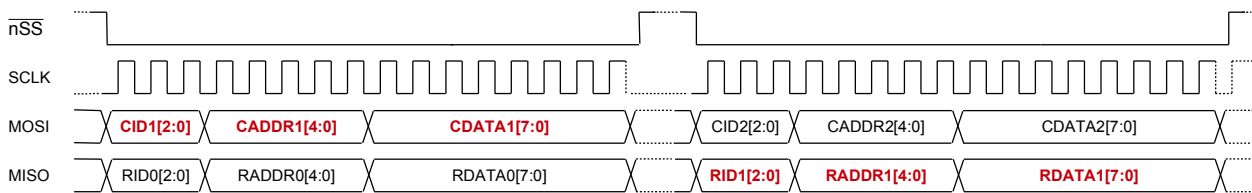


Figure 62: SPI frame format: Command and response thereof (red marked)

The $\overline{\text{nSS}}$ signal needs to be de-asserted and re-asserted between two consecutive SPI frames to allow correct on-chip synchronization and error detection. This inter-frame gap can be as short as defined in Table 78, parameter t_{SFD} . The falling $\overline{\text{nSS}}$ transition to LOW needs to be followed by a rising SCLK edge to HIGH. Refer to Table 78, parameter t_{DR1} . The rising edge of $\overline{\text{nSS}}$ terminates the command and starts the processing of the instruction, e.g. new register value becomes active.

Because the SPI transmits data bidirectionally at the same time, a request will be answered in the following SPI frame. Examples of correct sequences of the command protocols are shown in Figure 63 and Figure 64.

Example 1: READ commands

SPI frame 1	SPI frame 2	SPI frame 3	SPI frame 4	SPI frame 5
RD1	RD2	RD3	NOP	NOP
IDLE	RD1_DONE	RD2_DONE	RD3_DONE	IDLE

Figure 63: Read commands

Note: Use "NOP" to get last result.

Example 2: WRITE with delay and READ

If the epc611 is "BUSY" e.g. WRITE_NOT_DONE, any incoming command will be ignored. The application must track the responses and repeat a dropped command (red and blue frame).

SPI frame 1	SPI frame 2	SPI frame 3	SPI frame 4	SPI frame 5
WR1	RD1 (drop)	RD2	RD1 (repeat)	NOP
IDLE	WR1_NOT_DONE	WR1_DONE	RD2_DONE	RD1_DONE

Figure 64: WRITE with delay and READ

11.3. SPI commands

Command	CID [2:0]	Address [4:0]	Data [7:0]	Operation / usage																																																						
NOP	000	0 0000	0000 0000	"No operation". Used for polling during waiting for the response from the SPI or for completing the imager operation.																																																						
READ	001	a aaaa	0000 0000	Reads data from the requested register address a aaaa 5 bit read address																																																						
WRITE	010	a aaaa	dddd dddd	Writes data to the requested register address a aaaa 5 bit write address dddd dddd 8 bit write data																																																						
QUIT	011	0 0000	0000 0000	Stops all on-going READ or WRITE operations and returns to IDLE state.																																																						
PAGE_SELECT	100	0 0 P2 P1 P0	0000 0000	Selects the memory page (pointer). Refer also to Figure 60. The pointer remains until it is changed. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Page</th> <th>Memory addr.</th> <th>P2</th> <th>P1</th> <th>P0</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0x00 ... 0x1F</td> <td>0</td> <td>0</td> <td>0</td> <td>X</td> </tr> <tr> <td>1</td> <td>0x20 ... 0x3F</td> <td>0</td> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>2</td> <td>0x40 ... 0x5F</td> <td>0</td> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>3</td> <td>0x60 ... 0x7F</td> <td>0</td> <td>1</td> <td>1</td> <td></td> </tr> <tr> <td>4</td> <td>0x80 ... 0x9F</td> <td>1</td> <td>0</td> <td>0</td> <td></td> </tr> <tr> <td>5</td> <td>0xA0 ... 0xBF</td> <td>1</td> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>6</td> <td>0xC0 ... 0xDF</td> <td>1</td> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>7</td> <td>0xE0 ... 0xFF</td> <td>1</td> <td>1</td> <td>1</td> <td></td> </tr> </tbody> </table> <p style="text-align: center;">Table 80: Mapping of the memory page pointer bits P2, P1 and P0</p>	Page	Memory addr.	P2	P1	P0	Default	0	0x00 ... 0x1F	0	0	0	X	1	0x20 ... 0x3F	0	0	1		2	0x40 ... 0x5F	0	1	0		3	0x60 ... 0x7F	0	1	1		4	0x80 ... 0x9F	1	0	0		5	0xA0 ... 0xBF	1	0	1		6	0xC0 ... 0xDF	1	1	0		7	0xE0 ... 0xFF	1	1	1	
Page	Memory addr.	P2	P1	P0	Default																																																					
0	0x00 ... 0x1F	0	0	0	X																																																					
1	0x20 ... 0x3F	0	0	1																																																						
2	0x40 ... 0x5F	0	1	0																																																						
3	0x60 ... 0x7F	0	1	1																																																						
4	0x80 ... 0x9F	1	0	0																																																						
5	0xA0 ... 0xBF	1	0	1																																																						
6	0xC0 ... 0xDF	1	1	0																																																						
7	0xE0 ... 0xFF	1	1	1																																																						
RESET	110	0 0000	0000 0000	Initiates a software reset. Reloads the values stored in the EEPROM into the volatile memory. After RESET the chip is in IDLE state.																																																						
All other commands not listed above are reserved.																																																										

Table 81: SPI command list

11.4. SPI response

Response	RID [2:0]	Address [4:0]	Data [7:0]	Response to	Operation / usage
IDLE	000	0 0000	0000 0000	NOP	The SPI is in IDLE state. No operations pending.
READ_DONE	001	a aaaa	dddd dddd	READ	Successful READ. Returns the read data: a aaaa 5 bit read address dddd dddd 8 bit read data
WRITE_DONE	010	a aaaa	dddd dddd	WRITE	Successful WRITE a aaaa 5 bit write address dddd dddd 8 bit write data
READ_NOT_DONE	011	1 0011	0011 0011	READ	READ in progress. Action: Polling with NOP until device answers READ_DONE.
PAGE_RESPONSE	100	0 0 P2 P1 P0	0000 0000	PAGE_SELECT	Successful PAGE_SELECT. Returns the current page number. P2, P1 and P0: Page pointer bits as defined in Table 79.
WRITE_NOT_DONE	110	0 1100	1100 1100	WRITE	WRITE in progress: Action: Polling with NOP until device answers WRITE_DONE.
SYS_NOT_READY	111	0 1011	1111 1111	any	Response during chip boot-up. Action: Polling with NOP until device answers IDLE.
QUIT_RESPONSE	111	0 0011	1000 1110	QUIT	Successful QUIT. The device is in IDLE state.
ERROR	111	1 0101	1111 1111	any	Error occurred on the SPI bus e.g. command length was not correct. Action: Repeat this command correctly.
SPI_NOT_READY	111	1 1111	1111 1111	any	SPI slave is not ready. Action: Polling with NOP until device answers IDLE.
All other responses not listed above are nor used nor valid.					

Table 82: SPI response list

11.5. SPI pixel data readout and DATA_RDY

The pixel data and validity information for readout are present in the readout registers, which correspond to the selected operating mode. Pixel data which is ready for readout is stored in a buffer for off-loading by the application via SPI commands.

Buffering and readout are done on double-rows, one row of each half of the pixel-field top and bottom, except for readouts with one pixel only. Whenever a double-row is read, the buffers are updated with the data of the next double-row. For this reason, the saturation information of the double-row should be read first, followed by the data read out.

The availability of pixel data is indicated by the DATA_RDY signal (pin). Alternatively, the register P2[0x15] can be polled. It provides the DATA_RDY bit and the number of available data bytes in the buffer. A frame has as many double-row readouts as the half pixel-field has rows. Furthermore, in case of an empty buffer, the DATA_RDY is de-asserted. Refer to Figure 62.

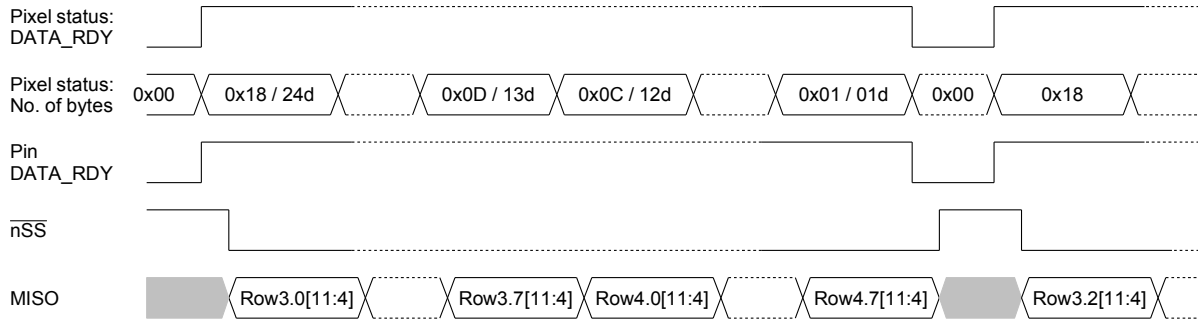


Figure 65: DATA_RDY control e.g. 12 bit data readout of a double-row

12. Register map

Notes:

P0[0x01] Array notation. Example is for the register at address 0x01 in SPI page 0. Refer to Figure 60.

** Shadow registers can be updated on-the-fly while a frame acquisition is going on. The new values are used at the start of the next SHUTTER.

Registers not listed are reserved and must not be altered by the user. Otherwise, chip malfunction can occur. However, if a register is accidentally overwritten, a RESET restores the factory settings.

The listed default values are after the download of the latest sequencer program to the chip.

12.1. SPI Page 0

Page addr.	RAM loc.	Type	Default	Description
P0[0x00]	0x00	R	---	IC type for device family identification. For chip type refer to register P7[0x1A].
P0[0x01]	0x01	R	---	IC version for device mask identification. For chip version refer to register P7[0x1B].
P0[0x11]	0x11	R/W	---	Address register for indirect read/write access to EEPROM: Refer to Figure 60. Use the absolute EEPROM address instead of the mapped page address.
P0[0x12]	0x12	R/W	---	Data register for indirect read/write access to EEPROM: Refer to Figure 60.

Table 83: Registers SPI Page 0

12.2. SPI Page 1

Page addr.	RAM loc.	Type	Default	Description		
P1[0x02]	0x22	R/W	0x34	DCS selection for 1 st frame (refer to the operation mode chapters):		
				Bit	Function	Default
				0	mgx0 modulator (mga0, mgb0):	0
				1	00: DCS 0 01: DCS 1 10: DCS 2 11: DCS 3	0
				2	mgx1 modulator (mga1, mgb1):	0
				3	00: DCS 0 01: DCS 1 10: DCS 2 11: DCS 3	0
4..7	reserved	0x3				
P1[0x04]	0x24	R/W	0x00	Modulation control 1 st frame (refer to Chapter 6.6):		
				Bit	Function	Default
				0..3	reserved	0
				4	0: LED/LD is modulated 1: LED/LD on during integration: Refer to IMPORTANT, Chapter 6.6	0
				5	0: LED/LD is modulated 1: LED/LD off during integration	0
6,7	reserved	0				
P1[0x05]	0x25	R/W	0x3D	DCS selection for 2 nd frame (refer to the operation mode chapters):		
				Bit	Function	Default
				0	mgx0 modulator (mga0, mgb0):	0
				1	00: DCS 0 01: DCS 1 10: DCS 2 11: DCS 3	0
				2	mgx1 modulator (mga1, mgb1):	0
				3	00: DCS 0 01: DCS 1 10: DCS 2 11: DCS 3	0
4..7	reserved	0x3				

Table 84: Registers SPI Page 1

Page addr.	RAM loc.	Type	Default	Description		
P1[0x07]	0x27	R/W	0x00	Modulation control 2 nd frame (refer to Chapter 6.6):		
				Bit	Function	Default
				0..3	reserved	0
				4	0: LED/LD is modulated 1: LED/LD on during integration: Refer to IMPORTANT, Chapter 6.6	0
				5	0: LED/LD is modulated 1: LED/LD off during integration	0
6,7	reserved	0				
P1[0x1C]	0x3C	R/W	0x26	Modulation control in grayscale mode (refer to Chapter 6.6):		
				Bit	Function	Default
				0..3	reserved	0x6
				4	0: LED/LD is modulated 1: LED/LD on during integration: Refer to IMPORTANT, Chapter 6.6	0
				5	0: LED/LD is modulated 1: LED/LD off during integration	1
6,7	reserved	0				

Cont. Table 84: Registers SPI Page 1

12.3. SPI Page 2

Page addr.	RAM loc.	Type	Default	Description
P2[0x0A]	0x4A	R	0x00	Temperature sensor:
P2[0x0B]	0x4B	R	0x00	Temperature reading must follow temperature/greyscale image reading referred in Chapter 8.
P2[0x0C]	0x4C	R	0x00	12 bit/pixel data readout mode: PIXEL_EVEN and PIXEL_ODD readout for TIM, RBH, GIM and GBI modes. Refer to the corresponding operating mode chapters for detailed description. Refer also to register P2[0x0D] ... P2[0x13]: saturation, ADC over- and underflow flags.
P2[0x0D]	0x4D	R	0x00	Pixel saturation flags per row of top half of the pixel-field for 12 bit/pixel data readout mode: b7 ... b0: correspond to pixel-field column 7 ... 0. 0: Pixel is not saturated 1: Pixel is saturated. Pixel data is not reliable. Validity: Saturation flags of any double-row should be read first, followed by the data read out. Whenever a double-row has been read, the buffers are updated with the data of the next double-row.
P2[0x0E]	0x4E	R	0x00	Pixel saturation flags per row of bottom half of the pixel-field for 12 bit/pixel data readout mode: Description, see register P2[0x0D] above.
P2[0x10]	0x50	R	0x00	ADC overflow flags per row of top half of the pixel-field for 12 bit/pixel data readout mode: b7 ... b0: correspond to pixel-field column 7 ... 0. 0: no ADC overflow 1: ADC overflow detected. Pixel data is not reliable. Validity: ADC overflow flags of any double-row should be read first, followed by the data read out. Whenever a double-row has been read, the buffers are updated with the data of the next double-row.
P2[0x11]	0x51	R	0x00	ADC overflow flags per row of bottom half of the pixel-field for 12 bit/pixel data readout mode: Description, see register P2[0x10] above.
P2[0x12]	0x52	R	0x00	ADC underflow flags per row of top half of the pixel-field for 12 bit/pixel data readout mode: b7 ... b0: correspond to pixel-field column 7 ... 0: 0: no ADC underflow 1: ADC underflow detected. Pixel data is not reliable. Validity: ADC underflow flags of any double-row should be read first, followed by the data read out. Whenever a double-row has been read, the buffers are updated with the data of the next double-row.
P2[0x13]	0x53	R	0x00	ADC underflow flags per row of bottom half of the pixel-field for 12 bit/pixel data readout mode: Description, see register P2[0x12] above.

Table 85: Registers SPI Page 2

Page addr.	RAM loc.	Type	Default	Description												
P2[0x14]	0x54	R	0x00	14, 15, 18 bit pixel data readout register for digital on-chip sum_modes SUM_DATA: 14 bit: UFS and LNH mode, 15 bit: UHD and NBF mode, 18 bit: ULN mode Refer to the corresponding operating mode chapter for detailed description. Notes: 1. Unsigned data applies the same format rules but with corresponding unsigned values e.g. signed 0x 01 FF FF is same as unsigned 0x 03 FF FF. 2. SUM_DATA is raw format without embedded information if P4[0x15], bit 6 is 1.												
P2[0x15]	0x55	R	0x00	Pixel readout status (refer to Figure 65): <table border="1"> <thead> <tr> <th>Bit</th> <th>Function</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>0..5</td> <td>Number of bytes ready/remaining for current double-row readout.</td> <td>0</td> </tr> <tr> <td>6</td> <td>reserved</td> <td>0</td> </tr> <tr> <td>7</td> <td>Pixel data ready status. Same signal as on pin 3, DATA_RDY: 0: No data for readout 1: Ready for readout register P2[0x0C] or P2[0x14] according to selected operating mode.</td> <td>0</td> </tr> </tbody> </table>	Bit	Function	Default	0..5	Number of bytes ready/remaining for current double-row readout.	0	6	reserved	0	7	Pixel data ready status. Same signal as on pin 3, DATA_RDY: 0: No data for readout 1: Ready for readout register P2[0x0C] or P2[0x14] according to selected operating mode.	0
Bit	Function	Default														
0..5	Number of bytes ready/remaining for current double-row readout.	0														
6	reserved	0														
7	Pixel data ready status. Same signal as on pin 3, DATA_RDY: 0: No data for readout 1: Ready for readout register P2[0x0C] or P2[0x14] according to selected operating mode.	0														
P2[0x18]	0x58	R/W	0x00	SHUTTER control: <table border="1"> <thead> <tr> <th>Bit</th> <th>Function</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SHUTTER release. Refer to chapter 7.4. 0: disable 1: enable. In single shot mode: Starts acquisition and is auto cleared. Note: SHUTTER release is not auto-cleared when multiple frames is enabled.</td> <td>0</td> </tr> <tr> <td>1</td> <td>Multiple frames (auto-run or video mode). Refer to chapter 7.4.2. 0: disable. Single shot mode. 1: enable. Multiple frame mode active if shutter enabled.</td> <td>0</td> </tr> <tr> <td>2..7</td> <td>reserved</td> <td>0</td> </tr> </tbody> </table>	Bit	Function	Default	0	SHUTTER release. Refer to chapter 7.4. 0: disable 1: enable. In single shot mode: Starts acquisition and is auto cleared. Note: SHUTTER release is not auto-cleared when multiple frames is enabled.	0	1	Multiple frames (auto-run or video mode). Refer to chapter 7.4.2. 0: disable. Single shot mode. 1: enable. Multiple frame mode active if shutter enabled.	0	2..7	reserved	0
Bit	Function	Default														
0	SHUTTER release. Refer to chapter 7.4. 0: disable 1: enable. In single shot mode: Starts acquisition and is auto cleared. Note: SHUTTER release is not auto-cleared when multiple frames is enabled.	0														
1	Multiple frames (auto-run or video mode). Refer to chapter 7.4.2. 0: disable. Single shot mode. 1: enable. Multiple frame mode active if shutter enabled.	0														
2..7	reserved	0														

Cont. Table 85: Registers SPI Page 2

12.4. SPI Page 3

Page addr.	RAM loc.	Type	Default	Description
P3[0x11]	0x71	R/W	0x00	Number of short DLL steps to delay the LED output by approx. 10ps per step:
P3[0x12]	0x72	R/W	0x00	Valid only if bit 2 in register P5[0x0E] is enabled. Refer also to register P5[0x0E] and Chapter 6.7. Max. value is 799 (0x31F). Note: Delay is sensitive to V _{DD} variations and noise.
P3[0x13]	0x73	R/W	0x00	Number of large DLL steps to delay the LED output by approx. 2ns per step: Valid only if bit 2 in register P5[0x0E] is enabled. Refer also to register P5[0x0E] and Chapter 6.7. Max. value is 49 (0x31). Note: Delay is sensitive to V _{DD} variations and noise.

Table 86: Registers SPI Page 3

12.5. SPI Page 4

Page addr.	RAM loc.	Type	Default	Description																					
P4[0x00]	0x80	R/W	0x3F	Clock control: <table border="1"> <thead> <tr> <th>Bit</th> <th>Function</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>0..5</td> <td>reserved</td> <td>0x3F</td> </tr> <tr> <td>6</td> <td>Modulation clock source: 0: Internal modulation clock 1: External clock from EXTMOD input</td> <td>0</td> </tr> <tr> <td>7</td> <td>reserved</td> <td>0</td> </tr> </tbody> </table>	Bit	Function	Default	0..5	reserved	0x3F	6	Modulation clock source: 0: Internal modulation clock 1: External clock from EXTMOD input	0	7	reserved	0									
Bit	Function	Default																							
0..5	reserved	0x3F																							
6	Modulation clock source: 0: Internal modulation clock 1: External clock from EXTMOD input	0																							
7	reserved	0																							
P4[0x05]	0x85	R/W	0x01	Modulation clock divider: <table border="1"> <thead> <tr> <th>Bit</th> <th>Function</th> <th>Default</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Modulation clock divider provides the clock to the LED modulator and pixel-field demodulator circuits by integer division of the internal PLL clock or EXTMOD:</td> <td>1</td> </tr> <tr> <td>1</td> <td></td> <td>0</td> </tr> <tr> <td>2</td> <td>$f_{mod_clk} = 80MHz / (modulation\ clock\ divider + 1)$</td> <td>0</td> </tr> <tr> <td>3</td> <td>Default: 80MHz / (0x01 + 0x01): $f_{mod_clk} = 40MHz$</td> <td>0</td> </tr> <tr> <td>4</td> <td>Maximal value of modulation clock divider = 0x1F: $f_{mod_clk} = 2.5MHz$ Note: The LED modulation frequency is 4 times lower than f_{mod_clk}</td> <td>0</td> </tr> <tr> <td>5..7</td> <td>reserved</td> <td>0</td> </tr> </tbody> </table>	Bit	Function	Default	0	Modulation clock divider provides the clock to the LED modulator and pixel-field demodulator circuits by integer division of the internal PLL clock or EXTMOD:	1	1		0	2	$f_{mod_clk} = 80MHz / (modulation\ clock\ divider + 1)$	0	3	Default: 80MHz / (0x01 + 0x01): $f_{mod_clk} = 40MHz$	0	4	Maximal value of modulation clock divider = 0x1F: $f_{mod_clk} = 2.5MHz$ Note: The LED modulation frequency is 4 times lower than f_{mod_clk}	0	5..7	reserved	0
Bit	Function	Default																							
0	Modulation clock divider provides the clock to the LED modulator and pixel-field demodulator circuits by integer division of the internal PLL clock or EXTMOD:	1																							
1		0																							
2	$f_{mod_clk} = 80MHz / (modulation\ clock\ divider + 1)$	0																							
3	Default: 80MHz / (0x01 + 0x01): $f_{mod_clk} = 40MHz$	0																							
4	Maximal value of modulation clock divider = 0x1F: $f_{mod_clk} = 2.5MHz$ Note: The LED modulation frequency is 4 times lower than f_{mod_clk}	0																							
5..7	reserved	0																							

Table 87: Registers SPI Page 4

Page addr.	RAM loc.	Type	Default	Description		
P4[0x0B]	0x8B	R/W	0x01	<p>Number of PLL clock periods to delay the demodulation signal (all modulation modes): It can be used to insert a phase-shift between modulation (LED) and demodulation (pixel). 1 PLL clock cycle is 12.5ns @ 80MHz PLL clock. This is equivalent to a distance shift of 1.875m independent of the LED modulation frequency. Note: This phase-shift is temperature independent.</p> <p>0: no delay 1: 1 clock 2: 2 clocks ... 12: 12 clocks (max. value)</p>		
P4[0x10]	0x90	R/W	0xC4	LED Modulation selection (refer to Chapter 6.6):		
				Bit	Function	Default
				0	reserved	0
				1	Inverts output signals LEDOD and LEDPP if drivers are enabled: 0: non-inverted, e.g. LED = 0, not active: Pin LEDOD non-conductive, LEDPP = GND. 1: inverted, e.g. LED = 0, not active: Pin LEDOD conductive, LEDPP = V _{DDIO} .	0
				2	LED output selection: 0: LED driver is disable. Pin LED is non-conductive. 1: LED driver is enabled.	1
				3	reserved	0
				4	LED/LD permanently on (torch function, no modulation) if drivers are enabled: 0: off 1: on (Refer to IMPORTANT, Chapter 6.6)	0
				5	LEDPP output selection: 0: LEDPP driver disabled. Output is in Tri-State with termination resistor to GND. 1: LEDPP driver enabled.	0
6..7	reserved	1				
P4[0x12] **	0x92	R/W	0x30	DCS mode selection (refer to Chapters 7.2 and 7.3):		
				Bit	Function	Default
				0	Modulation selection per frame:	0
				1	00: All rows use same DCSx	0
					01: reserved	
					10: RBH mode with 2 DCS group based	
					11: NBF mode with 4 DCS	
				2	Integration time selection per frame:	0
				3	00: All rows use integration length P5[0x02], P5[0x03].	0
					01: reserved	
10: Multiple integration times according to the settings in the integration length row registers P7[0x00] ... P7[0x0F]. 11: reserved						
4	Number of DCS readouts:	1				
5	00: 1x DCSx or grayscale	1				
	01: 2x DCSx: DCS0, DCS1 or DCS2, DCS3					
	10: reserved					
	11: 4x DCSx: DCS0, DCS1, DCS2, DCS3					
6	Modulation mode selection:	0				
7	00: TOF mode	0				
	01: reserved					
	10: reserved					
	11: Grayscale mode					

Cont. Table 87: Registers SPI Page 4

Page addr.	RAM loc.	Type	Default	Description		
P4[0x15] **	0x95	R/W	0x23	Readout mode (refer to Chapters 7.2 and 7.3):		
				Bit	Function	Default
				0, 1	reserved	1
				2	Pixel-field readout mode selection:	0
				3	Refer to specific operating modes for details.	0
				4	000: Basic mode 8x8 pixel: TIM, GIM 001: 64 pixel sum: ULN 010: 4 pixel sum center: UFS 011: 8 pixel row sum: UHD, NBF 100: 4 pixel row sum (h+v binning): LNH 101: Basic mode 4x4 pixel (h+v binning): RBH, GBI others: reserved	0
				5	Readout data-format selection: 0: unsigned integer (0 ... 4'095d) 1: 2's complement signed integer (-2'048 ... 2'047d), default	1
				6	Embedding of validity information in data word (saturation, ADC overflow, ADC underflow): 0: Embedded in data, default 1: Raw data format	0
7	reserved	0				

Cont. Table 87: Registers SPI Page 4

12.6. SPI Page 5

Page addr.	RAM loc.	Type	Default	Description
P5[0x00] **	0xA0	R/W	0x00	Integration length multiplier (10 bit value):
P5[0x01] **	0xA1	R/W	0x01	Refer to Chapter 7.5.
P5[0x02] **	0xA2	R/W	0x00	Integration length (16 bit value):
P5[0x03] **	0xA3	R/W	0x01	Number of modulation clock periods for the integration time setting, using single integration time mode per frame. Refer to Chapter 7.5.1, Single integration time per frame.
P5[0x0E]	0xAE	R/W	0x01	DLL control: Refer to register P3[0x13] and Chapter 6.7. 0x01: no delay 0x04: delay manually set by register P3[0x13]

Table 88: Registers SPI Page 5

12.7. SPI Page 6

P6[0x19]	0xD9	R/W	---	Temperature offset correction: Value according to the formula of Chapter 8 for the calculation by the application SW. Range approx. -27 ... +27°C in steps of 0.2°C approx. The reference temperature is +27°C. 0x7F (127) corresponds to 0°C offset. 0xFF: Function is not yet supported. Temperature reading must follow temperature/greyscale image reading referred in Chapter 8.
P6[0x1A]	0xDA	R/W	---	DLL step: Refer for details to register P3[0x13] and Figure 19. The exact value is $t_{DLL} = ((\text{register P6[0x1A]} - 128) * 0.003\text{ns}) + 2.1\text{ns}$ (at +27°C, $V_{DD}, V_{DDPLL} = 1.8\text{V}$). 0xFF: Function is not yet supported.

Table 89: Registers SPI Page 6

12.8. SPI Page 7

Page addr.	RAM loc.	Type	Default	Description
P7[0x00] **	0xE0	R/W	0x00	Integration length row0:
P7[0x01] **	0xE1	R/W	0x01	Number of modulation clock periods for the integration time setting of row 0 using multiple integration time mode per frame (UHD, LNH, RBH). Refer to Chapter 7.5.2, Multiple integration times per frame.
P7[0x02] **	0xE2	R/W	0x00	Integration length row1:
P7[0x03] **	0xE3	R/W	0x01	Description, see register P7[0x00].
P7[0x04] **	0xE4	R/W	0x00	Integration length row2:
P7[0x05] **	0xE5	R/W	0x01	Description, see register P7[0x00].
P7[0x06] **	0xE6	R/W	0x00	Integration length row3:
P7[0x07] **	0xE7	R/W	0x01	Description, see register P7[0x00].
P7[0x08] **	0xE8	R/W	0x00	Integration length row4:
P7[0x09] **	0xE9	R/W	0x01	Description, see register P7[0x00].
P7[0x0A] **	0xEA	R/W	0x00	Integration length row5:
P7[0x0B] **	0xEB	R/W	0x01	Description, see register P7[0x00].
P7[0x0C] **	0xEC	R/W	0x00	Integration length row6:
P7[0x0D] **	0xED	R/W	0x01	Description, see register P7[0x00].
P7[0x0E] **	0xEE	R/W	0x00	Integration length row7:
P7[0x0F] **	0xEF	R/W	0x01	Description, see register P7[0x00].
P7[0x10] **	0xF0	R/W	0x00	User register for user data:
P7[0x11] **	0xF1	R/W	0x00	Refer to Figure 60. Do not write the register during frame acquisition. The number of WRITE cycles into the EEPROM should not exceed 100 WRITE operations.
P7[0x15] **	0xF5	R/W	0x00	Customer ID: Refer to Figure 60. Do not write the register during frame acquisition. The number of WRITE cycles into the EEPROM should not exceed 100 WRITE operations.
P7[0x16]	0xF6	R	---	Wafer ID
P7[0x17]	0xF7	R	---	
P7[0x18]	0xF8	R	---	
P7[0x19]	0xF9	R	---	
P7[0x1A]	0xFA	R	0x06	Chip and part type: For epc611 = 0x06
P7[0x1B]	0xFB	R	---	Chip and part version (release) e.g. 0x01 for version -001

Table 90: Registers SPI Page 7

13. Control command examples

Note: Each operation mode chapter contains an example of the basic operation and readout of the chip.

13.1. Reading part version

Action	MOSI	MISO	Comment
Select page 7	0x 87 00	0x ...	
Read part version	0x 3B 00	0x 87 00	
NOP	0x 00 00	0x 3B xx	Response: Part version = 0x xx

Table 91: Reading part version

13.2. Reading IC version

Action	MOSI	MISO	Comment
Select page 0	0x 80 00	0x ...	
Read IC version	0x 21 00	0x 80 00	
NOP	0x 00 00	0x 21 xx	Response: IC version = 0x xx

Table 92: Reading IC version

13.3. Reading WAFER ID and CHIP ID

Action	MOSI	MISO	Comment
Select page 7	0x 87 00	0x	
Read Wafer ID MSB	0x 36 00	0x 87 00	
Read Wafer ID LSB	0x 37 00	0x 36 xx	Response: Wafer ID MSB = 0x xx
Read Chip ID MSB	0x 38 00	0x 37 xx	Response: Wafer ID LSB = 0x xx
Read Chip ID LSB	0x 39 00	0x 38 xx	Response: Chip ID MSB = 0x xx
NOP	0x 00 00	0x 39 xx	Response: Chip ID LSB = 0x xx

Table 93: Reading WAFER ID and CHIP ID

13.4. Writing to EEPROM

Action	MOSI	MISO	Comment
Select page 0	0x 80 00	0x	
Select EEPROM address 0x F0	0x 51 F0	0x 80 00	Select user register P7[0x10]
Write data to EEPROM	0x 52 xx	0x 51 F0	Data value = xx
NOP	0x 00 00	0x 52 xx	

Table 94: Write to EEPROM

13.5. Reading from EEPROM

Action	MOSI	MISO	Comment
Select page 0	0x 80 00	0x	
Select EEPROM address 0x F0	0x 51 F0	0x 80 00	Select user register P7[0x10]
Read data from EEPROM	0x 32 00	0x 51 F0	
NOP	0x 00 00	0x 73 33	READ_NOT_DONE
Send NOP until	0x 00 00	0x 32 xx	Response: Data = 0x xx

Table 95: Read EEPROM

13.6. Latest version of the sequencer program

For having best chip performance, download each time after power-up or reset the following code sequences. Use the sequencer program below (e.g. epc611_Seq_Prog-Vxx) and the "Adjust default settings" (see item 4 below). Is a more actual version available than listed here, it will always be enclosed in the latest version of the evaluation kit download package.

1. Start up epc611 chip.
2. Wait until the chip is in READY state.
3. Prior activating the shutter, download the sequencer program by SPI for reprogramming the epc611.
4. Refer to the basic example tables for each mode, sections "Adjust default settings": Set registers accordingly, e.g. for TIM mode Table 21.
5. The chip is now ready to be used according to the datasheet.

Actual sequencer program (at the time of publishing this datasheet version):

```
# epc611_Seq_Prog-V02
# This program is for following epc611 chip versions: >000.
# The following sequence of SPI commands re-programs an
# epc611 chip in order to be on most actual functionality.
#
# The syntax of the SPI commands is as follows:
# Writing to SPI bus: SPI w BYTE0 BYTE1
# Whereas:
# - BYTE0: CID[0:2] + Address[4:0]
# - BYTE1: Data[7:0]

SPI w 84 00 # PAGE_SELECT 4
SPI w 51 00 # WRITE 0x11 0x00
SPI w 82 00 # PAGE_SELECT 2
SPI w 47 01 # WRITE 0x07 (SR_Program) 0x01
SPI w 40 00 # WRITE 0x00 (SR_Address) 0x00
SPI w 41 43 # WRITE 0x01 (SR_Data_0) 0x43
SPI w 42 18 # WRITE 0x02 (SR_Data_1) 0x18
SPI w 43 10
SPI w 44 03
SPI w 45 50
SPI w 46 2F
SPI w 47 07
SPI w 40 01
SPI w 41 43
SPI w 42 08
SPI w 43 01
SPI w 44 00
SPI w 45 3C
SPI w 46 31
SPI w 47 07
SPI w 48 03
SPI w 47 00
SPI w 84 00 # PAGE_SELECT 0
SPI w 51 01 # WRITE 0x11 0x01
```

14. Addendum

14.1. Terms, definitions and abbreviations

Abbreviation	Term, definition	Explanation
ABS	Automatic Backlight Suppression	
ADC	Analog Digital Converter	
AMR	Ratio of Ambient-light / Modulated light	
CSP	Chip Scale Package	
DCS	Differential Correlation Sample	
DLL	Delay Locked Loop	On-chip delay line of the epc611 chip
fps	Frames per second	
GBI	4x4 pixel Grayscale Binned pixel Imager	
GIM	8x8 pixel Grayscale IMager	
HDR	High Dynamic Range	
IC	Integrated Circuit	
LED/LD	Light Emitting Diode / Laser Diode	
LNH	Low Noise High dynamic range range-finder	
LSB	Least Significant Bit	
MGA	Modulation Gate A	
MGB	Modulation Gate B	
MGX	Modulation Gate A or B	
mga	MGA control signal	
mgb	MGB control signal	
mgx	MGX control signal	
MSB	Most Significant Bit	
NBF	No motion-Blur Fast range-finder	
OSC	Oscillator	
PLL	Phase Locked Loop	
RBH	Reduced motion-Blur High dynamic range range-finder	
SGA	Storage Gate A	
SGB	Storage Gate B	
SGX	Storage Gate A or B	
SPI	Serial Peripheral Interface	
TIM	8x8 pixel 3D TOF Imager Mode	
TOF	Time of Flight	
UFS	Ultra Fast and Sensitive range-finder	
UHD	Ultra High Dynamic range range-finder	
XTAL	Crystal	

Table 96: Definitions and abbreviations

14.2. Related documents

- 3D-TOF, A guideline to 3D-TOF sensors that work, Beat De Coi, ISBN 978-3-033-07096-7.
- Application note AN08 Process-Rules CSP Assembly, ESPROS Photonics Corp.
- Application note AN10 Calibration and Compensation, ESPROS Photonics Corp.
- Application note AN11 DME 660 Photobiological Safety Analysis, ESPROS Photonics Corp.
- Application note AN12 TOF data improvement toolbox, ESPROS Photonics Corp.

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