



ON Semiconductor®

NC7SZ125

TinyLogic® UHS Buffer with Three-State Output

Features

- Ultra-High Speed: t_{PD} 2.6 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ± 24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V V_{CC}
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

Description

The NC7SZ125 is a single buffer with three-state output from ON Semiconductor's Ultra-High Speed (UHS) of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V range. The inputs and output are high impedance above ground when V_{CC} is 0 V. Inputs tolerate voltages up to 6 V independent of V_{CC} operating voltage. The output tolerates voltages above V_{CC} when in the 3-STATE condition.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ125M5X	7Z25	5-Lead SOT23, JEDEC MO-178 1.6 mm	3000 Units on Tape & Reel
NC7SZ125P5X	Z25	5-Lead SC70, EIAJ SC-88a, 1.25 mm Wide	3000 Units on Tape & Reel
NC7SZ125L6X	DD	6-Lead MicroPak™, 1.00 mm Wide	5000 Units on Tape & Reel
NC7SZ125FHX	DD	6-Lead, MicroPak2, 1x1 mm Body, .35mm Pitch	5000 Units on Tape & Reel

Connection Diagrams

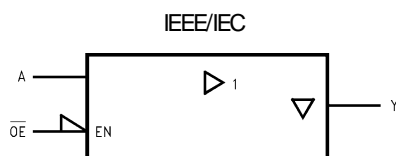


Figure 1. Logic Symbol

Pin Configurations

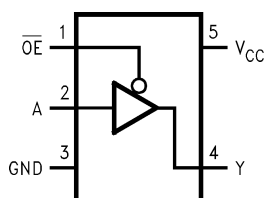


Figure 2. SC70 and SOT23 (Top View)

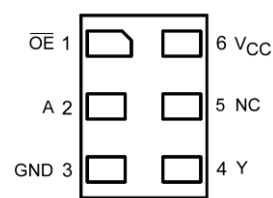


Figure 3. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70 / SOT23	Pin # MicroPak	Name	Description
1	1	OE	Input
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V _{CC}	Supply Voltage
	5	NC	No Connect

Function Table

Inputs		Output
/OE	In A	Out Y
L	L	L
L	H	H
H	X	Z

H = HIGH Logic Level

L = LOW Logic Level

X = HIGH or LOW Logic Level

Z = HIGH Impedance State

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	6.0	V
V_{IN}	DC Input Voltage		-0.5	6.0	V
V_{OUT}	DC Output Voltage		-0.5	6.0	V
I_{IK}	DC Input Diode Current	$V_{IN} < -0.5\text{ V}$		-50	mA
		$V_{IN} > 6.0\text{ V}$		+20	
I_{OK}	DC Output Diode Current	$V_{OUT} < -0.5\text{ V}$		-50	mA
		$V_{OUT} > 6\text{ V}, V_{CC}=\text{GND}$		+20	
I_{OUT}	DC Output Current			± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			± 50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SOT-23		200	mW
		SC70-5		150	
		MicroPak-6		130	
		MicroPak2-6		120	
ESD	Human Body Model, JESD22-A114			4000	V
	Charged Device Model, JESD22-C101			2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active State	0	V_{CC}	V
		Three-State	0	5.5	
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V, 2.5 V $\pm 0.2\text{ V}$	0	20	ns/V
		V_{CC} at 3.3 V $\pm 0.3\text{ V}$	0	10	
		V_{CC} at 5.0 V $\pm 0.5\text{ V}$	0	5	
θ_{JA}	Thermal Resistance	SOT-23		300	°C/W

		SC70-5		425	
		MicroPak-6		500	
		MicroPak2-6		560	

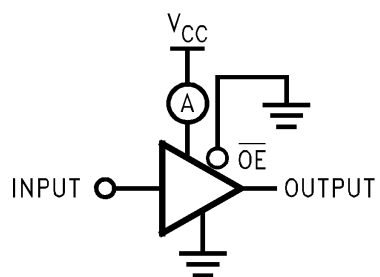
Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	Conditions	T _A =+25°C			T _A =-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95		0.75V _{CC}			0.75V _{CC}		V
		2.30 to 5.50		0.70V _{CC}			0.70V _{CC}		
V _{IL}	LOW Level Input Voltage	1.65 to 1.95				0.25V _{CC}		0.25V _{CC}	V
		2.30 to 5.50				0.30V _{CC}		0.30V _{CC}	
V _{OH}	HIGH Level Output Voltage	1.65	V _{IN} =V _{IH} , I _{OH} =-100 μA	1.55	1.65		1.55		V
		1.80		1.70	1.80		1.70		
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I _{OH} =-4 mA	1.29	1.52		1.29		
		2.30	I _{OH} =-8 mA	1.90	2.15		1.90		
		3.00	I _{OH} =-16 mA	2.40	2.80		2.40		
		3.00	I _{OH} =-24 mA	2.30	2.68		2.30		
		4.50	I _{OH} =-32 mA	3.80	4.20		3.80		
V _{OL}	LOW Level Output Voltage	1.65	V _{IN} =V _{IL} , I _{OL} =100 μA		0.00	0.10		0.00	V
		1.80			0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I _{OL} =4 mA		0.80	0.24		0.24	
		2.30	I _{OL} =8 mA		0.10	0.30		0.30	
		3.00	I _{OL} =16 mA		0.15	0.40		0.40	
		3.00	I _{OL} =24 mA		0.22	0.55		0.55	
		4.50	I _{OL} =32 mA		0.22	0.55		0.55	
I _{IN}	Input Leakage Current	0 to 5.5	0 ≥ V _{IN} ≥ 5.5 V			±1		±10	μA
I _{OZ}	3-STATE Output Leakage	0 to 5.5	V _{IN} =V _{IH} or V _{IL} 0 ≥ V _O ≥ 5.5 V			±1		±10	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5 V			1		10	μA
I _{CC}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5 V, GND			2		20	μA

The diagram illustrates the timing characteristics of a CMOS inverter. The input signal (INPUT) is a square wave with a rise time $t_r = 3 \text{ ns}$ and a fall time $t_f = 3 \text{ ns}$. The output signal (OUTPUT) is an inverted square wave with a high-level output voltage V_{OH} and a low-level output voltage V_{OL} . The propagation delay t_W is the time interval between the input signal crossing 50% and the output signal crossing 50%. The setup time t_{PLH} is the time interval from the input signal reaching 10% to the output signal reaching 50% during a low-to-high transition. The hold time t_{PHL} is the time interval from the output signal reaching 50% to the input signal reaching 10% during a high-to-low transition.



Note:

4. Input=AC Waveform; $t_r=t_f=1.8$ ns;
 PRR=10 MHz; Duty Cycle=50%.

Figure 5. I_{CCD} Test Circuit

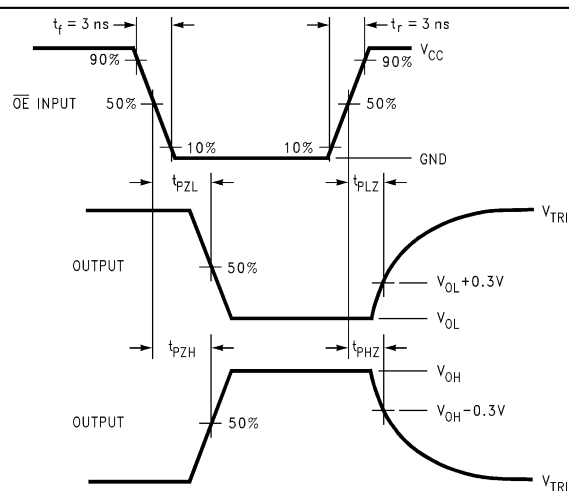


Figure 6. AC Waveforms

Physical Dimensions

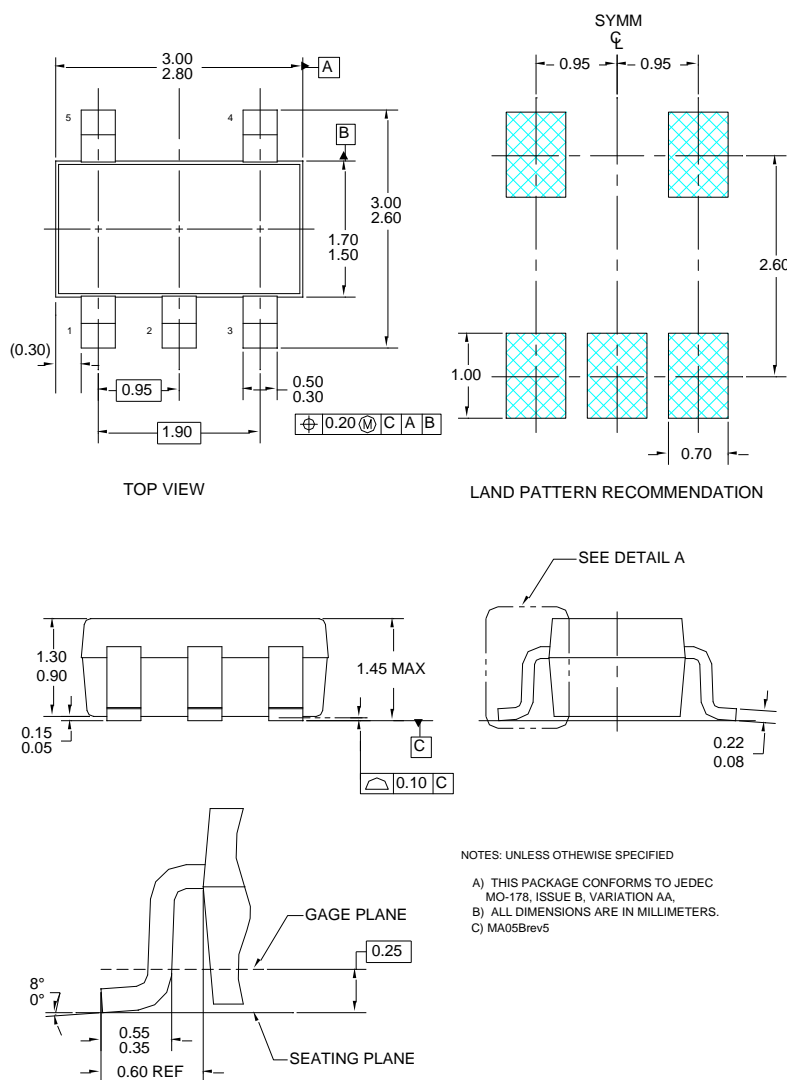


Figure 7. 5-Lead SOT23, JEDEC MO-178 1.6 mm

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Tape and Reel Specifications

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
M5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

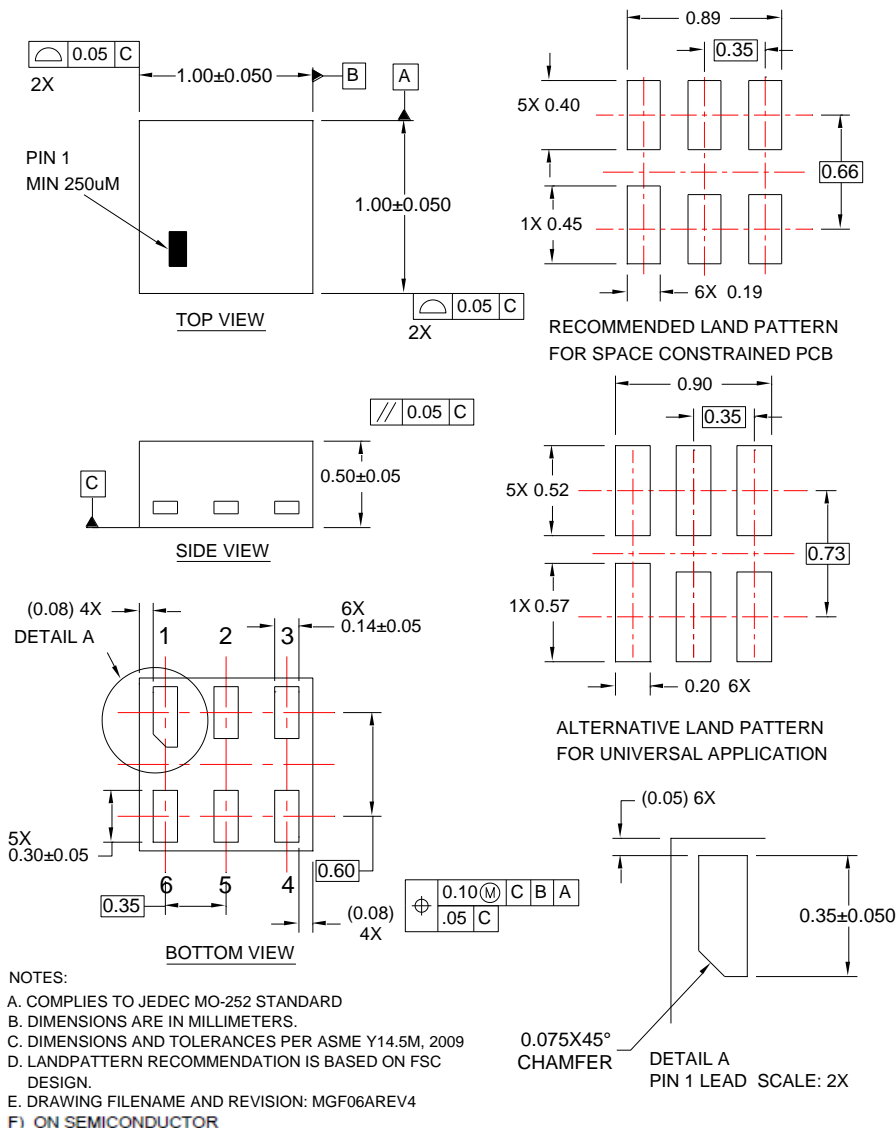


Figure 10. 6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch

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Tape and Reel Specifications

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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