32-Lane 8-Port PCIe® Gen3 System Interconnect Switch

89HPES32H8G3
Data Sheet

Device Overview

The 89HPES32H8G3 is a 32-lane, 8-port system interconnect switch optimized for PCI Express Gen3 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

- **High Performance Non-Blocking Switch Architecture**
  - 32-lane 8-port PCIe switch
    - *Seven x4 ports switch ports*
  - Integrated SerDes supports 8.0 GT/s Gen3, 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 32 GBps (256 Gbps) of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- **Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - Implements the following optional PCI Express features
    - *Advanced Error Reporting (AER) on all ports*
    - *End-to-End CRC (ECRC)*
    - *Access Control Services (ACS)*
    - *Power Budgeting Enhanced Capability*
    - *Device Serial Number Enhanced Capability*
    - *Sub-System ID and Sub-System Vendor ID Capability*
    - *Internal Error Reporting ECN*
    - *Atomic operations ECN*
    - *TLP processing hints ECN*
    - *Latency Tolerance Reporting (LTR) ECN*
    - *Optimized Buffer Flush/Fill (OBFF) ECN*
    - *ARI ECN*
    - *VGA and ISA enable*
    - *L0s and L1 ASPM*
- **Port Configurability**
  - x4 and x8 ports
    - *Ability to merge adjacent x4 ports to create a x8 port*
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Autonomous and software managed link width and speed control
  - Per lane SerDes configuration
    - *Full back channel equalization support*
    - *Rx, 5 tap DFE*
    - *Rx, single tap has pulse shaping*
    - *Rx CTLE compensates for up to 25db @ 4G/s*
    - *Tx De-emphasis*
    - *Tx pre-shoot*
    - *Programmable Drive strength*
    - *Tx Margin*
- **Switch Partitioning**
  - IDT proprietary feature that creates logically independent switches in the device
  - Supports up to 8 fully independent switch partitions
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - *Dynamic port reconfiguration — downstream, upstream*
    - *Dynamic migration of ports between partitions*
    - *Movable upstream port within and between switch partitions*
- **Initialization / Configuration**
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- **Quality of Service (QoS)**
  - Port arbitration
    - *Round robin*
  - Request metering
    - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
  - High performance switch core architecture
    - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*
- **Clocking**
  - Supports 100 MHz reference clock frequency
  - Flexible port clocking modes
    - *Common clock*
    - *Non-common clock*
    - *Local port clock with SSC and port reference clock input*
- **Hot-Plug and Hot Swap**
  - Hot-plug controller on all ports
    - *Hot-plug supported on all downstream switch ports*

- All ports support hot-plug using low-cost external SMBus I/O expanders
- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
  - *Enables SCI/SMI generation for legacy operating system support*
- Hot swap capable I/O

◆ **Power Management**

- Supports D0, D3hot and D3 power management states
- Active State Power Management (ASPM)
  - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
  - *Configurable L0s and L1 entry timers allow performance/ power-savings tuning*
- Supports PCI Express Power Budgeting Capability
- SerDes power savings
  - *Supports low swing / half-swing SerDes operation*
  - *SerDes optionally turned-off in D3hot*
  - *SerDes associated with unused ports are turned-off*
  - *SerDes associated with unused lanes are placed in a low power state*

◆ **9 General Purpose I/O**

◆ **Reliability, Availability and Serviceability (RAS)**

- ECRC support
- AER on all ports
- SECDED ECC protection on all internal RAMs
- End-to-end data path parity protection
- Checksum Serial EEPROM content protected
- Autonomous link reliability (preserves system operation in the presence of faulty links)
- Ability to generate an interrupt (INTx or MSI) on link up/down transitions

◆ **Test and Debug**

- On-die scope
- On-chip link activity and status outputs available for several ports including the upstream ports
- Per port link activity and status outputs available using external SMBus I/O expander for all remaining ports
- SerDes test modes
- Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG

◆ **Power Supplies**

- Requires three power supply voltages (1.0V, 1.8V, and 3.3V)
- No power sequencing requirements

◆ **Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express Gen3 interconnect, the PES32H8G3 provides the most efficient system interconnect switching solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 32 GBps (256 Gbps) of aggregated, full-duplex switching capacity through 32 integrated serial lanes, using proven and robust IDT technology. Each lane is capable of 8 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base specification 3.0.

The PES32H8G3 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 3.0. The PES32H8G3 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES32H8G3 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES32H8G3 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES32H8G3 configuration.

Block Diagram

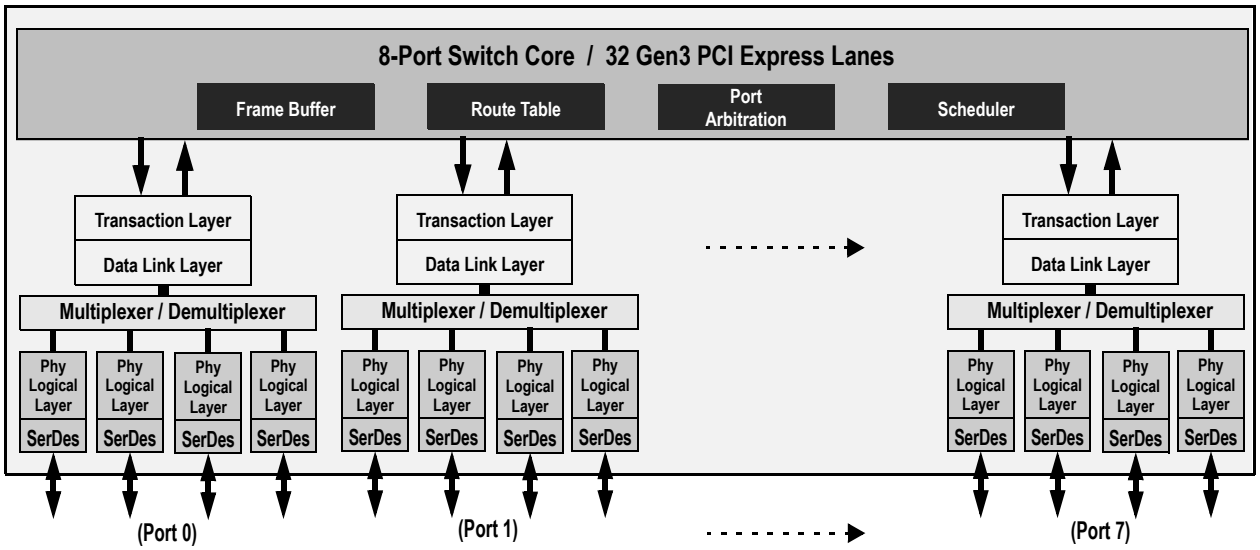


Figure 2 Internal Block Diagram

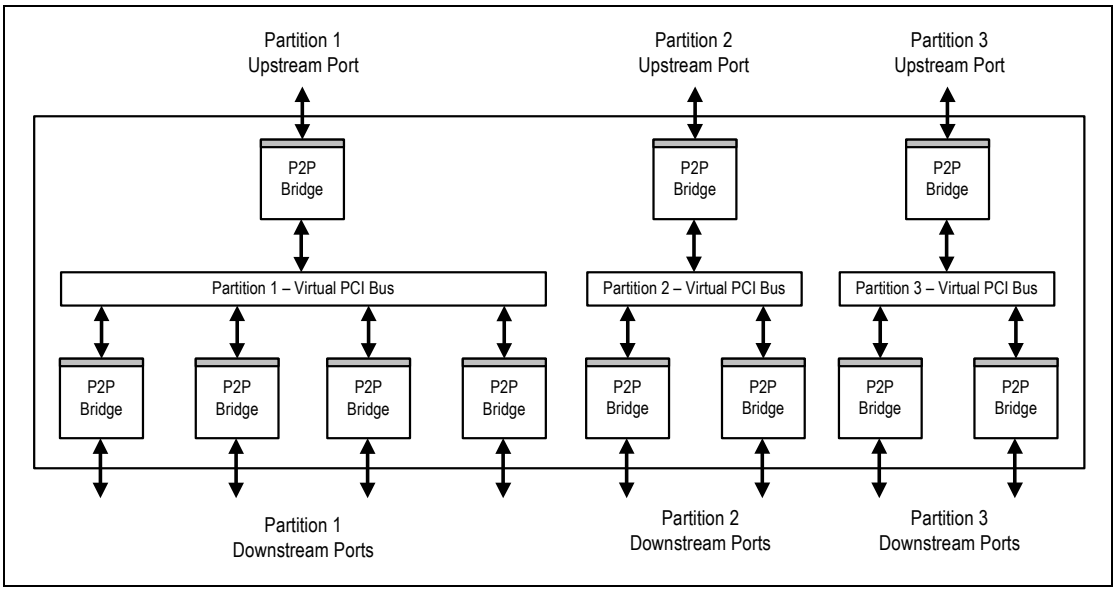


Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES32H8G3 contains an SMBus master interface. This master interface allows the default configuration register values of the PES32H8G3 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Two pins make up the SMBus master interface: an SMBus clock pin and an SMBus data pin. Four pins make up the SMBus slave interface: an SMBus clock pin and an SMBus data pin plus two address pins, SSMBADDR[2,1]. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	0
2	SSMBADDR[2]	0
3	1	0
4	0	0
5	1	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment

As shown in Figure 2, the master and slave SMBuses may only be used in a split configuration.

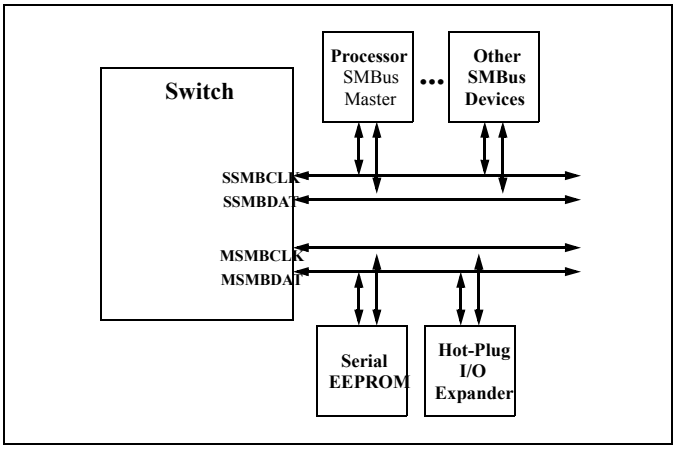


Figure 2 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES32H8G3 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES32H8G3 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32H8G3 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES32H8G3. In response to an I/O expander interrupt, the PES32H8G3 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES32H8G3 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES32H8G3. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE00RP[3:0] PE00RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TP[3:0] PE00TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RP[3:0] PE01RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7.
PE01TP[3:0] PE01TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7.
PE02RP[3:0] PE02RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TP[3:0] PE02TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RP[3:0] PE03RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7.
PE03TP[3:0] PE03TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7.
PE04RP[3:0] PE04RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TP[3:0] PE04TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RP[3:0] PE05RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
PE05TP[3:0] PE05TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7.
PE06RP[3:0] PE06RN[3:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE06TP[3:0] PE06TN[3:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE07RP[3:0] PE07RN[3:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7.
PE07TP[3:0] PE07TN[3:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7.

Table 2 PCI Express Interface Pins (Part 2 of 2)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pairs. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is 100MHz. Note: Both pairs of the Global Reference Clocks must be connected to and derived from the same clock source. Refer to the Overview section of Chapter 3 in the PES32H8G3 User Manual for additional details.
P[2:0]CLKN P[2:0]CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with ports 0, 1, and 2.[1]

Table 3 Reference Clock Pins

1. Unused port clock pins should be connected to Vss on the board.

Signal	Type	Name/Description
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[2,1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition.
GPIO[4]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[8]	I	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt.

Table 5 General Purpose I/O Pins

Signal	Type	Name/Description
CLKMODE[2:0]		**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
P67MERGEN	I	**Port 6 and 7 Merge.** P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port.
PERSTN	I	**Global Reset.** Assertion of this signal resets all logic inside PES32H8G3.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES32H8G3 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the PES32H8G3 switch operating mode. **Note:** These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition with port 0 selected as the upstream port 0x1 - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (i.e., port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (i.e., port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (i.e., port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (i.e., port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved

Table 6 System Pins

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 7 Test Pins

Signal	Type	Name/Description
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic (1.0V).
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply (3.3V).
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (1.8V).
V_{SS}	I	Ground.

Table 8 Power and Ground Pins

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any of these pins left floating can cause a slight increase in power consumption. Finally, unused Serdes (Rx and Tx) pins should be left floating.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[3:0]	I	PCIe Differential[2]	Serial Link		
	PE00RP[3:0]	I				
	PE00TN[3:0]	O				
	PE00TP[3:0]	O				
	PE01RN[3:0]	I				
	PE01RP[3:0]	I				
	PE01TN[3:0]	O				
	PE01TP[3:0]	O				
	PE02RN[3:0]	I				
	PE02RP[3:0]	I				
	PE02TN[3:0]	O				
	PE02TP[3:0]	O				
	PE03RN[3:0]	I				
	PE03RP[3:0]	I				
	PE03TN[3:0]	O				
	PE03TP[3:0]	O				
	PE04RN[3:0]	I				
	PE04RP[3:0]	I				
	PE04TN[3:0]	O				
	PE04TP[3:0]	O				
	PE05RN[3:0]	I				
	PE05RP[3:0]	I				
	PE05TN[3:0]	O				
	PE05TP[3:0]	O				
	PE06RN[3:0]	I				
	PE06RP[3:0]	I				
	PE06TN[3:0]	O				
	PE06TP[3:0]	O				
	PE07RN[3:0]	I				
	PE07RP[3:0]	I				
	PE07TN[3:0]	O				
	PE07TP[3:0]	O				

Table 9 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (Cont.)	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 16
	GCLKP[1:0]	I				
	P00CLKN, P00CLKP	I				
	P01CLKN, P01CLKP	I				
	P02CLKN, P02CLKP	I				
SMBus	MSMBCLK	I/O	LVTTL	STI[3]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[2:1]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	STI, High Drive	pull-up	
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	
	CLKMODE[2]	I			pull-down	
	P01MERGEN	I			pull-down	
	P23MERGEN	I			pull-down	
	P45MERGEN	I			pull-down	
	P67MERGEN	I			pull-down	
	PERSTN	I		STI		
	RSTHALT	I		Input	pull-down	
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	

Table 9 Pin Characteristics (Part 2 of 2)

1. Internal resistor values for pull-up and pull-down are in the range 27K – 34KΩ with 30KΩ being typical.
2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
3. Schmitt Trigger Input (STI).

Logic Diagram — PES32H8G3

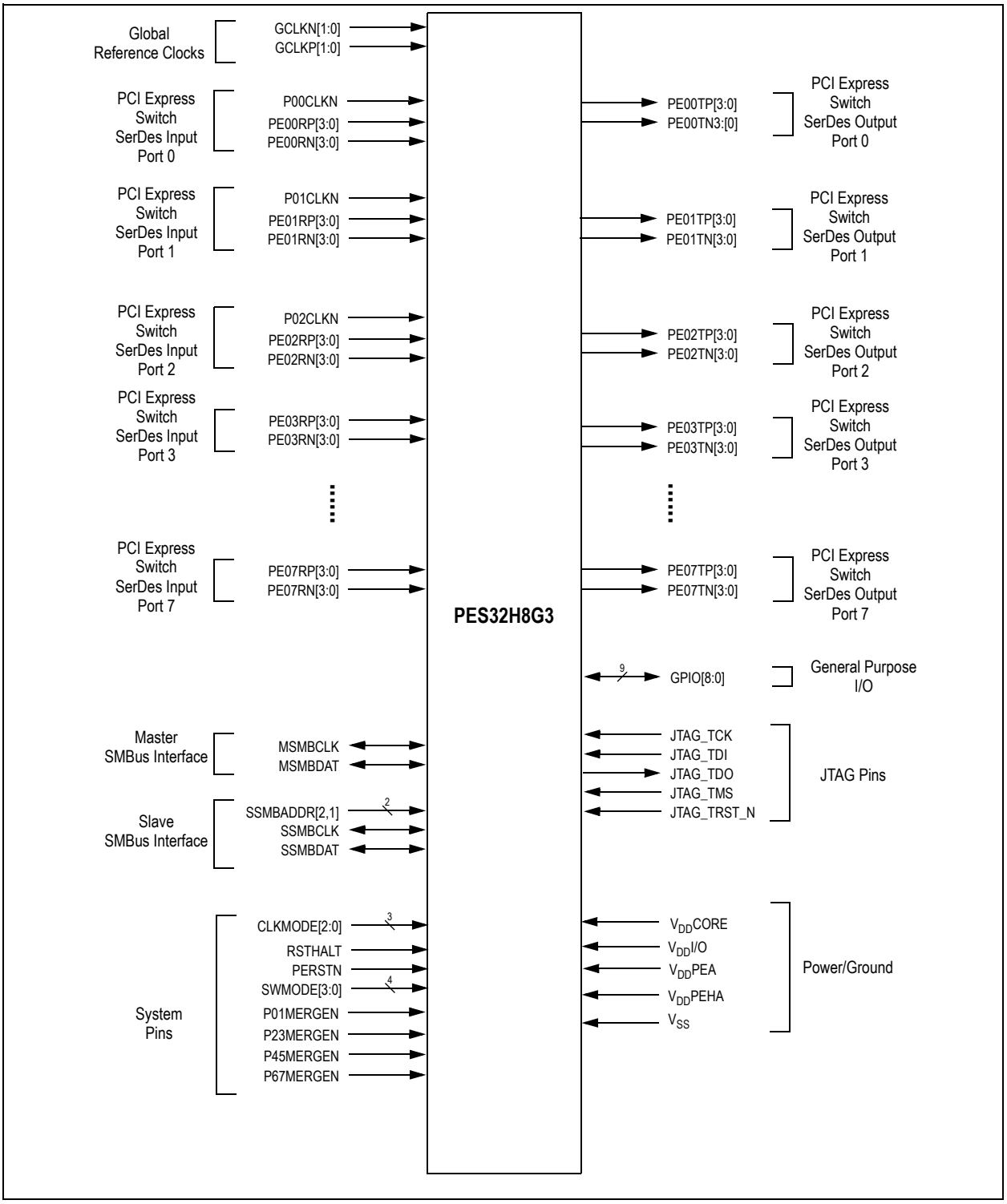


Figure 2 PES32H8G3 Logic Diagram

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 10 PES32H8G3 Operating Temperatures

Thermal Considerations

This section describes thermal considerations for the PES32H8G3 (23mm^2 FCBGA484 package). The data in Table 11 below contains information that is relevant to the thermal performance of the PES32H8G3 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum for commercial-rated products
		85	°C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	11.7	°C/W	Zero air flow
		7.7	°C/W	1 m/S air flow
		6.3	°C/W	2 m/S air flow
		5.5	°C/W	3 m/S air flow
		5.1	°C/W	4 m/S air flow
		4.9	°C/W	5 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	2.7	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	°C/W	
P	Power Dissipation of the Device	13.04	Watts	Maximum

Table 11 Thermal Specifications for PES32H8G3, 23x23 mm FCBGA484 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 11. Consequently, the effective junction to ambient thermal resistance (q_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$q_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired q_{JA} becomes a known entity to the system designer. How to achieve the desired q_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of q_{JC} (value provided in Table 11), thermal resistance of the chosen adhesive (q_{CS}), that of the heat sink (q_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range V_{DD}CORE	–0.5 to 1.35	V
Supply voltage range V_{DD}PEA	–0.5 to 1.35	V
Supply voltage range V_{DD}PEHA	–0.5 to 2.5	V
Supply voltage range V_{DD}I/O	–0.5 to 4.0	V
Voltage range Differential I/O	–0.5 to V_{DD}PEHA +0.5	V
3.3V Control IO	–0.5 to V_{DD}I/O + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±200	V
Storage ambient temperature	-55 to 150	°C

Table 12 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Description	Min	Typical	Max	Unit
Power-Supply Pin Requirements					
V_{DD}CORE	1.0V DC digital core supply voltage	0.95	1.0	1.1	V
V_{DD}PEA[1]	1.0V DC analog supply voltage	0.95	1.0	1.1	V
V_{DD}PEHA[2]	1.8V DC analog high supply voltage	1.71	1.8	1.98	V
V_{DD}I/O	3.3V DC supply voltage for SMBus/JTAG/IO	3.0	3.3	3.6	V

Table 13 Recommended Operating Conditions

1. V_{DD}PEA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.8V nominal DC value.

Power-Up/Power-Down Sequence

There are no power-up or power-down sequence requirements for the various operating supply voltages for this device. Therefore, power supplies can be ramped up and ramped down in any order.

Power Consumption

Table 14 below lists power consumption values under typical and maximum operating conditions.

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 1.8V	Max 1.98V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/8/8/8 (Full Swing)	mA	4150	6225	2384	2742	1248	1435	72	94		
	Watts	4.15	6.85	2.38	3.02	2.25	2.84	0.24	0.34	9.02	13.04

Table 14 PES32H8G3 Power Consumption

Note 1: The above power consumption assumes that all ports are functioning at Gen3 (8.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA and V_{DD}PEHA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above two power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 2: Using a port in Gen2 mode (5.0GT/S) results in approximately TBD % power savings for each power rail: V_{DD}PEA and V_{DD}PEHA.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately TBD % power savings for each power rail: V_{DD}PEA and V_{DD}PEHA.

Note 4: Tc (max case temp): 100°C.

DC Specifications

Parameter	Description	Min	Typical	Max	Unit
3.3V I/O Requirements					
V_{IL_VDDIO}	Digital Input Signal Voltage Low Level	-0.3	—	0.8	V
V_{IH_VDDIO}	Digital Input Signal Voltage High Level	2.1	—	V_{DD}I/O + 0.3	V
$V_{OL\_VDDIO\_HP}$	Digital Output Signal Voltage Low Level, High Power, IOL=4mA[1,2]	—	—	0.4	V
$V_{OL\_VDDIO\_LP}$	Digital Output Signal Voltage Low Level, Low Power, IOL=350uA	—	—	0.4	V
V_{HYS_VDDIO}	Hysteresis of Schmitt Trigger Input	0.1	—	—	V

Table 15 DC Specification

1. VOL low power and high power state is controlled via an external pull-up design in the end-application.

2. Applies to JTAG input pins.

Clock Specifications

The PES32H8G3 includes differential input clock buffers which are compatible with HCSL-type drivers and are designed to work with IDT standard 100 MHz PCIe reference clock generator devices (for information on IDT's Clock/Timing products, contact www.idt.com/go/clockhelp).

The standard 100 MHz PCIe input reference clock electrical specifications are shown in Table 16.

Parameter	Description	100 MHz Input		Unit
		Min	Max	
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150		mV
V_{IL}	Differential Input Low Voltage		-150	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSSDELTA}$	Variation of Vcross over all rising clock edges		+140	mV
V_{RS}	Ring-back voltage margin	-100	+100	mV
V_{STABLE}	Time before V_{RS} is allowed	500		ps
$V_{PERIODAVG}$	Average Clock Period Accuracy	-300	+2800	ppm
$V_{PERIODABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps
V_{MAX}	Absolute Max input voltage		+1.15	V
V_{MIN}	Absolute Min input voltage		-0.3	V
Duty Cycle	Duty Cycle	40	60	%
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%
Z_{C-DC}	Clock source DC impedance	40	60	W

Table 16 Input Reference Clock Buffer Electrical Specifications

AC Electrical Specifications

Note: For the tables in this section, please refer to PCI Express Base Specification 3.0 for setup and measurement conditions.

PCI Express Transmitter Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
BW_{TX-PLL}	Tx PLL BW for 2.5 GT/s	1.5	22	—	—	—	—	MHz	
$BW_{TX-PKG-PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL1}$ specified below.	—	—	8	16	2	4	MHz	
$BW_{TX-PKG-PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$ specified below.	—	—	5	16	2	5	MHz	
$PKG_{TX-PLL1}$	Tx PLL peaking	—	—	—	3.0	—	2.0	dB	
$PKG_{TX-PLL2}$	Tx PLL peaking	—	—	—	1.0	—	1.0	dB	

Table 17 PLL Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0. Note that the values in this table apply to both Tx and Rx since both use the same PLL.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8	1.2	0.8	1.2	See $V_{TX-FS-NO-EQ}$ in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		>1.8		>1.8		Absolute maximum swing value across all possible register settings.
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	0.4	1.2	0.4	1.2	See $V_{TX-RS-NO-EQ}$ in Table 21		VPP	Defined by register settings in compliance with PCI Express Specification.
			1.8		1.8		1.8		Absolute maximum swing value across all possible register settings.
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio	2.5	4.5	2.5	4.5	See Table 21		dB	Programmable over a wide range with included registers.
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level	5.0	7.0	5.0	7.0	See Table 21		dB	Programmable over a wide range with included registers.
$V_{TX-CM-AC-PP}$	Tx AC peakpeak common mode voltage (5.0 GT/s)	—	—	—	150	—	150	mVPP	

Table 18 Transmitter Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{TX-CM-AC-P}$	Tx AC peak common mode voltage (2.5 GT/s)	20	20	—	—	—	—	mV	
$I_{TX-SHORT}$	Transmitter short-circuit current limit	—	90	—	90	—	90	mA	
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	3.6	0	3.6	0	3.6	V	
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	100	0	100	0	100	mV	
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	25	0	25	0	25	mV	
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0	20	0	20	0	20	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	—	—	0	5	0	5	mV	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	600	—	600	—	600	mV	

Table 18 Transmitter Voltage and Current Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—	—	0.9	—	See Table 21		UI	
T_{TX-EYE}	Transmitter Eye including all jitter sources	0.75	—	0.75	—	See Table 21		UI	
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and max deviation from the median	—	0.125	—	—	—	—	UI	
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	See Table 21		UI	
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5 MHz	—	—	—	3.0	See Table 21		ps RMS	
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	—	—	—	0.1	—	—	UI	
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	20	—	20	—	20	—	ns	

Table 19 Transmitter Timing and Jitter Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an EIOS	—	8	—	8	—	8	ns	
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving Electrical Idle	—	8	—	8	—	8	ns	
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	500 ps + 2 UI	—	500 ps + 4 UI	—	500 ps + 6 UI	ps	

Table 19 Transmitter Timing and Jitter Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$T_{RES-ISI-5GBPS}$	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 60-inch FR4 trace at 5Gbps	—	—	—	0.25	—		UI_{pkpk}	
$T_{RES-ISI-8GBPS}$	Residual Deterministic ISI Jitter at output pins after a signal has passed through a 40-inch FR4 trace at 8Gbps	—	—	—	—	—	0.25	UI_{pkpk}	
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz	—	8 for >1.25 - 2.5GHz	—		
						4 for 2.5 - 4GHz	—		
RL_{TX-CM}	Tx package plus Si common mode return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
						3 for 2.5GHz - 4GHz	—		
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	80	120	—	120	—	120	Ω	
C_{TX}	AC Coupling Capacitor	75	265	75	265	176	265	nF	

Table 20 Miscellaneous Transmitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen3 8.0GT/s		Unit	Notes
		Min[1]	Max[1]		
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEq	800	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See $V_{TX-DIFF-PP}$ in Table 18 for absolute maximum swing value.
$V_{TX-RS-NO-EQ}$	Reduced swing Tx voltage with no TxEq	—	1300	mVPP	Defined by register settings in compliance with PCI Express Specification. See $V_{TX-DIFF-PP-LOW}$ in Table 18 for absolute maximum swing value.
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250	—	mVPP	Programmable over a wide range with included registers.
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232	—	mVPP	Programmable over a wide range with included registers.
$V_{TX-BOOST-FS}$	Tx boost ratio for full swing	8.0	—	dB	Programmable over a wide range with included registers.
$V_{TX-BOOST-RS}$	Tx boost ratio for reduced swing	2.5	—	dB	Programmable over a wide range with included registers.
T_{TX-UTJ}	Tx uncorrelated total jitter	—	31.25	ps PP @ 10^{-12}	
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	—	12	ps PP	
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	—	24	ps PP @ 10^{-12}	
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	—	10	ps PP	
T_{TX-DDJ}	Data dependent jitter	—	18	ps PP	
$EQ_{TX-COEFF-RES}$	Tx coefficient resolution	1/63	1/24	N/A	
$ps21_{TX}$	Pseudo package loss	-3.0	—	dB	
Preshoot_3.5dB	Preshoot (P7, P8, P9)	2.5	4.5	dB	
Preshoot_1.9dB	Preshoot (P5)	0.9	2.9	dB	
Preshoot_2.5dB	Preshoot (P6)	1.5	3.5	dB	
Deemphasis_3.5dB	Deemphasis (P1, P8)	2.5	4.5	dB	
Deemphasis_6dB	Deemphasis (P0, P7)	4.5	7.5	dB	
Deemphasis_2.5dB	Deemphasis (P3)	1.5	3.5	dB	
Deemphasis_4.4dB	Deemphasis (P2)	2.9	5.9	dB	

Table 21 Gen3-specific Transmitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen2 5.0 GT/s		Unit	Notes
		Min[1]	Max[1]		
UI	Unit interval without SSC	199.94	200.06	ps	
$T_{RX-HF-RMS}$	1.5 – 100 MHz RMS jitter	—	4.2	ps RMS	
$T_{RX-HF-DJ-DD}$	Max Dj impinging on Rx under tolerancing	—	88	ps	
$T_{RX-LF-RMS}$	10 kHz to 1.5 MHz RMS jitter	—	8.0	ps RMS	
$T_{RX-MIN-PULSE}$	Minimum single pulse applied at Rx	120	—	ps	
$V_{RX-MIN-MAXRATIO}$	Min/max pulse voltage ratio seen over an time interval of 2 UI	—	5		
V_{RX-EYE}	Receive eye voltage opening	100	—	mVPP diff	
$V_{RX-CM-CH-SRC}$	Common mode noise from Rx	—	300	mVPP	

Table 22 Gen 2 Tolerancing Limits for Data Clocked Rx Architecture

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

PCI Express Receiver Specifications

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-peak voltage for data clocked Rx architecture	0.175	1.2	0.100	1.2	0.175	2.0	V	
		Closed eye	2.0	Closed eye	2.0	Closed eye	2.0		Extended specification of this device.
$V_{RX-MAX-MIN-RATIO}$	Min/Max pulse voltage on consecutive UI	—	—	—	5	—	—		
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	—	150	—	150	—	75 mV (EH <100 mVPP) 125 mV (EH ≥ 100 mVPP) See Table 4.22 in the PCIe Base Specification 3.0	mVP	

Table 23 Receiver Voltage and Current Specifications (Part 1 of 2)

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	175	65	175	65	175	mV	Programmable over a wide range with included registers

Table 23 Receiver Voltage and Current Specifications (Part 2 of 2)

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
UI	Unit Interval	399.88	400.12	199.94	200.06	124.96	125.03	ps	
T_{RX-EYE}	Receiver eye time opening	0.40	—	—	—	See Tables 4.22 and 4.23 in the PCIe Base Specification 3.0		UI	
$T_{RX-TJ-DC}$	Max Rx inherent timing error	—	—	—	0.34			UI	
$T_{RX-DJ-DD-DC}$	Max Rx inherent deterministic timing error	—	—	—	0.24			UI	
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Max time delta between median and deviation from median	—	0.3	—	—	—	—	UI	
$T_{RX-MIN-PULSE}$	Minimum width pulse at Rx	—	—	0.6	—	—	—	UI	
T_{RX-GND_FLOAT}	Rx termination ground float time	—	—	—	—	—	500	µs	
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	10	—	10	—	10	ms	
$L_{RX-SKEW}$	Lane to Lane input skew	—	20	—	8	—	6	ns	

Table 24 Receiver Timing and Jitter Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Parameter	Description	Gen1 2.5 GT/s		Gen2 5.0 GT/s		Gen3 8.0 GT/s		Unit	Notes
		Min[1]	Max[1]	Min[1]	Max[1]	Min[1]	Max[1]		
$RL_{RX-DIFF}$	Rx package plus Si differential return loss	10	—	10 for 0.05 - 1.25GHz	—	10 for 0.05 - 1.25GHz	—	dB	
				8 for >1.25 - 2.5GHz	—	8 for >1.25 - 2.5GHz	—		
						5 for 2.5GHz - 4GHz	—		
RL_{RX-CM}	Common mode Rx return loss	6	—	6 for 0.05 - 2.5GHz	—	6 for 0.05 - 2.5GHz	—	dB	
						5 for 2.5GHz - 4GHz	—		
Z_{RX-DC}	Receiver DC single ended impedance	40	60	40	60	—	—	Ω	
$Z_{RX-DIFF-DC}$	DC differential impedance	80	120	—	—	—	—	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input CM Input Impedance for V>0 during Reset or power down	10 k or 20 k	—	10 k or 20 k	—	10 k or 20 k	—	Ω	
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input CM Input Impedance for V < 0 during Reset or power down	1.0 k	—	1.0 k	—	1.0 k	—	Ω	

Table 25 Miscellaneous Receiver Specifications

1. Minimum and Maximum values meet the requirements under PCI Express Base Specification 3.0.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[8:0][1]	Tpw[2]	None	50	—	ns	

Table 26 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

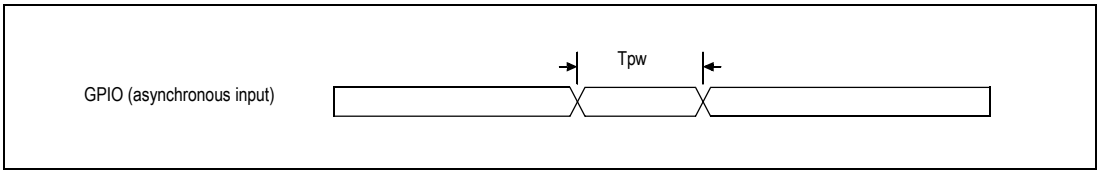


Figure 2 GPIO AC Timing Waveform

JTAG AC Timing Specifications

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 2.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 27 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

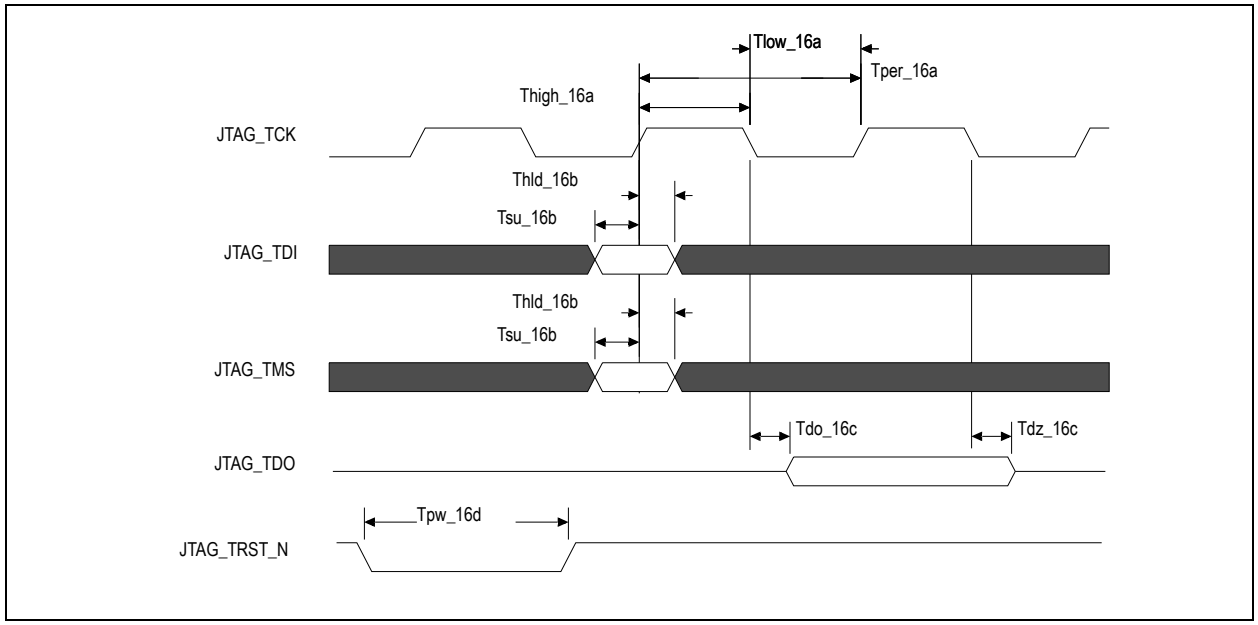


Figure 2 JTAG AC Timing Waveform

SMBus Characterization

Symbol	Parameter	Slow SMBus[1]		
		3.0V	3.3V	3.6V
DC Parameter for SDA Pin				
V_{IL}	Input Low	1.5	1.6	1.7
V_{IH}	Input High	1.6	1.7	1.9
$V_{OL@4mA}$	Output Low	245	230	220
$V_{OL@3mA}$	Output Low	185	175	165
$V_{OL@6mA}$	Output Low	380	350	330
$V_{OL@1mA}$	Output Low	65	65	65
$V_{OL@3350uA}$	Output Low	30	30	30
$I_{OL@0.4V}$		6.4	7	7.4
I_{Pullup}	Current Source	—	—	—
I_{IL_Leak}	Input Low Leakage	0	0.1	.01
I_{IH_Leak}	Input High Leakage	0	0.1	.01
DC Parameter for SCL Pin				
$V_{IL\ (V)}$	Input Low	1.5	1.6	1.7

Table 28 SMBus DC Characterization Data

Symbol	Parameter	Slow SMBus[1]		
		3.0V	3.3V	3.6V
$V_{IH\ (V)}$	Input High	1.6	1.7	1.9
I_{IL_Leak}	Input Low Leakage	0	0.1	0.1
I_{IH_Leak}	Input High Leakage	0	0.1	0.1

Table 28 SMBus DC Characterization Data

1. Data at room and hot temperature.

Symbol	Parameter	SMBus @3.3V ±10%[1]		Unit
		Min	Max	
F_{SCL}	Clock frequency	6	625	KHz
T_{BUF}	Bus free time between Stop and Start	3.7	—	µs
$T_{HD:STA}$	Start condition hold time	1.2	—	µs
$T_{SU:STA}$	Start condition setup time	1.2	—	µs
$T_{SU:STO}$	Stop condition setup time	1.2	—	µs
$T_{HD:DAT}$	Data hold time	1.2	—	ns
$T_{SU:DAT}$	Data setup time	1.2	—	ns
$T_{TIMEOUT}$	Detect clock low time out	—	74.7	ms
T_{LOW}	Clock low period	3.7	—	µs
T_{HIGH}	Clock high period	3.7	—	µs
T_F	Clock/Data fall time	—	68.4	ns
T_R	Clock/Data rise time	—	127.6	ns
$T_{POR@10kHz}$	Time which a device must be operational after power-on reset	20	—	ms

Table 29 SMBus AC Timing Data

1. Data at room and hot temperature.

PES32H8G3 Package Pinout, 23x23mm 484-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES32H8G3 (23x23mm) device. Note: NC stands for No Connection.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B5	V_{SS}		C9	V_{SS}	
A2	$V_{DD}IO$		B6	PE03TN1		C10	V_{SS}	
A3	PE03TP3		B7	PE03TN0		C11	V_{SS}	
A4	PE03TP2		B8	V_{SS}		C12	V_{SS}	
A5	V_{SS}		B9	GCLKN0		C13	V_{SS}	
A6	PE03TP1		B10	V_{SS}		C14	V_{SS}	
A7	PE03TP0		B11	PE02TN3		C15	V_{SS}	
A8	V_{SS}		B12	PE02TN2		C16	V_{SS}	
A9	GCLKP0		B13	V_{SS}		C17	V_{SS}	
A10	V_{SS}		B14	P02CLKN		C18	V_{SS}	
A11	PE02TP3		B15	V_{SS}		C19	PERSTN	
A12	PE02TP2		B16	PE02TN1		C20	JTAG_TRST_N	
A13	V_{SS}		B17	PE02TN0		C21	SSMBDAT	
A14	P02CLKP		B18	$V_{DD}IO$		C22	SSMBADDR1	
A15	V_{SS}		B19	MSMBCLK		D1	V_{SS}	
A16	PE02TP1		B20	JTAG_TMS		D2	V_{SS}	
A17	PE02TP0		B21	SSMBCLK		D3	V_{SS}	
A18	$V_{DD}IO$		B22	JTAG_TCK		D4	V_{SS}	
A19	MSMBDAT		C1	V_{SS}		D5	V_{SS}	
A20	JTAG_TDO		C2	$V_{DD}IO$		D6	V_{SS}	
A21	CLKMODE1		C3	V_{SS}		D7	PE03RN3	
A22	SSMBADDR2		C4	V_{SS}		D8	PE03RN2	
B1	V_{SS}		C5	V_{SS}		D9	NC	
B2	$V_{DD}IO$		C6	V_{SS}		D10	PE03RN1	
B3	PE03TN3		C7	V_{SS}		D11	PE03RN0	
B4	PE03TN2		C8	V_{SS}		D12	V_{SS}	

Table 30 PES32H8G3 Signal Pin-Out (Part 1 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
D13	V_{SS}		E17	PE02RP1		F21	PE01TN2	
D14	PE02RN3		E18	PE02RP0		F22	PE01TP2	
D15	PE02RN2		E19	V_{DD}PEHA		G1	PE04TP0	
D16	NC		E20	V_{SS}		G2	PE04TN0	
D17	PE02RN1		E21	PE01TN3		G3	V_{SS}	
D18	PE02RN0		E22	PE01TP3		G4	PE04RN1	
D19	V_{SS}		F1	V_{SS}		G5	PE04RP1	
D20	JTAG_TDI		F2	V_{SS}		G6	V_{DD}PEA	
D21	V_{DD}IO		F3	V_{SS}		G7	V_{SS}	
D22	V_{DD}IO		F4	PE04RN0		G8	V_{DD}CORE	
E1	V_{SS}		F5	PE04RP0		G9	V_{DD}CORE	
E2	V_{SS}		F6	V_{DD}PEHA		G10	V_{SS}	
E3	V_{SS}		F7	V_{DD}PEHA		G11	V_{DD}CORE	
E4	V_{SS}		F8	V_{DD}PEA		G12	V_{DD}CORE	
E5	V_{DD}PEHA		F9	V_{DD}PEA		G13	V_{SS}	
E6	V_{DD}PEHA		F10	V_{DD}PEA		G14	V_{DD}CORE	
E7	PE03RP3		F11	V_{DD}PEA		G15	V_{DD}CORE	
E8	PE03RP2		F12	V_{DD}PEA		G16	V_{SS}	
E9	V_{SS}		F13	V_{DD}PEA		G17	V_{DD}PEA	
E10	PE03RP1		F14	V_{DD}PEA		G18	V_{SS}	
E11	PE03RP0		F15	V_{DD}PEA		G19	V_{SS}	
E12	V_{SS}		F16	V_{DD}PEA		G20	V_{SS}	
E13	V_{SS}		F17	V_{DD}PEHA		G21	V_{SS}	
E14	PE02RP3		F18	V_{DD}PEHA		G22	V_{SS}	
E15	PE02RP2		F19	V_{DD}PEHA		H1	PE04TP1	
E16	V_{SS}		F20	V_{SS}		H2	PE04TN1	

Table 30 PES32H8G3 Signal Pin-Out (Part 2 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H3	V_{SS}		J7	V_{SS}		K11	V_{DD}CORE	
H4	NC		J8	V_{DD}CORE		K12	V_{DD}CORE	
H5	V_{SS}		J9	V_{DD}CORE		K13	V_{SS}	
H6	V_{DD}PEA		J10	V_{SS}		K14	V_{DD}CORE	
H7	V_{SS}		J11	V_{DD}CORE		K15	V_{DD}CORE	
H8	V_{DD}CORE		J12	V_{DD}CORE		K16	V_{SS}	
H9	V_{DD}CORE		J13	V_{SS}		K17	V_{DD}PEA	
H10	V_{SS}		J14	V_{DD}CORE		K18	V_{SS}	
H11	V_{DD}CORE		J15	V_{DD}CORE		K19	NC	
H12	V_{DD}CORE		J16	V_{SS}		K20	V_{SS}	
H13	V_{SS}		J17	V_{DD}PEA		K21	V_{SS}	
H14	V_{DD}CORE		J18	PE01RP2		K22	V_{SS}	
H15	V_{DD}CORE		J19	PE01RN2		L1	PE04TP3	
H16	V_{SS}		J20	V_{SS}		L2	PE04TN3	
H17	V_{DD}PEA		J21	P00CLKN		L3	V_{SS}	
H18	PE01RP3		J22	P00CLKP		L4	V_{SS}	
H19	PE01RN3		K1	PE04TP2		L5	V_{SS}	
H20	V_{SS}		K2	PE04TN2		L6	V_{DD}PEA	
H21	P01CLKN		K3	V_{SS}		L7	V_{SS}	
H22	P01CLKP		K4	PE04RN3		L8	V_{DD}CORE	
J1	V_{SS}		K5	PE04RP3		L9	V_{DD}CORE	
J2	V_{SS}		K6	V_{DD}PEA		L10	V_{SS}	
J3	V_{SS}		K7	V_{SS}		L11	V_{DD}CORE	
J4	PE04RN2		K8	V_{DD}CORE		L12	V_{DD}CORE	
J5	PE04RP2		K9	V_{DD}CORE		L13	V_{SS}	
J6	V_{DD}PEA		K10	V_{SS}		L14	V_{DD}CORE	

Table 30 PES32H8G3 Signal Pin-Out (Part 3 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
L15	V_{DD}CORE		M19	PE01RN0		P1	PE05TP1	
L16	V_{SS}		M20	V_{SS}		P2	PE05TN1	
L17	V_{DD}PEA		M21	PE01TN0		P3	V_{SS}	
L18	PE01RP1		M22	PE01TP0		P4	NC	
L19	PE01RN1		N1	PE05TP0		P5	V_{SS}	
L20	V_{SS}		N2	PE05TN0		P6	V_{DD}PEA	
L21	PE01TN1		N3	V_{SS}		P7	V_{SS}	
L22	PE01TP1		N4	PE05RN1		P8	V_{DD}CORE	
M1	V_{SS}		N5	PE05RP1		P9	V_{DD}CORE	
M2	V_{SS}		N6	V_{DD}PEA		P10	V_{SS}	
M3	V_{SS}		N7	V_{SS}		P11	V_{DD}CORE	
M4	PE05RN0		N8	V_{DD}CORE		P12	V_{DD}CORE	
M5	PE05RP0		N9	V_{DD}CORE		P13	V_{SS}	
M6	V_{DD}PEA		N10	V_{SS}		P14	V_{DD}CORE	
M7	V_{SS}		N11	V_{DD}CORE		P15	V_{DD}CORE	
M8	V_{DD}CORE		N12	V_{DD}CORE		P16	V_{SS}	
M9	V_{DD}CORE		N13	V_{SS}		P17	V_{DD}PEA	
M10	V_{SS}		N14	V_{DD}CORE		P18	PE00RP3	
M11	V_{DD}CORE		N15	V_{DD}CORE		P19	PE00RN3	
M12	V_{DD}CORE		N16	V_{SS}		P20	V_{SS}	
M13	V_{SS}		N17	V_{DD}PEA		P21	PE00TN3	
M14	V_{DD}CORE		N18	V_{SS}		P22	PE00TP3	
M15	V_{DD}CORE		N19	V_{SS}		R1	V_{SS}	
M16	V_{SS}		N20	V_{SS}		R2	V_{SS}	
M17	V_{DD}PEA		N21	V_{SS}		R3	V_{SS}	
M18	PE01RP0		N22	V_{SS}		R4	PE05RN2	

Table 30 PES32H8G3 Signal Pin-Out (Part 4 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
R5	PE05RP2		T9	V_{DD}CORE		U13	V_{DD}PEA	
R6	V_{DD}PEA		T10	V_{SS}		U14	V_{DD}PEA	
R7	V_{SS}		T11	V_{DD}CORE		U15	V_{DD}PEA	
R8	V_{DD}CORE		T12	V_{DD}CORE		U16	V_{DD}PEA	
R9	V_{DD}CORE		T13	V_{SS}		U17	V_{DD}PEHA	
R10	V_{SS}		T14	V_{DD}CORE		U18	PE00RP1	
R11	V_{DD}CORE		T15	V_{DD}CORE		U19	PE00RN1	
R12	V_{DD}CORE		T16	V_{SS}		U20	V_{SS}	
R13	V_{SS}		T17	V_{DD}PEA		U21	PE00TN1	
R14	V_{DD}CORE		T18	V_{SS}		U22	PE00TP1	
R15	V_{DD}CORE		T19	NC		V1	V_{DD}IO	
R16	V_{SS}		T20	V_{SS}		V2	V_{DD}IO	
R17	V_{DD}PEA		T21	V_{SS}		V3	V_{SS}	
R18	PE00RP2		T22	V_{SS}		V4	V_{SS}	
R19	PE00RN2		U1	PE05TP3		V5	V_{DD}PEHA	
R20	V_{SS}		U2	PE05TN3		V6	PE06RP0	
R21	PE00TN2		U3	V_{SS}		V7	PE06RP1	
R22	PE00TP2		U4	V_{SS}		V8	V_{SS}	
T1	PE05TP2		U5	V_{DD}PEHA		V9	PE06RP2	
T2	PE05TN2		U6	V_{DD}PEHA		V10	PE06RP3	
T3	V_{SS}		U7	V_{DD}PEA		V11	V_{SS}	
T4	PE05RN3		U8	V_{DD}PEA		V12	PE07RP0	
T5	PE05RP3		U9	V_{DD}PEA		V13	PE07RP1	
T6	V_{DD}PEHA		U10	V_{DD}PEA		V14	V_{SS}	
T7	V_{SS}		U11	V_{DD}PEA		V15	PE07RP2	
T8	V_{DD}CORE		U12	V_{DD}PEA		V16	PE07RP3	

Table 30 PES32H8G3 Signal Pin-Out (Part 5 of 7)

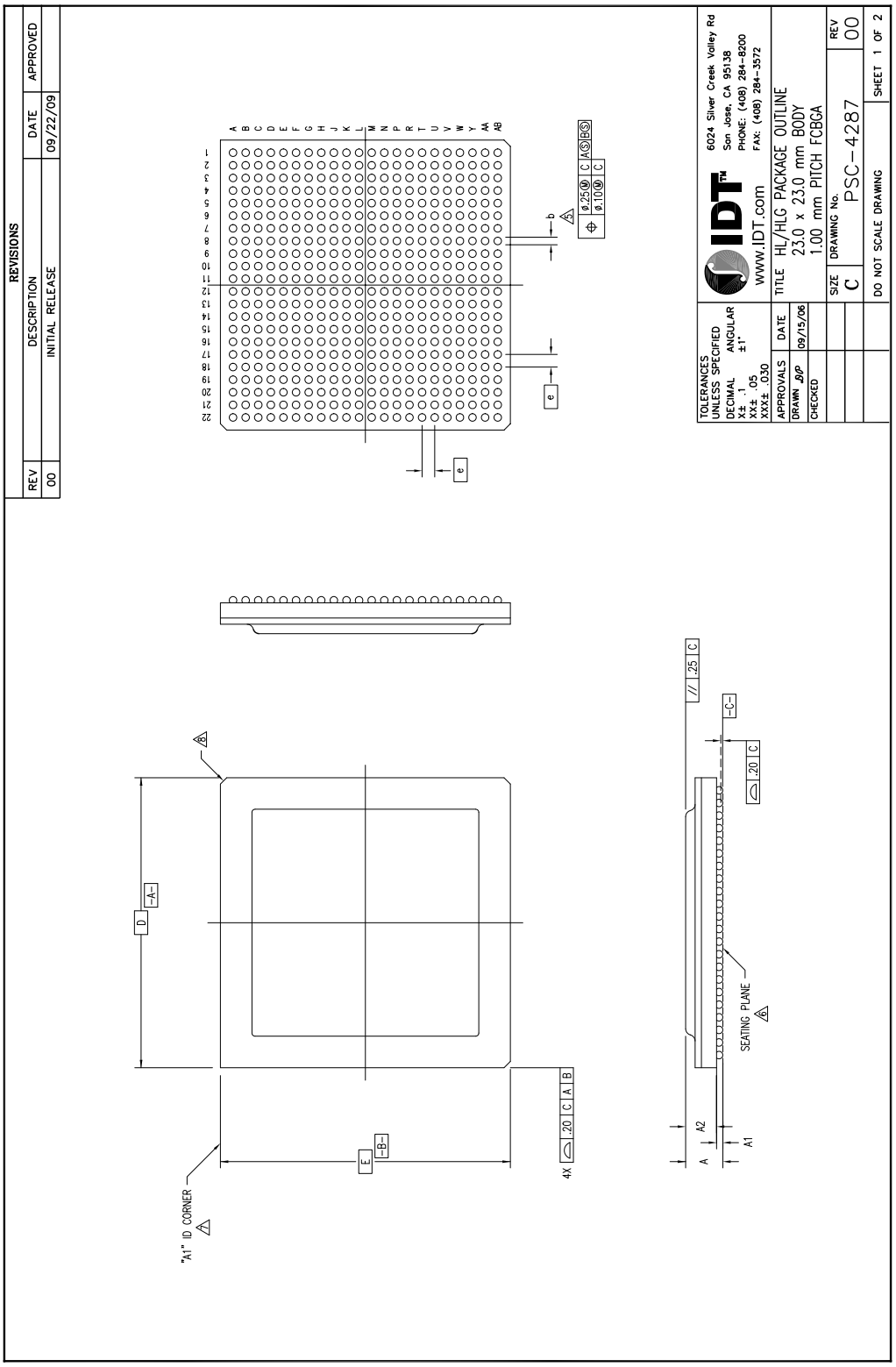
Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
V17	V_{DD}PEHA		W21	V_{DD}IO		AA3	SWMODE0	
V18	PE00RP0		W22	V_{DD}IO		AA4	V_{SS}	
V19	PE00RN0		Y1	P01MERGEN		AA5	V_{DD}IO	
V20	V_{SS}		Y2	P67MERGEN		AA6	PE06TN0	
V21	PE00TN0		Y3	CLKMODE2		AA7	PE06TN1	
V22	PE00TP0		Y4	V_{DD}IO		AA8	V_{SS}	
W1	V_{SS}		Y5	V_{SS}		AA9	PE06TN2	
W2	P23MERGEN		Y6	V_{SS}		AA10	PE06TN3	
W3	P45MERGEN		Y7	V_{SS}		AA11	V_{SS}	
W4	V_{DD}IO		Y8	V_{SS}		AA12	GCLKN1	
W5	V_{SS}		Y9	V_{SS}		AA13	V_{SS}	
W6	PE06RN0		Y10	V_{SS}		AA14	PE07TN0	
W7	PE06RN1		Y11	V_{SS}		AA15	PE07TN1	
W8	NC		Y12	V_{SS}		AA16	V_{SS}	
W9	PE06RN2		Y13	V_{SS}		AA17	PE07TN2	
W10	PE06RN3		Y14	V_{SS}		AA18	PE07TN3	
W11	V_{SS}		Y15	V_{SS}		AA19	V_{SS}	
W12	PE07RN0		Y16	V_{SS}		AA20	GPIO03	1
W13	PE07RN1		Y17	V_{SS}		AA21	GPIO04	1
W14	NC		Y18	V_{SS}		AA22	GPIO05	2
W15	PE07RN2		Y19	V_{SS}		AB1	SWMODE1	
W16	PE07RN3		Y20	GPIO06		AB2	RSTHALT	
W17	V_{DD}PEHA		Y21	GPIO07		AB3	SWMODE2	
W18	V_{DD}PEHA		Y22	GPIO08	1	AB4	SWMODE3	
W19	V_{SS}		AA1	CLKMODE0		AB5	V_{DD}IO	
W20	V_{DD}IO		AA2	NC		AB6	PE06TP0	

Table 30 PES32H8G3 Signal Pin-Out (Part 6 of 7)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AB7	PE06TP1		AB13	V_{SS}		AB19	V_{SS}	
AB8	V_{SS}		AB14	PE07TP0		AB20	GPIO00	1
AB9	PE06TP2		AB15	PE07TP1		AB21	GPIO01	1
AB10	PE06TP3		AB16	V_{SS}		AB22	GPIO02	
AB11	V_{SS}		AB17	PE07TP2				
AB12	GCLKP1		AB18	PE07TP3				

Table 30 PES32H8G3 Signal Pin-Out (Part 7 of 7)

PES32H8G3 Package Drawing — 484-Pin HL/HLG484

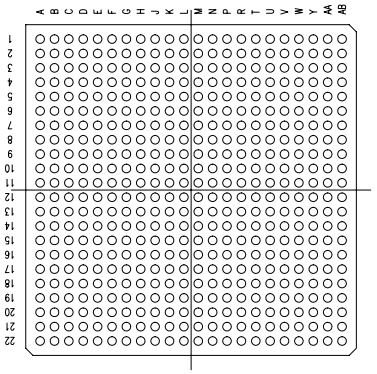


PES32H8G3 Package Drawing — Page Two

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/22/09	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS



SYMBOL	JEDEC VARIATION NONE			NOTE
	MIN	NOM	MAX	
A	–	–	2.92	
A1	–	.50	–	
A2	1.96	–	2.32	
D		23.00 BSC		
E		23.00 BSC		
M		22		3
N		484		4
e		1.00 BSC		
b	.50	.64	.70	5
CENTER BALL MATRIX		N/A		

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS	DATE
DRAWN BP	09/22/09
CHECKED	

IDT™ 6024 Silver Creek Valley Rd
www.IDT.com San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE HL/HLG PACKAGE OUTLINE
23.0 x 23.0 mm BODY
1.00 mm PITCH FCBGA

SIZE	DRAWING No.	REV
C	PSC-4287	00

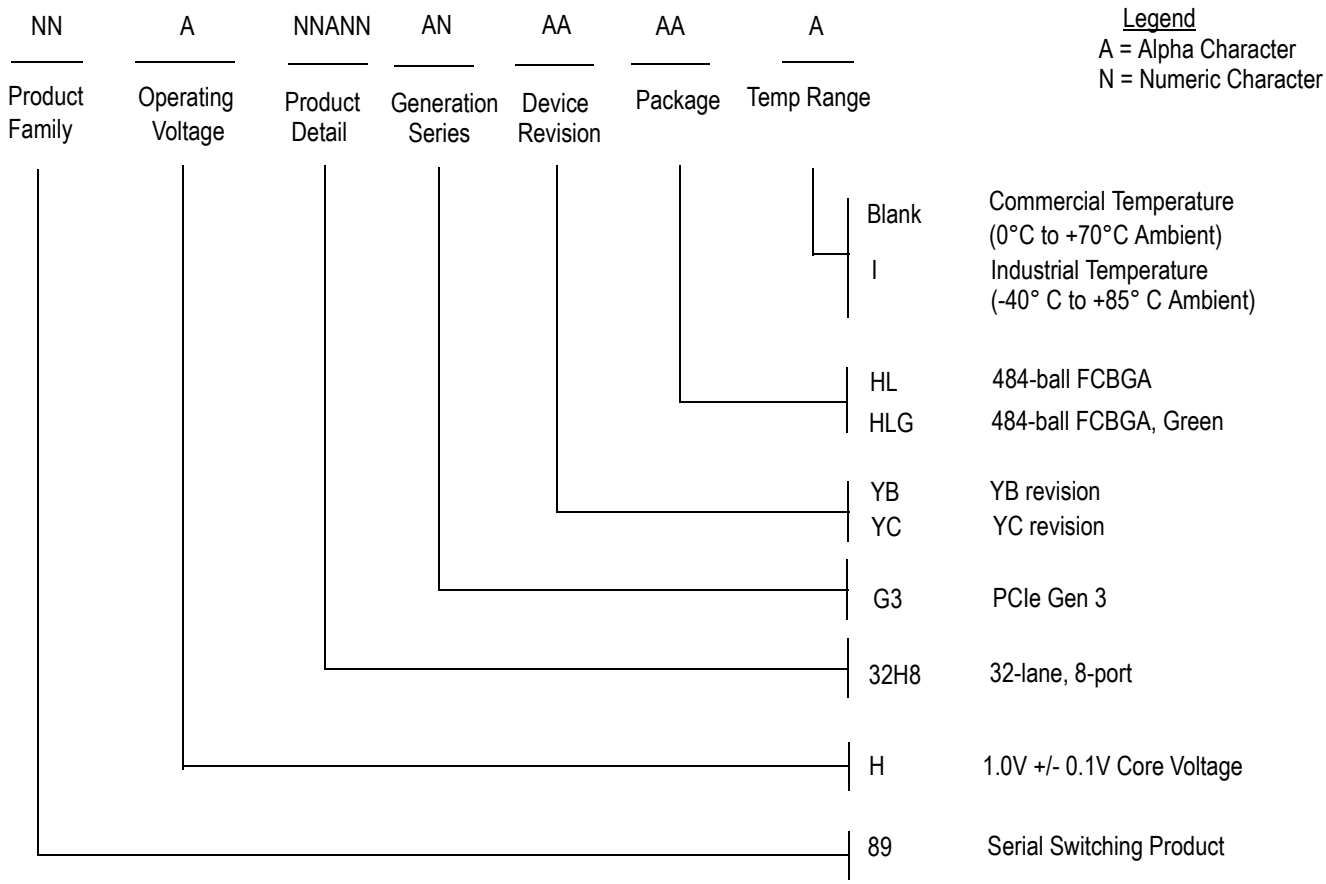
DO NOT SCALE DRAWING | SHEET 2 OF 2

Revision History

March 12, 2013: Initial publication of final data sheet.

April 17, 2013: In Power Consumption table (Table 14) footnotes, added Note #4 Tc (max case temp).

Ordering Information



Valid Combinations

89H32H8G3YBHL	484-ball FCBGA package, Commercial Temp.	89H32H8G3YCHL	484-ball FCBGA package, Commercial Temp.
89H32H8G3YBHLG	484-ball Green FCBGA package, Commercial Temp.	89H32H8G3YCHLG	484-ball Green FCBGA package, Commercial Temp.
89H32H8G3YBHLI	484-ball FCBGA package, Industrial Temp.	89H32H8G3YCHLI	484-ball FCBGA package, Industrial Temp.
89H32H8G3YBHLGI	484-ball Green FCBGA package, Industrial Temp.	89H32H8G3YCHLGI	484-ball Green FCBGA package, Industrial Temp.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: ssdhelp@idt.com
phone: 408-284-8208