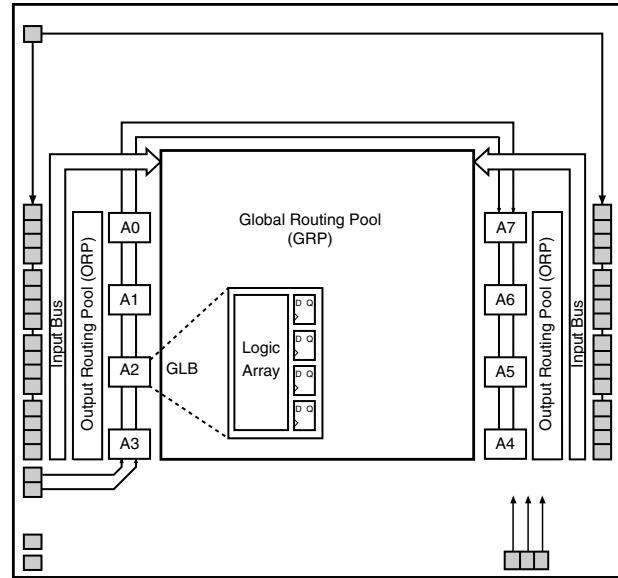




## Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 1000 PLD Gates
  - 32 I/O Pins, Two Dedicated Inputs
  - 32 Registers
  - High Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - 100% Functional, JEDEC and Pinout Compatible with ispLSI 2032V Devices
- **3.3V LOW VOLTAGE 2032 ARCHITECTURE**
  - Interfaces With Standard 5V TTL Devices
- **HIGH PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 300$  MHz Maximum Operating Frequency
  - $t_{pd} = 3.0$  ns Propagation Delay
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - 100% Tested at Time of Manufacture
  - Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - 3.3V In-System Programmability Using Boundary Scan Test Access Port (TAP)
  - Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR or Bus Arbitration Logic
  - Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - Reprogram Soldered Devices for Faster Prototyping
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAs**
  - Enhanced Pin Locking Capability
  - Three Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Programmable Output Slew Rate Control
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
  - Lead-Free Package Options

## Functional Block Diagram



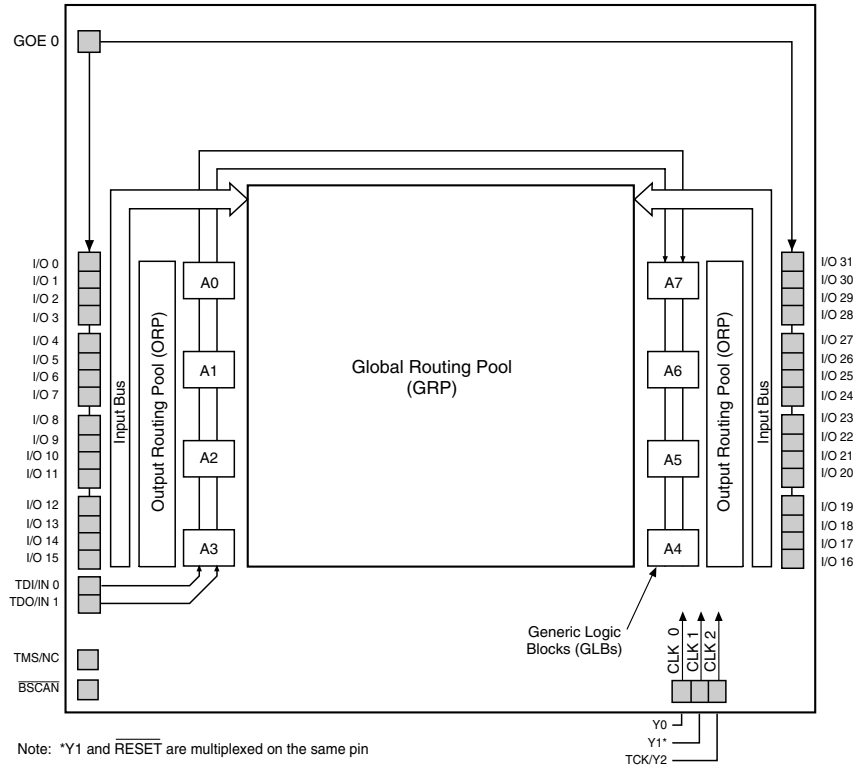
## Description

The ispLSI 2032VE is a High Density Programmable Logic Device that can be used in both 3.3V and 5V systems. The device contains 32 Registers, 32 Universal I/O pins, two Dedicated Input Pins, three Dedicated Clock Input Pins, one dedicated Global OE input pin and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2032VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2032VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2032VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. A7 (see Figure 1). There are a total of eight GLBs in the ispLSI 2032VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

**Functional Block Diagram**

**Figure 1. ispLSI 2032VE Functional Block Diagram**



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The device also has 32 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5 Volt signal levels to support mixed-voltage systems.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the ORPs. Each ispLSI 2032VE device contains one Megablock.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2032VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

**Programmable Open-Drain Outputs**

In addition to the standard output configuration, the outputs of the ispLSI 2032VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is the totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice design tools.

**Absolute Maximum Ratings <sup>1</sup>**

Supply Voltage  $V_{CC}$  ..... -0.5 to +5.4V  
 Input Voltage Applied ..... -0.5 to +5.6V  
 Off-State Output Voltage Applied ..... -0.5 to +5.6V  
 Storage Temperature ..... -65 to +150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

**DC Recommended Operating Condition**

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
$V_{CC}$	Supply Voltage	Commercial $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	3.0	3.6	V
		Industrial $T_A = -40^\circ\text{C to } +85^\circ\text{C}$	3.0	3.6	V
$V_{IL}$	Input Low Voltage		$V_{SS} - 0.5$	0.8	V
$V_{IH}$	Input High Voltage		2.0	5.25	V

Table 2-0005/2032VE

**Capacitance ( $T_A=25^\circ\text{C}$ ,  $f=1.0\text{ MHz}$ )**

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
$C_1$	Dedicated Input Capacitance	8	pf	$V_{CC} = 3.3\text{V}$ , $V_{IN} = 0.0\text{V}$
$C_2$	I/O Capacitance	6	pf	$V_{CC} = 3.3\text{V}$ , $V_{I/O} = 0.0\text{V}$
$C_3$	Clock Capacitance	10	pf	$V_{CC} = 3.3\text{V}$ , $V_Y = 0.0\text{V}$

Table 2-0006/2032VE

**Erase Reprogram Specifications**

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	–	Cycles

Table 2-0008A/2032VE

**Switching Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time 10% to 90%	≤ 1.5 ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

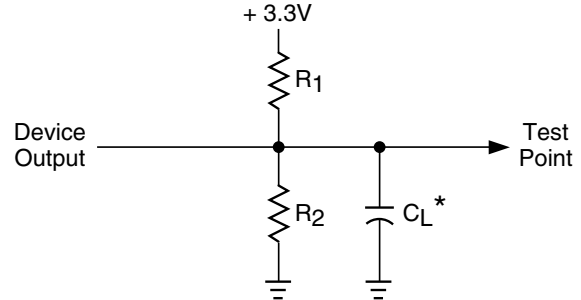
Table 2-0003/2032VE

**Output Load Conditions (see Figure 2)**

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at $V_{OH}-0.5V$	∞	348Ω	5pF
	Active Low to Z at $V_{OL}+0.5V$	316Ω	348Ω	5pF

Table 2-0004A/2032VE

**Figure 2. Test Load**



\*CL includes Test Fixture and Probe Capacitance.

0213A/2032VE

**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>V<sub>OL</sub></b>	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	–	–	0.4	V
<b>V<sub>OH</sub></b>	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	–	–	V
<b>I<sub>IL</sub></b>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (\text{Max.})$	–	–	-10	μA
<b>I<sub>IH</sub></b>	Input or I/O High Leakage Current	$(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$	–	–	10	μA
		$V_{CC} \leq V_{IN} \leq 5.25V$	–	–	10	μA
<b>I<sub>IL-isp</sub></b>	BSCAN Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>I<sub>IL-PU</sub></b>	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>I<sub>OS</sub><sup>1</sup></b>	Output Short Circuit Current	$V_{CC} = 3.3V, V_{OUT} = 0.5V$	–	–	-100	mA
<b>I<sub>CC</sub><sup>2, 4, 5</sup></b>	Operating Power Supply Current	$V_{IL} = 0.0V, V_{IH} = 3.0V$ $f_{CLOCK} = 1\text{MHz}$	-300/-225	80	–	mA
		Others	–	65	–	mA

Table 2-0007/2032VE

- One output at a time for a maximum duration of one second.  $V_{OUT} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
- Measured using two 16-bit counters.
- Typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ .
- Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .
- Unused inputs at  $V_{IL} = 0V$ .

## External Timing Parameters

### Over Recommended Operating Conditions

PARAMETER	TEST COND. <sup>3</sup>	#	DESCRIPTION <sup>1</sup>	-300		-225		UNITS
				MIN.	MAX.	MIN.	MAX.	
<b>t<sub>pd1</sub></b>	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	3.0	–	4.0	ns
<b>t<sub>pd2</sub></b>	A	2	Data Propagation Delay	–	4.5	–	6.0	ns
<b>f<sub>max</sub></b>	A	3	Clock Frequency with Internal Feedback <sup>2</sup>	300	–	225	–	MHz
<b>f<sub>max</sub> (Ext.)</b>	–	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )	208	–	154	–	MHz
<b>f<sub>max</sub> (Tog.)</b>	–	5	Clock Frequency, Max. Toggle	333	–	250	–	MHz
<b>t<sub>su1</sub></b>	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	2.0	–	2.5	–	ns
<b>t<sub>co1</sub></b>	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	2.0	–	3.0	ns
<b>t<sub>h1</sub></b>	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
<b>t<sub>su2</sub></b>	–	9	GLB Reg. Setup Time before Clock	2.8	–	3.5	–	ns
<b>t<sub>co2</sub></b>	A	10	GLB Reg. Clock to Output Delay	–	2.5	–	4.0	ns
<b>t<sub>h2</sub></b>	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
<b>t<sub>r1</sub></b>	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	4.5	–	5.0	ns
<b>t<sub>rw1</sub></b>	–	13	Ext. Reset Pulse Duration	3.0	–	3.5	–	ns
<b>t<sub>p<sub>to</sub>en</sub></b>	B	14	Input to Output Enable	–	5.0	–	7.0	ns
<b>t<sub>p<sub>to</sub>edis</sub></b>	C	15	Input to Output Disable	–	5.0	–	7.0	ns
<b>t<sub>g<sub>oe</sub>en</sub></b>	B	16	Global OE Output Enable	–	3.0	–	3.5	ns
<b>t<sub>g<sub>oe</sub>edis</sub></b>	C	17	Global OE Output Disable	–	3.0	–	3.5	ns
<b>t<sub>wh</sub></b>	–	18	External Synchronous Clock Pulse Duration, High	1.5	–	2.0	–	ns
<b>t<sub>wl</sub></b>	–	19	External Synchronous Clock Pulse Duration, Low	1.5	–	2.0	–	ns

1. Unless noted otherwise, all parameters use a GRP load of 4, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030A/2032VE  
v.0.1

**External Timing Parameters**

**Over Recommended Operating Conditions**

PARAMETER	TEST COND. <sup>3</sup>	#	DESCRIPTION <sup>1</sup>	-180		-135		-110		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	5.0	–	7.5	–	10.0	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay	–	7.5	–	10.0	–	13.0	ns
f <sub>max</sub>	A	3	Clock Frequency with Internal Feedback <sup>2</sup>	180	–	135	–	111	–	MHz
f <sub>max</sub> (Ext.)	–	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )	118	–	100	–	77.0	–	MHz
f <sub>max</sub> (Tog.)	–	5	Clock Frequency, Max. Toggle	200	–	167	–	125	–	MHz
t <sub>su1</sub>	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	3.0	–	4.0	–	5.5	–	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	4.0	–	4.5	–	5.0	ns
t <sub>h1</sub>	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	0.0	–	ns
t <sub>su2</sub>	–	9	GLB Reg. Setup Time before Clock	4.0	–	5.5	–	7.5	–	ns
t <sub>co2</sub>	A	10	GLB Reg. Clock to Output Delay	–	5.0	–	5.5	–	6.5	ns
t <sub>h2</sub>	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	0.0	–	ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	6.0	–	9.0	–	12.5	ns
t <sub>rw1</sub>	–	13	Ext. Reset Pulse Duration	4.0	–	5.0	–	6.5	–	ns
t <sub>ptoen</sub>	B	14	Input to Output Enable	–	10.0	–	12.0	–	14.5	ns
t <sub>ptoedis</sub>	C	15	Input to Output Disable	–	10.0	–	12.0	–	14.5	ns
t <sub>goeen</sub>	B	16	Global OE Output Enable	–	5.0	–	6.0	–	7.0	ns
t <sub>goedis</sub>	C	17	Global OE Output Disable	–	5.0	–	6.0	–	7.0	ns
t <sub>wh</sub>	–	18	External Synchronous Clock Pulse Duration, High	2.5	–	3.0	–	4.0	–	ns
t <sub>wl</sub>	–	19	External Synchronous Clock Pulse Duration, Low	2.5	–	3.0	–	4.0	–	ns

Table 2-0030B/2032VE  
v.0.1

1. Unless noted otherwise, all parameters use a GRP load of 4, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

## Internal Timing Parameters<sup>1</sup>

### Over Recommended Operating Conditions

PARAMETER	# <sup>2</sup>	DESCRIPTION	-300		-225		UNITS
			MIN.	MAX.	MIN.	MAX.	
<b>Inputs</b>							
<b>t<sub>io</sub></b>	20	Input Buffer Delay	–	0.4	–	0.6	ns
<b>t<sub>din</sub></b>	21	Dedicated Input Delay	–	1.0	–	1.3	ns
<b>GRP</b>							
<b>t<sub>grp</sub></b>	22	GRP Delay	–	0.6	–	0.7	ns
<b>GLB</b>							
<b>t<sub>4ptbpc</sub></b>	23	4 Product Term Bypass Path Delay (Combinatorial)	–	0.9	–	1.2	ns
<b>t<sub>4ptbpr</sub></b>	24	4 Product Term Bypass Path Delay (Registered)	–	1.1	–	1.2	ns
<b>t<sub>1ptxor</sub></b>	25	1 Product Term/XOR Path Delay	–	1.9	–	2.2	ns
<b>t<sub>20ptxor</sub></b>	26	20 Product Term/XOR Path Delay	–	1.9	–	2.2	ns
<b>t<sub>xoradj</sub></b>	27	XOR Adjacent Path Delay <sup>3</sup>	–	1.9	–	2.2	ns
<b>t<sub>gbp</sub></b>	28	GLB Register Bypass Delay	–	0.0	–	0.0	ns
<b>t<sub>gsu</sub></b>	29	GLB Register Setup Time before Clock	0.5	–	0.8	–	ns
<b>t<sub>gh</sub></b>	30	GLB Register Hold Time after Clock	1.5	–	1.7	–	ns
<b>t<sub>gco</sub></b>	31	GLB Register Clock to Output Delay	–	0.3	–	0.7	ns
<b>t<sub>gro</sub></b>	32	GLB Register Reset to Output Delay	–	1.3	–	1.3	ns
<b>t<sub>ptre</sub></b>	33	GLB Product Term Reset to Register Delay	–	2.5	–	3.2	ns
<b>t<sub>ptoe</sub></b>	34	GLB Product Term Output Enable to I/O Cell Delay	–	3.0	–	4.2	ns
<b>t<sub>ptck</sub></b>	35	GLB Product Term Clock Delay	0.4	2.3	0.5	2.8	ns
<b>ORP</b>							
<b>t<sub>orp</sub></b>	36	ORP Delay	–	0.6	–	1.3	ns
<b>t<sub>orpbp</sub></b>	37	ORP Bypass Delay	–	0.1	–	0.3	ns
<b>Outputs</b>							
<b>t<sub>ob</sub></b>	38	Output Buffer Delay	–	1.0	–	1.2	ns
<b>t<sub>sl</sub></b>	39	Output Slew Limited Delay Adder	–	2.0	–	2.0	ns
<b>t<sub>oen</sub></b>	40	I/O Cell OE to Output Enabled	–	1.0	–	1.5	ns
<b>t<sub>odis</sub></b>	41	I/O Cell OE to Output Disabled	–	1.0	–	1.5	ns
<b>t<sub>goe</sub></b>	42	Global Output Enable	–	2.0	–	2.0	ns
<b>Clocks</b>							
<b>t<sub>gy0</sub></b>	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	0.6	0.6	0.8	0.8	ns
<b>t<sub>gy1/2</sub></b>	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	0.8	0.8	1.0	1.0	ns
<b>Global Reset</b>							
<b>t<sub>gr</sub></b>	45	Global Reset to GLB	–	2.1	–	2.2	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2032VE  
v.0.1

## Internal Timing Parameters<sup>1</sup>

### Over Recommended Operating Conditions

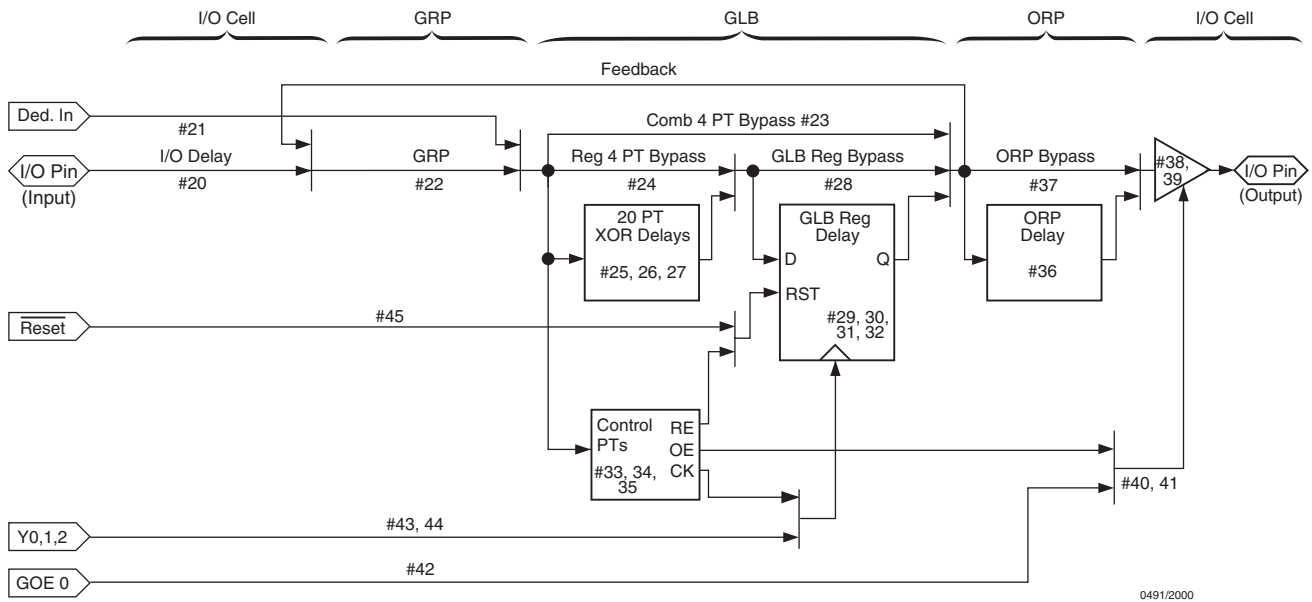
PARAMETER	# <sup>2</sup>	DESCRIPTION	-180		-135		-110		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
<b>Inputs</b>									
<b>t<sub>io</sub></b>	20	Input Buffer Delay	–	0.8	–	0.8	–	1.3	ns
<b>t<sub>din</sub></b>	21	Dedicated Input Delay	–	1.5	–	1.7	–	2.5	ns
<b>GRP</b>									
<b>t<sub>grp</sub></b>	22	GRP Delay	–	0.7	–	0.9	–	1.2	ns
<b>GLB</b>									
<b>t<sub>4ptbpc</sub></b>	23	4 Product Term Bypass Path Delay (Combinatorial)	–	1.8	–	3.9	–	4.8	ns
<b>t<sub>4ptbpr</sub></b>	24	4 Product Term Bypass Path Delay (Registered)	–	2.1	–	2.9	–	3.4	ns
<b>t<sub>1ptxor</sub></b>	25	1 Product Term/XOR Path Delay	–	3.1	–	4.4	–	5.4	ns
<b>t<sub>20ptxor</sub></b>	26	20 Product Term/XOR Path Delay	–	3.1	–	4.4	–	5.4	ns
<b>t<sub>xoradj</sub></b>	27	XOR Adjacent Path Delay <sup>3</sup>	–	3.1	–	4.4	–	5.4	ns
<b>t<sub>gbp</sub></b>	28	GLB Register Bypass Delay	–	0.2	–	1.0	–	1.4	ns
<b>t<sub>gsu</sub></b>	29	GLB Register Setup Time before Clock	0.9	–	1.1	–	1.4	–	ns
<b>t<sub>gh</sub></b>	30	GLB Register Hold Time after Clock	2.1	–	2.9	–	4.1	–	ns
<b>t<sub>gco</sub></b>	31	GLB Register Clock to Output Delay	–	0.8	–	0.9	–	1.0	ns
<b>t<sub>gro</sub></b>	32	GLB Register Reset to Output Delay	–	1.3	–	1.8	–	2.7	ns
<b>t<sub>ptre</sub></b>	33	GLB Product Term Reset to Register Delay	–	4.0	–	6.1	–	7.1	ns
<b>t<sub>ptoe</sub></b>	34	GLB Product Term Output Enable to I/O Cell Delay	–	5.7	–	6.9	–	8.6	ns
<b>t<sub>ptck</sub></b>	35	GLB Product Term Clock Delay	1.4	3.6	1.7	4.1	2.5	4.4	ns
<b>ORP</b>									
<b>t<sub>orp</sub></b>	36	ORP Delay	–	1.4	–	1.5	–	1.9	ns
<b>t<sub>orpbp</sub></b>	37	ORP Bypass Delay	–	0.4	–	0.5	–	0.9	ns
<b>Outputs</b>									
<b>t<sub>ob</sub></b>	38	Output Buffer Delay	–	1.3	–	1.4	–	1.8	ns
<b>t<sub>sl</sub></b>	39	Output Slew Limited Delay Adder	–	2.0	–	2.0	–	2.0	ns
<b>t<sub>oen</sub></b>	40	I/O Cell OE to Output Enabled	–	2.8	–	3.4	–	3.4	ns
<b>t<sub>odis</sub></b>	41	I/O Cell OE to Output Disabled	–	2.8	–	3.4	–	3.4	ns
<b>t<sub>goe</sub></b>	42	Global Output Enable	–	2.2	–	2.6	–	3.6	ns
<b>Clocks</b>									
<b>t<sub>gy0</sub></b>	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.5	1.5	1.7	1.7	1.8	1.8	ns
<b>t<sub>gy1/2</sub></b>	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.7	1.7	1.9	1.9	2.0	2.0	ns
<b>Global Reset</b>									
<b>t<sub>gr</sub></b>	45	Global Reset to GLB	–	3.0	–	5.3	–	7.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2032VE  
v.0.1



**ispLSI 2032VE Timing Model**



**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Product Term Clock**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{io} + t_{grp} + t_{20ptxor}) + (t_{gsu}) - (t_{io} + t_{grp} + t_{ptck(min)}) \\
 &= (\#20 + \#22 + \#26) + (\#29) - (\#20 + \#22 + \#35) \\
 2.0\text{ns} &= (0.4 + 0.6 + 1.9) + (0.5) - (0.4 + 0.6 + 0.4) \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gh}) - (t_{io} + t_{grp} + t_{20ptxor}) \\
 &= (\#20 + \#22 + \#35) + (\#30) - (\#20 + \#22 + \#26) \\
 1.9\text{ns} &= (0.4 + 0.6 + 2.3) + (1.5) - (0.4 + 0.6 + 1.9) \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{io} + t_{grp} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#20 + \#22 + \#35) + (\#31) + (\#36 + \#38) \\
 5.2\text{ns} &= (0.4 + 0.6 + 2.3) + (0.3) + (0.6 + 1.0)
 \end{aligned}$$

Note: Calculations are based on timing specifications for the ispLSI 2032VE-300L.

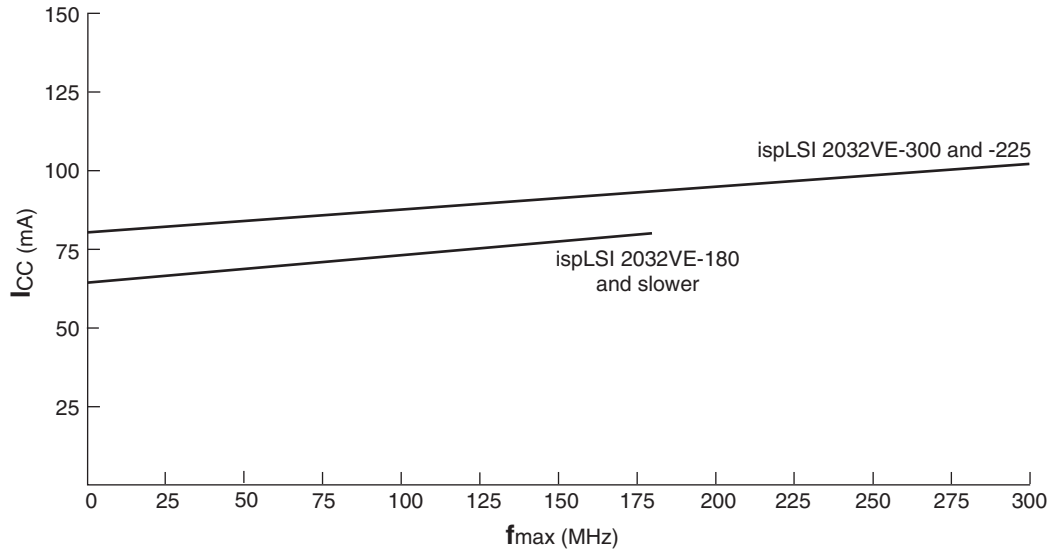
Table 2-0042/2032VE

## Power Consumption

Power consumption in the ispLSI 2032VE device depends on two primary factors: the speed at which the device is operating and the number of product terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of two 16-bit counters  
Typical current at 3.3V, 25° C

ICC can be estimated for the ispLSI 2032VE using the following equation:

For ispLSI 2032VE-300 and -225:  $I_{CC}(mA) = 4.5 + (\# \text{ of PTs} * 1.29) + (\# \text{ of nets} * F_{max} * 0.0068)$

For ispLSI 2032VE-180 and slower:  $I_{CC}(mA) = 4.5 + (\# \text{ of PTs} * 1.05) + (\# \text{ of nets} * F_{max} * 0.0068)$

Where:

# of PTs = Number of product terms used in design

# of nets = Number of signals used in device

Max freq = Highest clock frequency to the device (in MHz)

The ICC estimate is based on typical conditions ( $V_{CC} = 3.3V$ , room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

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## Signal Descriptions

Signal Name	Description
GOE 0	Global Output Enable input pin
Y0	Dedicated Clock input. This clock input is connected to one of the clock inputs of all the GLBs in the device.
RESET/Y1	This pin performs two functions: (1) Active Low (0) Reset pin which resets all of the registers in the device. (2) Dedicated Clock input.
BSCAN	Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a serial data input pin to load programming data into the device. (2) When BSCAN is high, it functions as a dedicated input pin.
TMS/NC <sup>1</sup>	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a mode control pin for the Boundary Scan state machine. (2) When BSCAN is high, this pin is not to be connected to any active signals, VCC or GND.
TDO/IN 1	Output/Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as an output pin to read serial shift register data. (2) When BSCAN is high, it functions as a dedicated input pin.
TCK/Y2	Input – This pin performs two functions. (1) When BSCAN is logic low, it functions as a clock pin for the Boundary Scan state machine. (2) When BSCAN is high, it functions as a Dedicated Clock input.
GND	Ground (GND)
VCC	Vcc
NC <sup>1</sup>	No Connect
I/O	Input/Output pins – These are the general purpose I/O pins used by the logic array.

## Signal Locations

Signal	44-Pin TQFP	44-Pin PLCC	48-Pin TQFP	49-Ball caBGA
GOE 0	40	2	43	A4
Y0	5	11	5	C1
RESET/Y1	29	35	31	D7
BSCAN	7	13	7	D1
TDI/IN 0	8	14	8	E2
TMS/NC <sup>1</sup>	30	36	32	C6
TDO/IN 1	18	24	19	G4
TCK/Y2	27	33	29	E7
GND	17, 39	1, 23	18, 42	C4, E4
VCC	6, 28	12, 34	6, 30	D3, D5
NC <sup>1</sup>	—	—	12, 24, 36, 48	A1, A7, D4, G1, G7

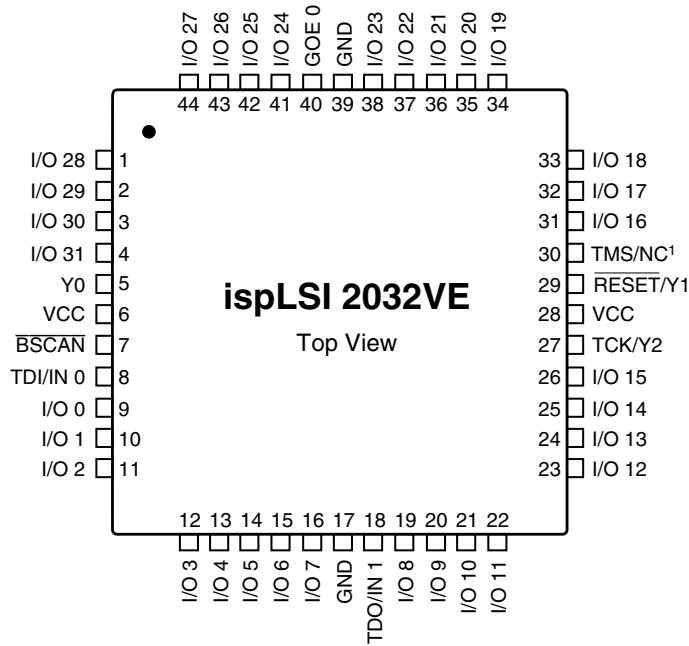
## I/O Locations

Signal	44-Pin TQFP	44-Pin PLCC	48-Pin TQFP	49-Ball caBGA
I/O 0 - I/O 6	9, 10, 11, 12, 13, 14, 15	15, 16, 17, 18, 19, 20, 21	9, 10, 11, 13, 14, 15, 16	E1, F2, F1, E3, F3, G2, F4
I/O 7 - I/O 13	16, 19, 20, 21, 22, 23, 24	22, 25, 26, 27, 28, 29, 30	17, 20, 21, 22, 23, 25, 26	G3, F5, G5, F6, G6, E5, E6
I/O 14 - I/O 20	25, 26, 31, 32, 33, 34, 35	31, 32, 37, 38, 39, 40, 41	27, 28, 33, 34, 35, 37, 38	F7, D6, C7, B6, B7, C5, B5
I/O 21 - I/O 27	36, 37, 38, 41, 42, 43, 44	42, 43, 44, 3, 4, 5, 6	39, 40, 41, 44, 45, 46, 47	A6, B4, A5, B3, A3, B2, A2
I/O 28 - I/O 31	1, 2, 3, 4	7, 8, 9, 10	1, 2, 3, 4	C3, C2, B1, D2

1. NC pins are not to be connected to any active signals, VCC or GND.

**Pin Configuration**

ispLSI 2032VE 44-Pin TQFP Pinout Diagram (0.8mm Lead Pitch/10.0 x 10.0mm Body Size)

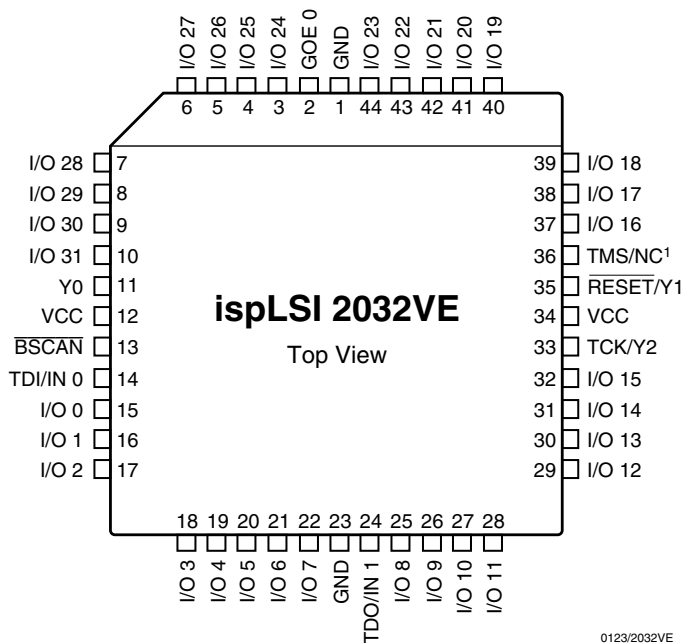


0851/2032VE

1. NC pins are not to be connected to any active signals, VCC or GND.

**Pin Configuration**

ispLSI 2032VE 44-Pin PLCC Pinout Diagram (0.5in Lead Pitch/0.65 x 0.65in Body Size)

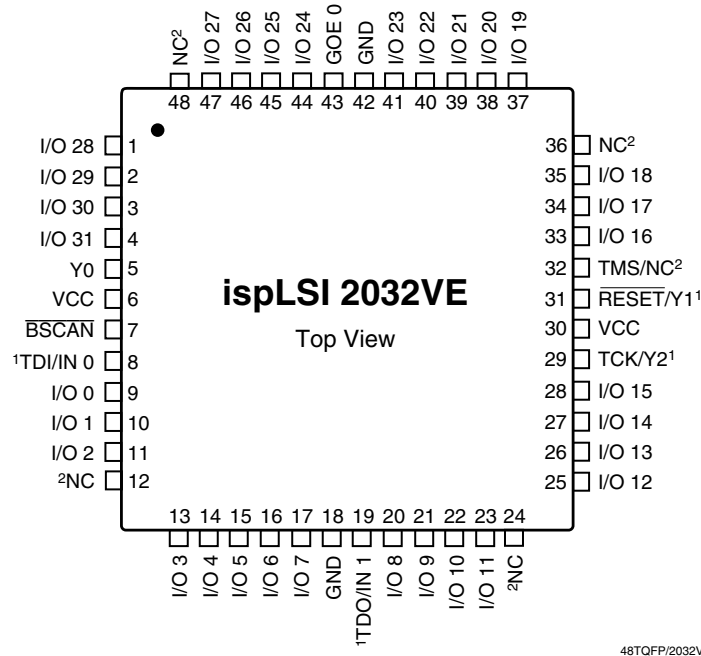


0123/2032VE

1. NC pins are not to be connected to any active signals, VCC or GND.

**Pin Configuration**

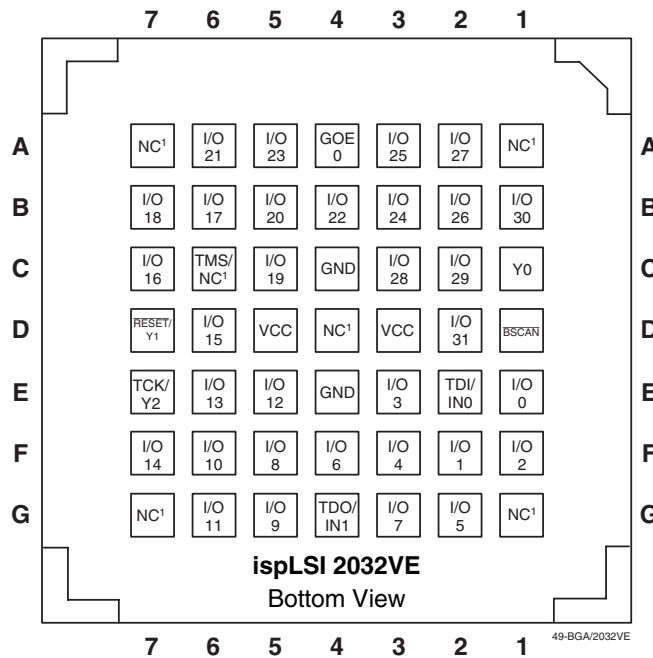
ispLSI 2032VE 48-Pin TQFP Pinout Diagram (0.5mm Lead Pitch/7.0 x 7.0mm Body Size)



1. Pins have dual function capability.
2. NC pins are not to be connected to any active signals, V<sub>CC</sub> or GND.

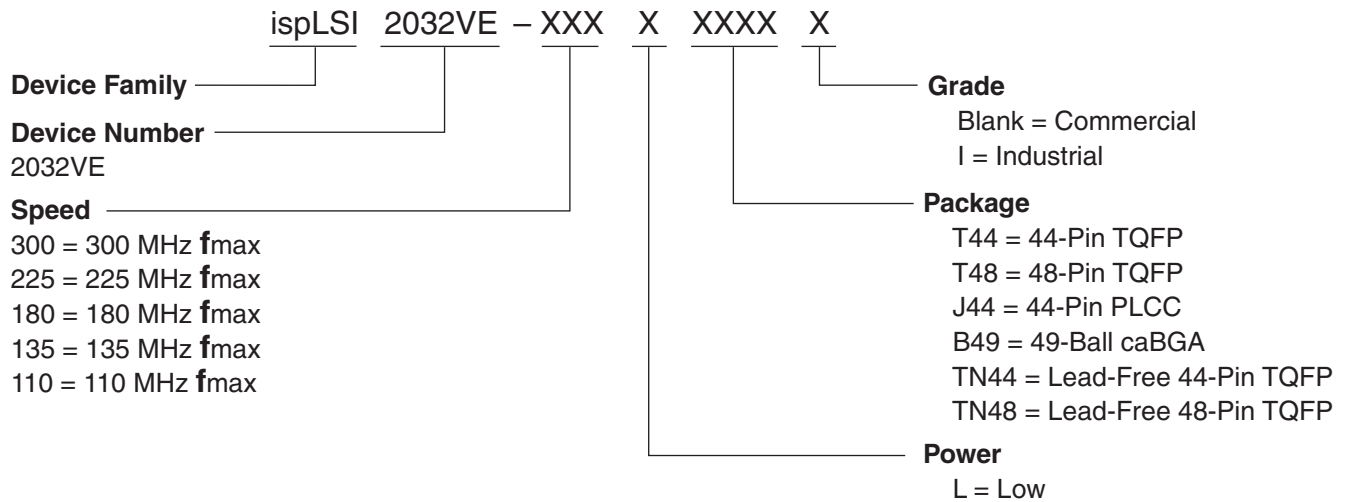
**Signal Configuration**

ispLSI 2032VE 49-Ball caBGA Signal Diagram (0.8mm Lead Pitch/7.0 x 7.0mm Body Size)



1. NCs are not to be connected to any active signals, V<sub>CC</sub> or GND.
- Note: Ball A1 indicator dot on top side of package.

## Part Number Description



## ispLSI 2032VE Ordering Information

### Conventional Packaging

### COMMERCIAL

FAMILY	f <sub>max</sub> (MHz)	t <sub>pd</sub> (ns)	ORDERING NUMBER	PACKAGE
ispLSI	300	3.0	ispLSI 2032VE-300LT44	44-Pin TQFP
	300	3.0	ispLSI 2032VE-300LT48	48-Pin TQFP
	300	3.0	ispLSI 2032VE-300LB49	49-Ball caBGA
	225	4.0	ispLSI 2032VE-225LT44*	44-Pin TQFP
	225	4.0	ispLSI 2032VE-225LT48*	48-Pin TQFP
	225	4.0	ispLSI 2032VE-225LJ44	44-Pin PLCC
	225	4.0	ispLSI 2032VE-225LB49*	49-Ball caBGA
	180	5.0	ispLSI 2032VE-180LT44	44-Pin TQFP
	180	5.0	ispLSI 2032VE-180LT48	48-Pin TQFP
	180	5.0	ispLSI 2032VE-180LJ44	44-Pin PLCC
	180	5.0	ispLSI 2032VE-180LB49	49-Ball caBGA
	135	7.5	ispLSI 2032VE-135LT44	44-Pin TQFP
	135	7.5	ispLSI 2032VE-135LT48	48-Pin TQFP
	135	7.5	ispLSI 2032VE-135LJ44	44-Pin PLCC
	135	7.5	ispLSI 2032VE-135LB49	49-Ball caBGA
	110	10	ispLSI 2032VE-110LT44	44-Pin TQFP
	110	10	ispLSI 2032VE-110LT48	48-Pin TQFP
	110	10	ispLSI 2032VE-110LJ44	44-Pin PLCC
110	10	ispLSI 2032VE-110LB49	49-Ball caBGA	

\*2032VE-300 recommended for new designs

Table 2-0041A/2032VE

### INDUSTRIAL

FAMILY	f <sub>max</sub> (MHz)	t <sub>pd</sub> (ns)	ORDERING NUMBER	PACKAGE
ispLSI	180	5.0	ispLSI 2032VE-180LT44I	44-Pin TQFP

Table 2-0041B/2032VE

**ispLSI 2032VE Ordering Information (Cont.)**
**Lead-Free Packaging**
**COMMERCIAL**

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	300	3.0	ispLSI 2032VE-300LTN44	Lead-Free 44-Pin TQFP
	300	3.0	ispLSI 2032VE-300LTN48	Lead-Free 48-Pin TQFP
	180	5.0	ispLSI 2032VE-180LTN44	Lead-Free 44-Pin TQFP
	180	5.0	ispLSI 2032VE-180LTN48	Lead-Free 48-Pin TQFP
	135	7.5	ispLSI 2032VE-135LTN44	Lead-Free 44-Pin TQFP
	135	7.5	ispLSI 2032VE-135LTN48	Lead-Free 48-Pin TQFP
	110	10	ispLSI 2032VE-110LTN44	Lead-Free 44-Pin TQFP
	110	10	ispLSI 2032VE-110LTN48	Lead-Free 48-Pin TQFP

**INDUSTRIAL**

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	180	5.0	ispLSI 2032VE-180LTN44I	Lead-Free 44-Pin TQFP

**Revision History**

Date	Version	Change Summary
—	10	Previous Lattice release.
August 2006	11	Updated for 48-pin TQFP lead-free package option.