DUAL HIGH SPEED DRIVER

DESCRIPTION

The SG1644/ SG3644 is a dual non-inverting monolithic high speed driver. This device utilizes high voltage Schottky logic to convert TTL signals to high speed outputs up to 18V. The totem pole outputs have 3A peak current capability, which enables them to drive 1000pF loads in typically less than 25ns. These speeds make it ideal for driving power MOSFETs and other large capacitive loads requiring high speed switching.

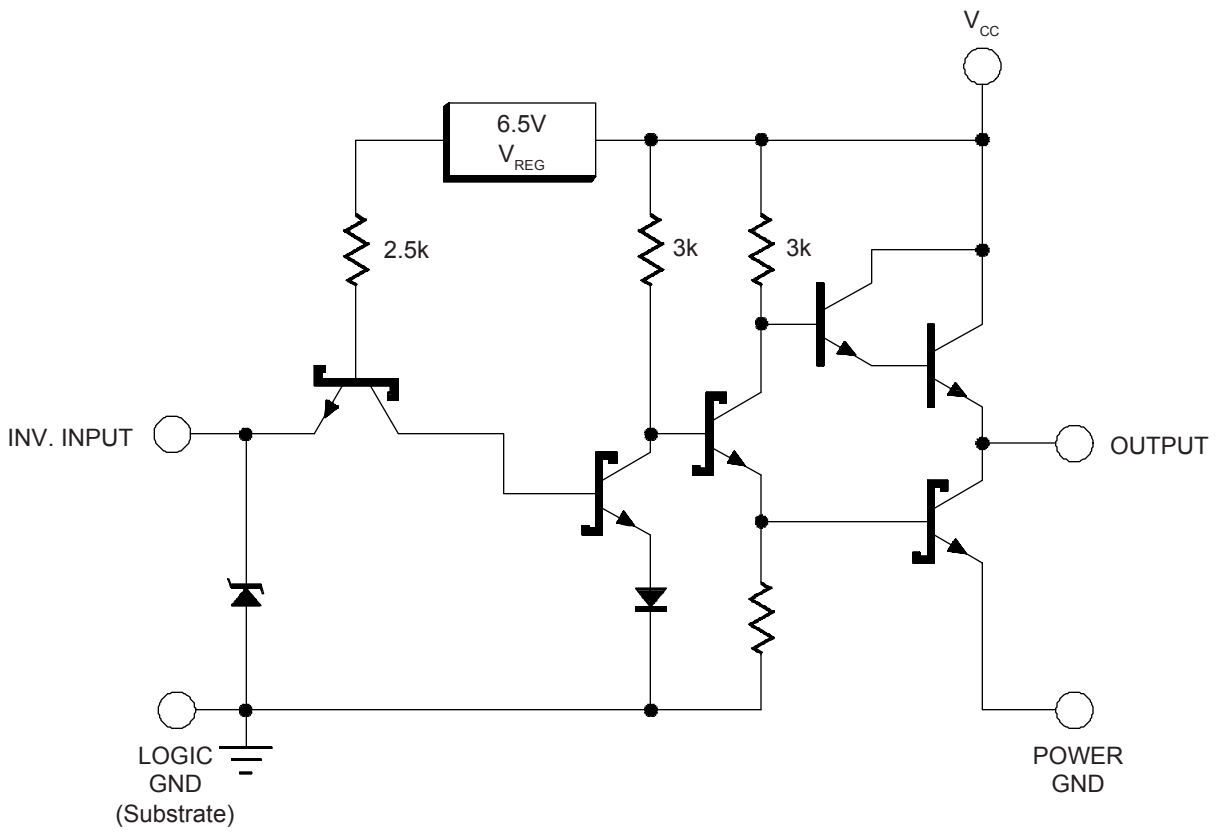
FEATURES

- Totem Pole Outputs with 3.0A Peak Current Capability
- Supply Voltage up to 22V
- Rise and Fall Times Less than 25ns
- Propagation Delays Less than 20ns
- Non-inverting High-speed High-voltage Schottky Logic
- Efficient Operation at High Frequency
- Available in:
  - 8 Pin Plastic and Ceramic DIP
  - 20 Pin LCC

HIGH RELIABILITY FEATURES

- Available to MIL-STD-883, ¶ 1.2.1
- Radiation Data Available
- MSC-AMS Level "S" Processing Available
- Available to DSCC - Standard Microcircuit Drawing (SMD)

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) 22V
Logic Input Voltage 7V
Source/Sink Output Current (Each Output)
  Continuous ..... ±0.5A
  Pulse, 500ns ..... ±3.0A

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. All currents are positive into the specified terminal.

Operating Junction Temperature
  Hermetic (Y-Package) ..... 150°C
  Plastic (M, L-Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 2. RoHS Peak Package Solder Reflow Temp. (40 sec. max. exp.) 260°C (+0, -5)

THERMAL DATA

Y Package:
Thermal Resistance-Junction to Case, θ_{JC} ..... 50°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} ..... 130°C/W

M Package:
Thermal Resistance-Junction to Case, θ_{JC} ..... 60°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} ..... 95°C/W

L Package:
Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximum for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Supply Voltage (V_{CC}) ..... 4.5V to 20V (Note 3)
Frequency Range ..... DC to 1.5MHz
Peak Pulse Current ..... ±3A
Logic Input Voltage ..... -0.5 to 5.5V

Operating Ambient Temperature Range (T_A)
  SG1644 ..... -55°C to 125°C
  SG3644 ..... 0°C to 70°C

Note 2. Range over which the device is functional.
Note 3. AC performance has been optimized for V_{CC} = 8V to 20V.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1644 with -55°C ≤ T_A ≤ 125°C, SG3644 with 0°C ≤ T_A ≤ 70°C, and V_{CC} = 20V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1644/SG3644			Units
		Min.	Typ.	Max.	
Static Characteristics					
Logic 1 Input Voltage		2.0			V
Logic 0 Input Voltage				0.7	V
Input High Current	V_{IN} = 2.4V			500	µA
Input High Current	V_{IN} = 5.5V			1.0	mA
Input Low Current	V_{IN} = 0V			-4	mA
Input Clamp Voltage	I_{IN} = -10mA			-1.5	V
Output High Voltage (Note 4)	I_{OUT} = -200mA	V_{CC}-3			V
Output Low Voltage (Note 4)	I_{OUT} = 200mA			1.0	V
Supply Current Outputs Low	V_{IN} = 0V (both inputs)		18	27	mA
Supply Current Outputs High	V_{IN} = 2.4V (both inputs)		7.5	12	mA

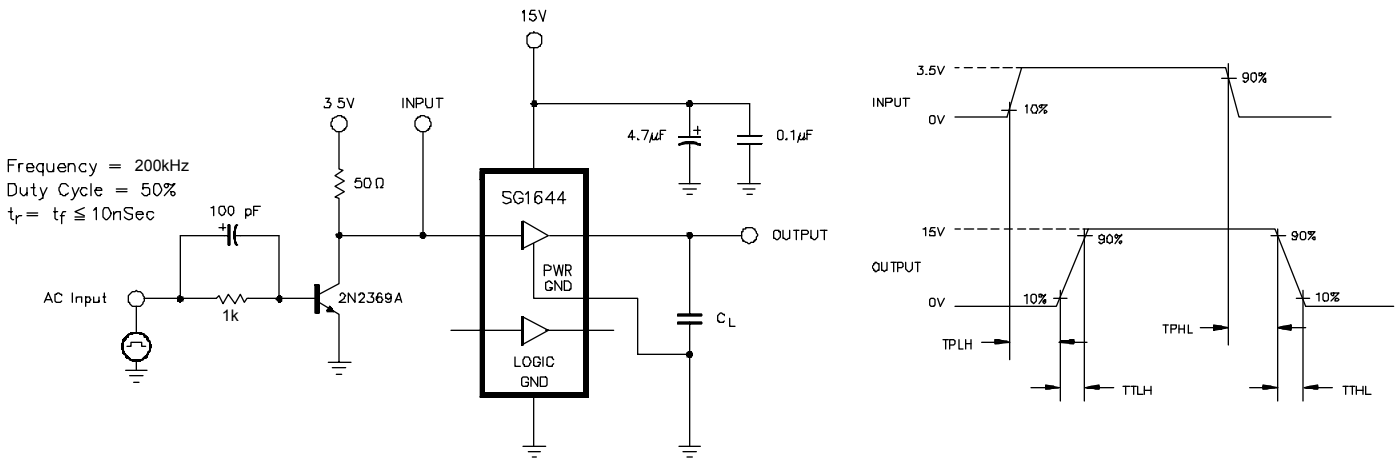
Note 4. V_{CC} = 10V to 20V.

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions (Figure 1)	SG1644/SG3644 T_A = 25°C			SG1644 T_A=-55°C to 125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Dynamic Characteristics (Note 6)								
Propagation Delay High-Low	C_L = 1000pF (Note 5)			30			40	ns
(TPHL)	C_L = 2500pF		26	35			50	ns
Propagation Delay Low-High	C_L = 1000pF (Note 5)			25			30	ns
(TPLH)	C_L = 2500pF		18	30			40	ns
Rise Time (TTLH)	C_L = 1000pF (Note 5)			30			35	ns
	C_L = 2500pF		30	40			50	ns
Fall Time (TTHL)	C_L = 1000pF (Note 5)			25			30	ns
	C_L = 2500pF		30	40			50	ns
Supply Current (I_{CC})	C_L = 2500pF, Freq. = 200kHz		30	35			40	mA
(both outputs)	Duty Cycle = 50%							

Note 5. These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.
Note 6. V_{CC} = 15V.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



CHARACTERISTIC CURVES

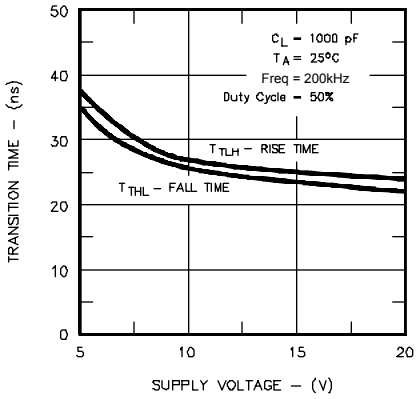


FIGURE 2.
TRANSITION TIMES VS. SUPPLY VOLTAGE

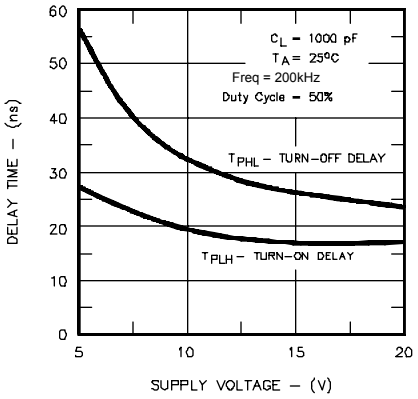


FIGURE 3.
PROPAGATION DELAY VS. SUPPLY VOLTAGE

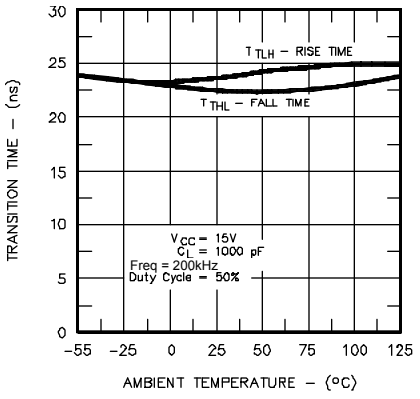


FIGURE 4.
TRANSITION TIMES VS. AMBIENT TEMPERATURE

CHARACTERISTIC CURVES (continued)

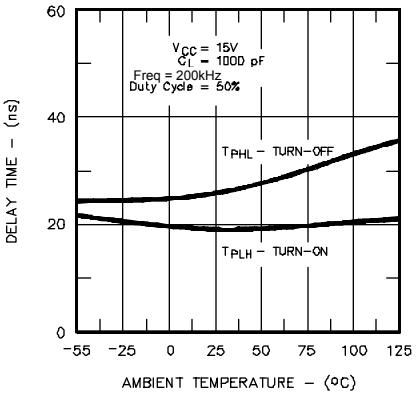


FIGURE 5.
PROPAGATION DELAY VS. AMBIENT TEMPERATURE

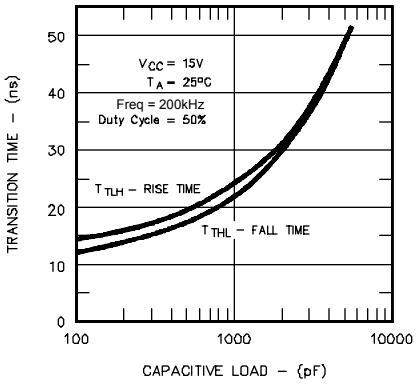


FIGURE 6.
TRANSITION TIMES VS. CAPACITIVE LOAD

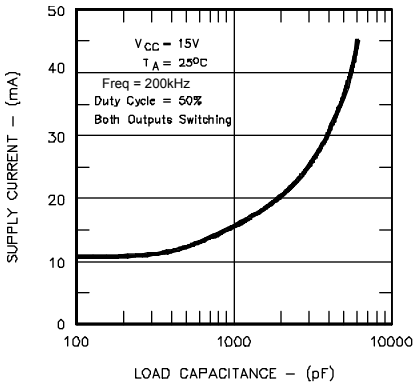


FIGURE 7.
SUPPLY CURRENT VS. CAPACITANCE LOAD

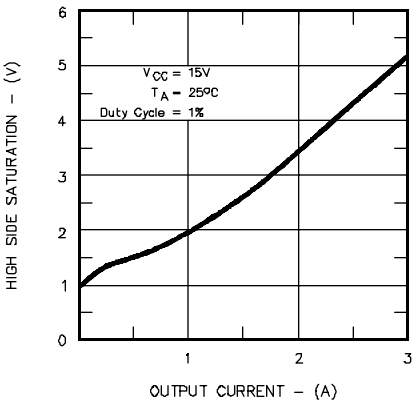


FIGURE 8.
HIGH SIDE SATURATION VS. OUTPUT CURRENT

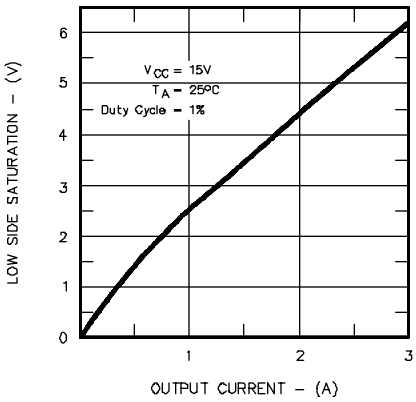


FIGURE 9.
LOW SIDE SATURATION VS. OUTPUT CURRENT

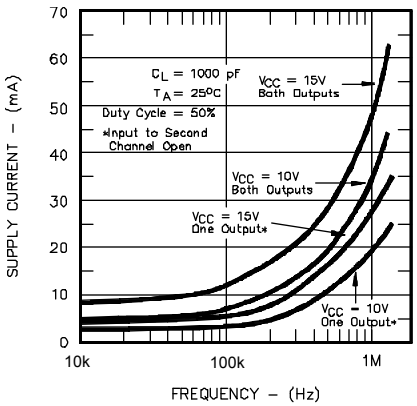


FIGURE 10.
SUPPLY CURRENT VS. FREQUENCY

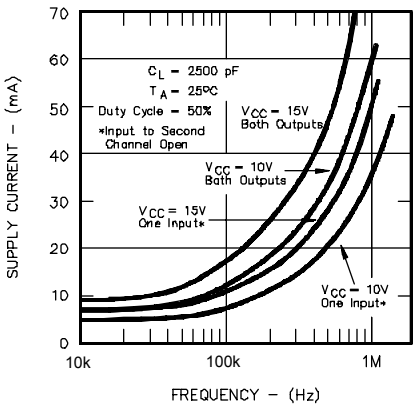


FIGURE 11.
SUPPLY CURRENT VS. FREQUENCY

APPLICATION INFORMATION

POWER DISSIPATION

The SG1644, while more energy-efficient than earlier gold-doped driver IC's, can still dissipate considerable power because of its high peak current capability at high frequencies. Total power dissipation in any specific application will be the sum of the DC or steady-state power dissipation, and the AC dissipation caused by driving capacitive loads.

The DC power dissipation is given by:

$P_{DC} = +V_{CC} \cdot I_{CC}$ [1]

where I_{CC} is a function of the driver state, and hence is duty-cycle dependent.

The AC power dissipation is proportional to the switching frequency, the load capacitance, and the square of the output voltage. In most applications, the driver is constantly changing state, and the AC contribution becomes dominant when the frequency exceeds 100-200kHz.

The SG1644 driver family is available in a variety of packages to accommodate a wide range of operating temperatures and power dissipation requirements. The Absolute Maximums section of the data sheet includes two graphs to aid the designer in choosing an appropriate package for his design.

The designer should first determine the actual power dissipation of the driver by referring to the curves in the data sheet relating operating current to supply voltage, switching frequency, and capacitive load. These curves were generated from data taken on actual devices. The designer can then refer to the Absolute Maximum Thermal Data section to choose a package type, and to determine if heat-sinking is required.

DESIGN EXAMPLE

Given: Two 2500pF loads must be driven push-pull from a +15 volt supply at 100kHz. The application is a commercial one in which the maximum ambient temperature is +50°C, and cost is important.

1. From Figure 11, the average driver current consumption under these conditions will be 18mA, and the power dissipation will be 15volts x 18mA, or 270mW.

2. From the thermal data table the M package provides a 95°C/W temperature rise junction to ambient. Therefore 270mW multiplied by 95°C/W calculates to a temperature rise of about 26°C. The M package has therefore enough thermal conduction to support operation at +50°C. The SG3644M driver would be specified for this application.

SUPPLY BYPASSING

Since the SG1644 can deliver peak currents above 3amps under some load conditions, adequate supply bypassing is essential for proper operation. Two capacitors in parallel are recommended to guarantee low supply impedance over a wide bandwidth: a 0.1µF ceramic disk capacitor for high frequencies, and a 4.7µF solid tantalum capacitor for energy storage. In military applications, a CK05 or CK06 ceramic operator with a CSR-13 tantalum capacitor is an effective combination. For commercial applications, any low-inductance ceramic disk capacitor teamed with a Sprague 150D or equivalent low ESR capacitor will work well. The capacitors must be located as close as physically possible to the V_{CC} pin, with combined lead and pc board trace lengths held to less than 0.5 inches.

GROUNDING CONSIDERATIONS

The ability of the SG1644 to deliver high peak currents into capacitive loads can cause undesirable negative transients on the logic and power grounds. To avoid this, a low inductance ground path should be considered for each output to return the high peak currents back to its own ground point. A ground plane is recommended for best performance. If space for a ground plane is not available, make the paths as short and as wide as possible. The logic ground can be returned to the supply bypass capacitor and be connected at one point to the power grounds.

LOGIC INTERFACE

The logic input of the 1644 is designed to accept standard DC-coupled 5 volt logic swings, with no speed-up capacitors required. If the input signal voltage exceeds 6 volts, the input pin must be protected against the excessive voltage in the HIGH state. Either a high speed blocking diode must be used, or a resistive divider to attenuate the logic swing is necessary.

LAYOUT FOR HIGH SPEED

The SG1644 can generate relatively large voltage excursions with rise and fall times around 20-30 nanoseconds with light capacitive loads. A Fourier analysis of these time domain signals will indicate strong energy components at frequencies much higher than the basic switching frequency. These high frequencies can induce ringing on an otherwise ideal pulse if sufficient inductance occurs in the signal path (either the positive signal trace or the ground return). Overshoot on the rising edge is undesirable because the excess drive voltage could rupture the gate oxide of a power MOSFET. Trailing edge undershoot is dangerous because the negative voltage excursion can forward-bias the parasitic PN substrate diode of the driver, potentially causing erratic operation or outright failure.

Ringing can be reduced or eliminated by minimizing signal path inductance, and by using a damping resistor between the drive output and the capacitive load. Inductance can be reduced by keeping trace lengths short, trace widths wide, and by using 2oz. copper if possible. The resistor value for critical damping can be calculated from:

$R_D = 2\sqrt{L/C_L}$ [2]

where L is the total signal line inductance, and C_L is the load capacitance. Values between 10 and 100ohms are usually sufficient. Inexpensive carbon composition resistors are best because they have excellent high frequency characteristics. They should be located as close as possible to the gate terminal of the power MOSFET.

TYPICAL APPLICATIONS

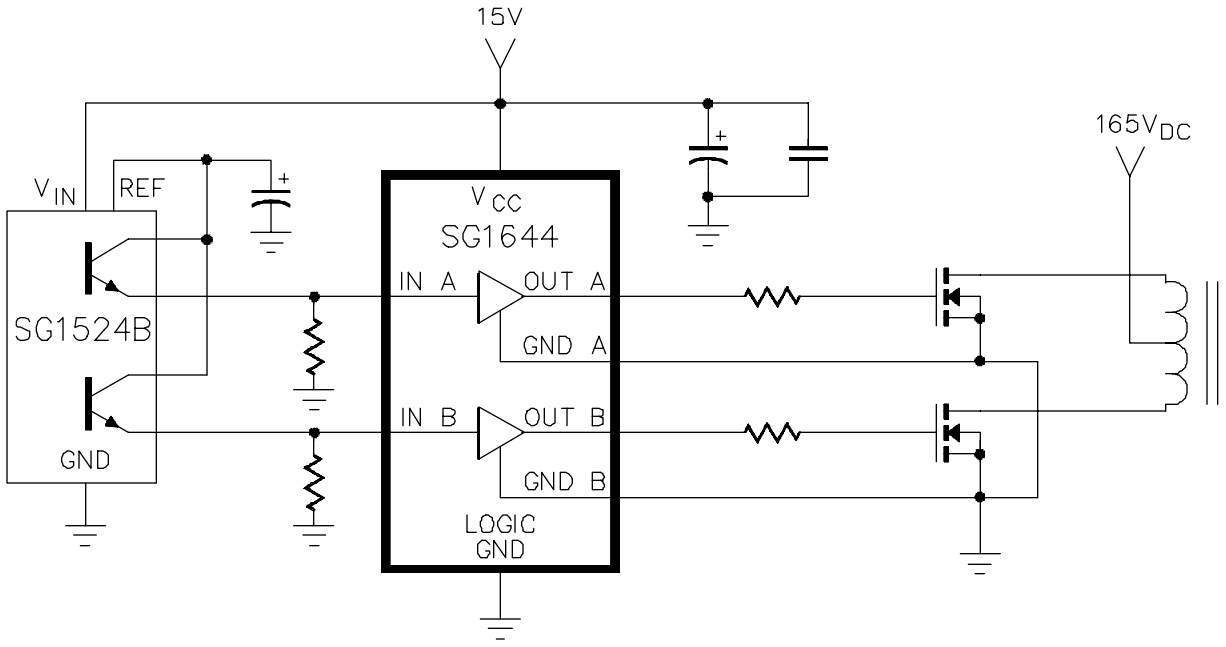


FIGURE 12.
In this push pull converter circuit, the control capabilities of the SG1524B PWM are combined with the powerful totem-pole drivers found in the SG1644 (see SG1626 for example). This inexpensive configuration results in very fast charge and discharge of the power MOSFET gate capacitance for efficient switching.

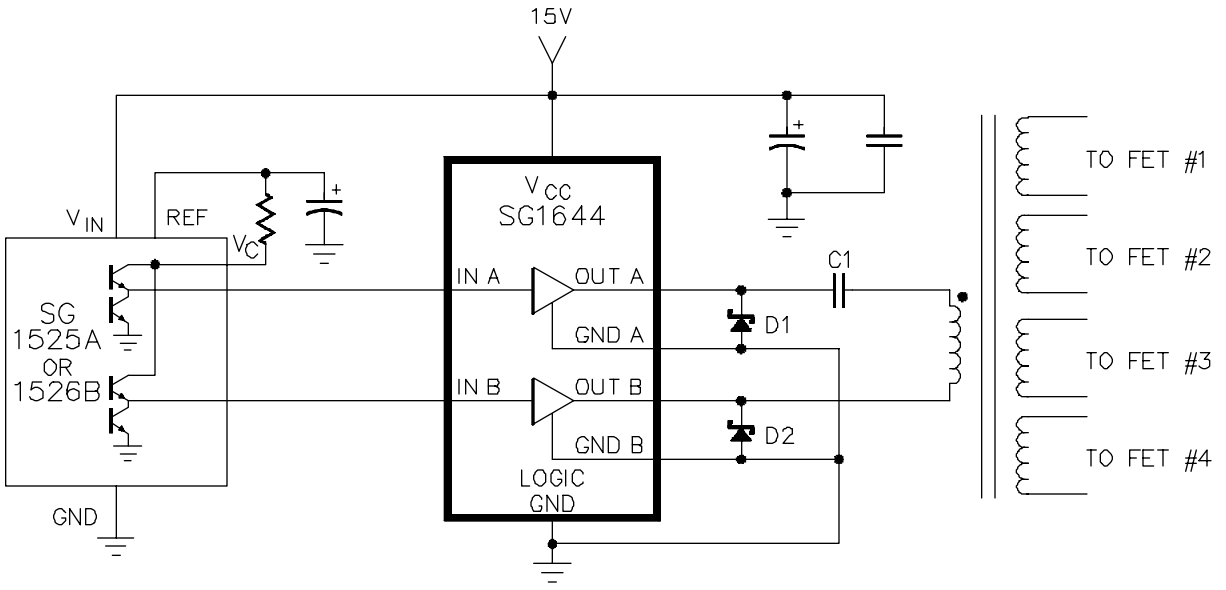


FIGURE 13.
When the peak current capabilities of PWM's such as 1525A or 1526B are not sufficient to drive high capacitive loads fast enough, SG1644 is one solution to this problem. This combination is especially suited for full bridge applications where high input capacitance MOSFETs are being used. Diodes D1 and D2 are necessary if the leakage inductance of the drive transformer will drive the output pins negative.

TYPICAL APPLICATIONS (continued)

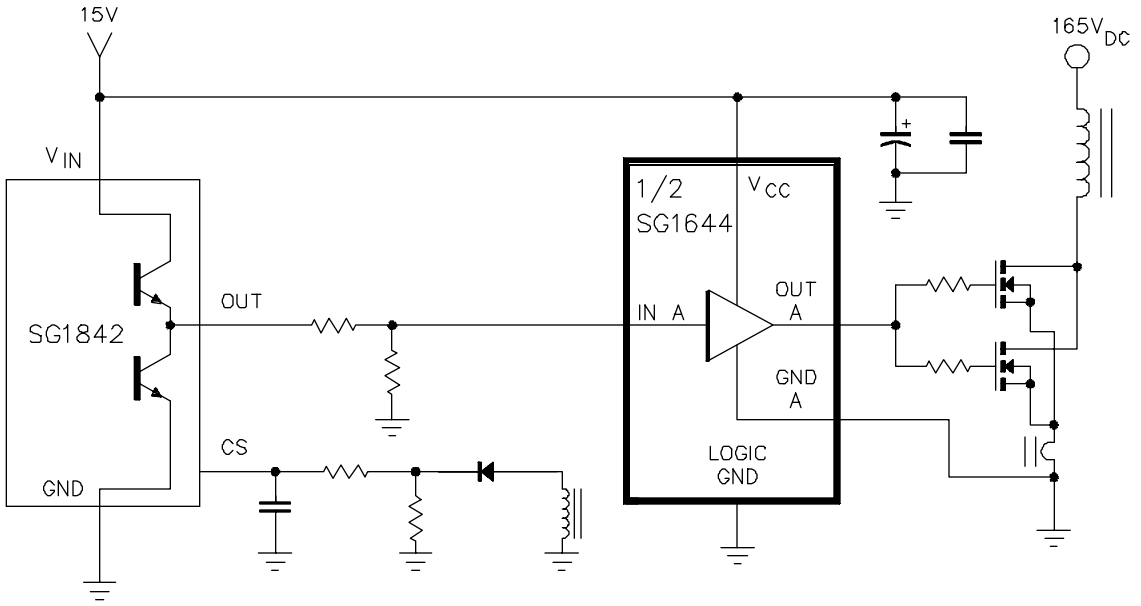


FIGURE 14.
A low cost, yet powerful alternative to the single ended converters with parallel MOSFETs is a combination of SG1842 and SG1644 as shown in Figure 16. This combination will also allow a low noise operation by separating the drive and its associated high peak currents, away from the PWM logic section.

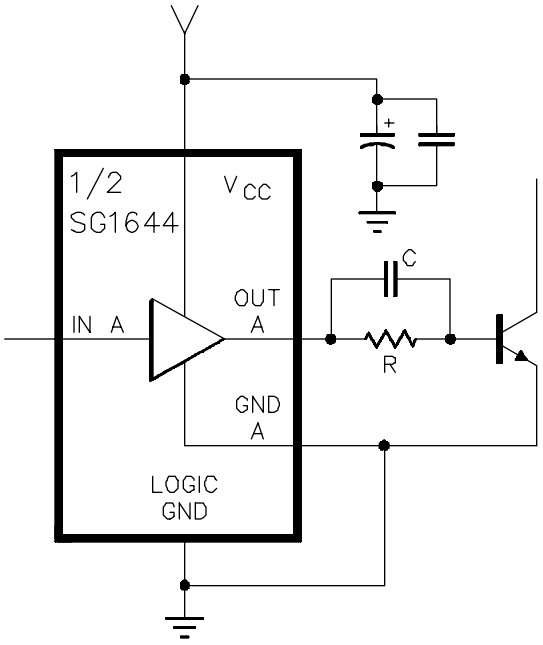


FIGURE 15.
Fast turn off of bipolar transistors is possible by the totem pole output stage of SG1644. The charge on capacitor C will drive the base negative for faster turn off.

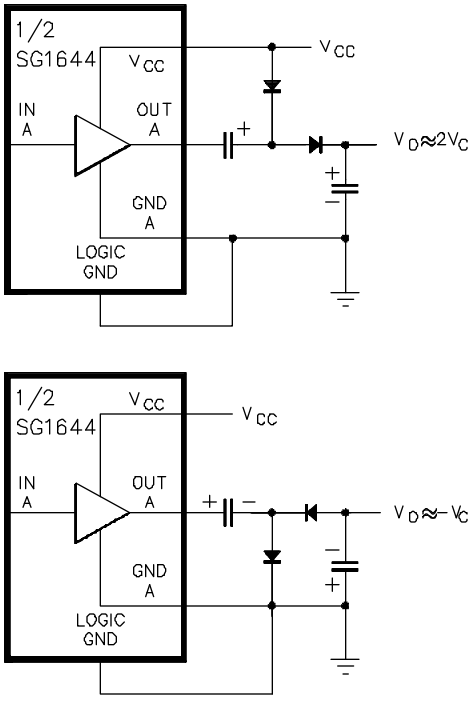
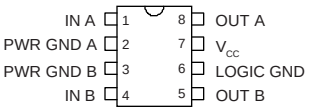
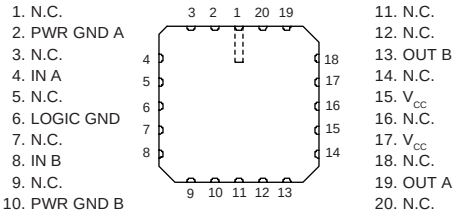


FIGURE 16.
When the inputs are driven with a TTL square wave drive, the high peak current capabilities of SG1644 allow easy implementation of charge pump voltage converters.

CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
8-PIN CERAMIC DIP Y - PACKAGE	SG1644Y-883B SG1644Y-DESC SG1644Y	-55°C to 125°C -55°C to 125°C -55°C to 125°C	
8-PIN PLASTIC DIP M - PACKAGE	SG3644M	0°C to 70°C	M Package: RoHS Compliant / Pb-free Transition DC: 0503 M Package: RoHS / Pb-free 100% Matte Tin Lead Finish
20-PIN CERAMIC (LCC) LEADLESS CHIP CARRIER L- PACKAGE	SG1644L-883B SG1644L-DESC	-55°C to 125°C -55°C to 125°C	

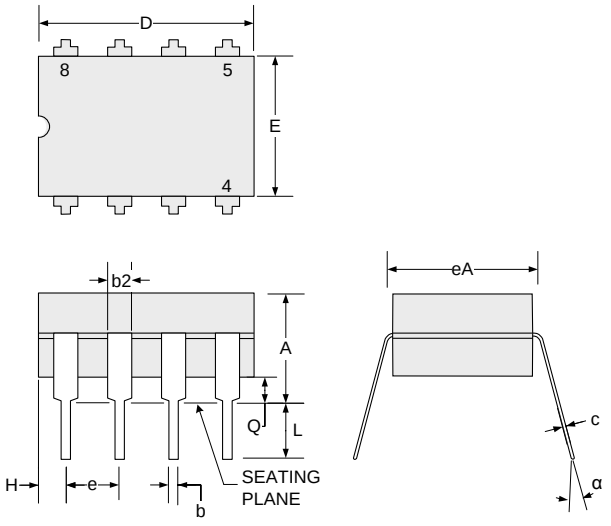
Note 1. Contact factory for DESC product availability.

Note 2. All packages are viewed from the top.

Note 3. Hermetic Packages Y and L use Pb37/Sn63 hot solder lead finish, contact factory for availability of RoHS versions.

PACKAGE OUTLINE DIMENSIONS

Controlling dimensions are in inches, metric equivalents are shown for general information.

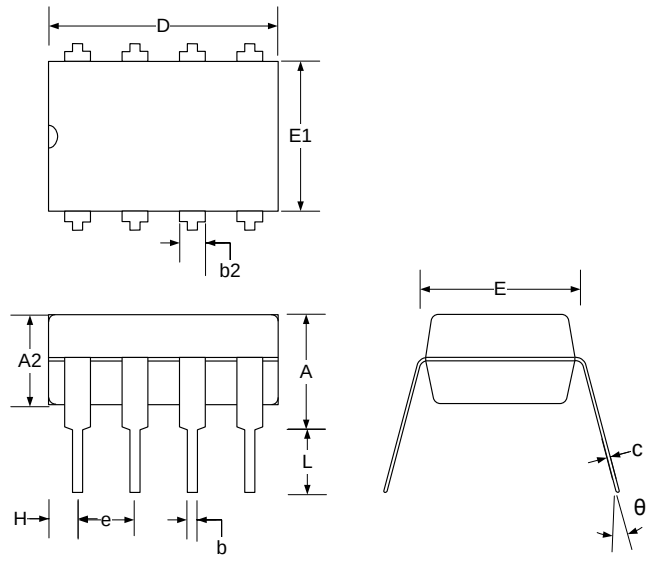


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	-	15°	-	15°
Q	0.51	1.02	0.020	0.040

Note:

Dimensions do not include protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 17 · Y 8-Pin CERDIP Package Dimensions



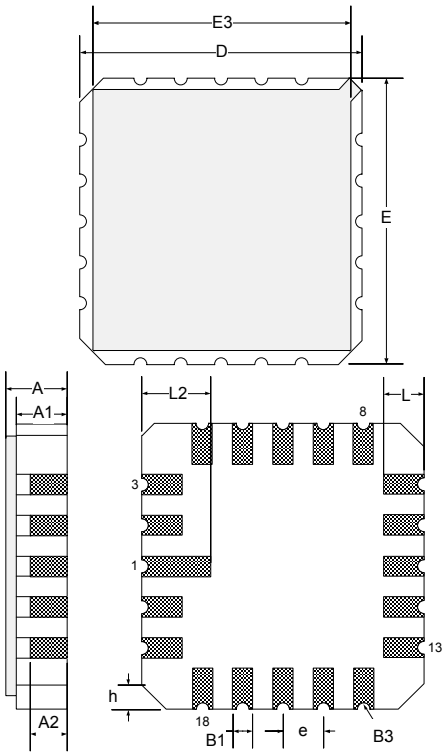
Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.08	-	0.200
A2	3.30 Typ.		1.30 Typ.	
b	0.38	0.51	0.145	0.020
b2	0.76	1.65	0.030	0.065
c	0.20	0.38	0.008	0.015
D	-	10.16	-	0.400
E	7.62 BSC		0.300 BSC	
e	2.54 BSC		0.100 BSC	
E1	6.10	6.86	0.240	0.270
L	3.05	-	0.120	-
θ	0°	15°	0°	15°

Note:

Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 18 · M 8-Pin PDIP Package Dimensions

PACKAGE OUTLINE DIMENSIONS (continued)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note: All exposed metalized area shall be gold plated 60 µ-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 19 · L 20-Pin Ceramic LCC Package Dimensions

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SG1644-1.3/02.15