Panasonic

AN44066A

37V/0.8A Stepping Motor Driver

FEATURES

- 2-phase input control by rationalization of interface (2-phase excitation, half-step, and 1-2 phase excitation enabled)
- 4-phase input control (W1-2 phase excitation enabled)
- Built-in CR chopping (with frequency selected)
- Built-in standby function
- Built-in thermal protection and low voltage detection circuit
- Built-in 5 V power supply
- 32 pin Plastic Shrink Small Outline Package (SSOP Type)

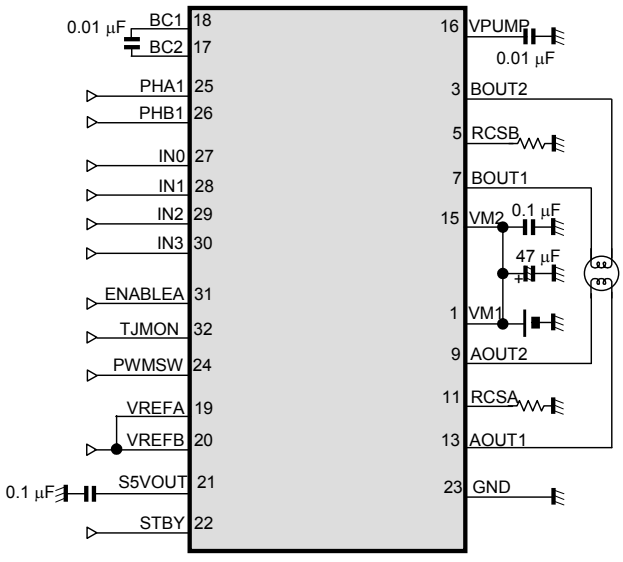
DESCRIPTION

AN44066A is a two channels H-bridge driver LSI. Bipolar stepping motor can be controlled by this single driver LSI.2-phase, half-step, 1-2 phase, W1-2 phase can be selected.

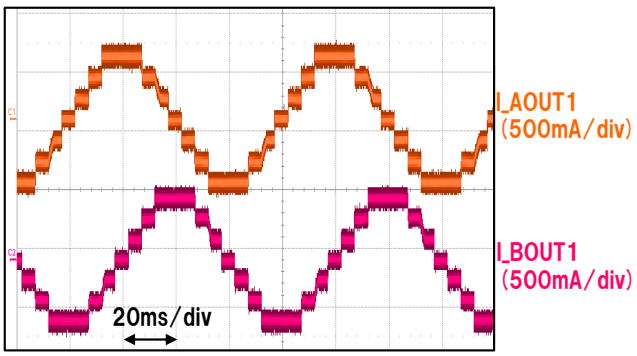
APPLICATIONS

- LSI for stepping motor drives

SIMPLIFIED APPLICATION



Motor Current Waveform



Condition:
VM=24V
Peak motor current:600mA
excitation mode :W1-2 phase drive

Notes)
This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage (Pin 1, 15)	V_M	37	V	*1
Power dissipation	P_D	0.427	W	*2
Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
Operating junction temperature	T_j	–20 to +150	°C	*3
Storage temperature	T_{stg}	–55 to +150	°C	*3
Output pin voltage (Pin 3, 7, 9, 13)	V_{OUT}	37	V	*4
Motor drive current (Pin 3, 7, 9, 13)	I_{OUT}	±0.8	A	*4
Flywheel diode current (Pin 3, 7, 9, 13)	I_f	0.8	A	*4
Input Voltage Range	V_{RCSA},V_{RCSB}	2.5	V	—
	V_{VPUMP}	(VM-1) to 43	V	*5
	V_{BC2}	(VM-1) to 43	V	*5
	V_{BC1}	VM+0.3	V	*5
	V_{VREFA},V_{VREFB}	-0.3 to 6	V	—
	V_{STBY}	-0.3 to 6	V	—
	I_{S5VOUT}	-5 to 0	mA	*5,*6
	V_{PWMSW}	-0.3 to 6	V	—
	V_{PHA1},V_{PHB1}	-0.3 to 6	V	—
	$V_{IN0\sim IN3}$	-0.3 to 6	V	—
	$V_{ENABLEA}$	-0.3 to 6	V	—
ESD	HBM (Human Body Model)	+2 -1	kV	—
	CDM (Charge Device Model)	± 1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 :The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) LSI package without a heat sink. When using this LSI, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

*4 : Do not apply external currents or voltages to any pin not specifically mentioned.
For the circuit currents, "+" denotes current flowing into the LSI, and "–" denotes current flowing out of the LSI.

*5 : Do not apply external voltages to this pin. Set not to exceed allowable range at any time.

*6 : This is the rating under the condition that VM is used in the range between 16 V and 34 V. When VM is used in the range between 10 V and 16 V, the rating is –1.4 mA to 0.

POWER DISSIPATION RATING

Condition	θ_{JA}	PD (Ta=25 °C)	PD (Ta=70 °C)
Mount on PWB *1	96.9 °C/W	1290mW	825mW
Without PWB	187.1 °C/W	668mW	427mW

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm)

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VM1,VM2	10	24	34	V	*1
Input Voltage Range	V_{PWMSW}	0	-	5.5	V	—
	V_{PHA1}, V_{PHB1}	0	-	5.5	V	—
	$V_{IN0\sim IN3}$	0	-	5.5	V	—
	$V_{ENABLEA}$	0	-	5.5	V	—
	V_{VREFA}, V_{VREFB}	0	-	5	V	—
External Constants	C_{BC}	-	0.01	-	µF	—
	C_{VPUMP}	-	0.01	-	µF	—
	C_{S5VOUT}	-	0.1	-	µF	—
Operating ambient temperature	Ta^{opr}	-20	-	70	°C	—
Operating junction temperature	Tj^{opr}	-	-	120	°C	—

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECRTRICAL CHARACTERISTICS

VM=24V,T_a = 25°C±2°C unless otherwise noted.

*1 : Typical Value checked by design.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Power Block							
High-level output saturation voltage	V_{OH}	I_{IN} = –0.5 A	V_M – 0.47	V_M – 0.31	—	V	—
Low-level output saturation voltage	V_{OL}	I_{IN} = 0.5 A	—	0.47	0.71	V	—
Flywheel diode forward voltage	V_{DI}	I_{IN} = ±0.5 A	0.5	1.0	1.5	V	—
Output leakage current	I_{LEAK}	V_M = 37 V, V_{RCS} = 0 V	—	10	20	µA	—
Supply current (at when only control system and charge Pump circuit are ON)	I_M	ENABLEA = 3.3 V STBY = 0 V	—	5.4	8.2	mA	—
Supply current (at standby mode)	I_{STBY}	STBY = 2.1 V	—	120	190	µA	—
Output slew rate 1	VT_r	Output voltage rising edge	—	270	—	V/µs	*1
Output slew rate 2	VT_f	Output voltage falling edge	—	330	—	V/µs	*1
Dead time	T_D	—	—	2.8	—	µs	*1
I/O Block							
High-level IN input voltage	V_{INH}	—	2.2	—	5.5	V	—
Low-level IN input voltage	V_{INL}	—	0	—	0.6	V	—
High-level IN input current	I_{INH}	IN0 = IN1 = IN2 = IN3 = 5 V	–10	—	10	µA	—
Low-level IN input current	I_{INL}	IN0 = IN1 = IN2 = IN3 = 0 V	–15	—	15	µA	—
High-level PHA1/PHB1 input voltage	V_{PHAH} V_{PHBH}	—	2.2	—	5.5	V	—
Low-level PHA1/PHB1 input voltage	V_{PHAL} V_{PHBL}	—	0	—	0.6	V	—
High-level PHA1/PHB1 input current	I_{PHAH} I_{PHBH}	PHA1 = PHB1 = 3.3 V	16.5	33	66	µA	—
Low-level PHA1/PHB1 input current	I_{PHAL} I_{PHBL}	PHA1 = PHB1 = 0 V	–15	—	15	µA	—
High-level ENABLEA input voltage	$V_{ENABLEAH}$	—	2.2	—	5.5	V	—
Low-level ENABLEA input voltage	$V_{ENABLEAL}$	—	0	—	0.6	V	—
High-level ENABLEA input current	$I_{ENABLEAH}$	ENABLEA = 5 V	–10	—	10	µA	—
Low-level ENABLEA input current	$I_{ENABLEAL}$	ENABLEA = 0 V	–15	—	15	µA	—
High-level PWMSW input voltage	V_{PWMSWH}	—	2.2	—	5.5	V	—
Low-level PWMSW input voltage	V_{PWMSWL}	—	0	—	0.6	V	—
High-level PWMSW input current	I_{PWMSWH}	PWMSW = 3.3 V	8	16.5	33	µA	—

ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I/O Block							
Low-level PWMSW input current	I_{PWMSWL}	PWMSW = 0 V	–15	—	15	μA	—
High-level STBY input voltage	V_{STBYH}	—	2.1	—	5.5	V	—
Low-level STBY input voltage	V_{STBYL}	—	0	—	0.6	V	—
High-level STBY input current	I_{STBYH}	STBY = 5 V	—	30	45	μA	—
Low-level STBY input current	I_{STBYL}	STBY = 0 V	–2	—	2	μA	—
High-level PHA1/PHB1 input current 2	I_{PHAH2} I_{PHBH2}	PHA1 = PHB1 = 5 V	—	68	—	μA	*1 *2
High-level PWMSW input current 2	$I_{PWMSWH2}$	PWMSW = 5 V	—	42	—	μA	*1 *2
Torque Control Block							
Input bias current	I_{REFA} I_{REFB}	V_{REFA} = 5 V V_{REFB} = 5 V	83.3	100	125	μA	—
PWM frequency1	f_{PWM1}	PWMSW = 0.6 V	34	52	70	kHz	—
PWM frequency2	f_{PWM2}	PWMSW = 2.2 V	17	26	35	kHz	—
Pulse blanking time	T_B	V_{REFA} = V_{REFB} = 0 V	0.38	0.75	1.12	μs	—
Comp threshold H (100%)	VT_H	V_{REFA} = V_{REFB} = 3.3 V IN0 = IN1 = 0.6 V IN2 = IN3 = 0.6 V	627	660	693	mV	—
Comp threshold C (67%)	VT_C	V_{REFA} = V_{REFB} = 3.3 V IN0 = 2.2 V, IN1 = 0.6 V IN2 = 2.2 V, IN3 = 0.6 V	410	440	470	mV	—
Comp threshold L (33%)	VT_L	V_{REFA} = V_{REFB} = 3.3 V IN0 = 0.6 V, IN1 = 2.2 V IN2 = 0.6 V, IN3 = 2.2 V	200	220	240	mV	—
Reference Voltage Block							
Reference voltage	V_{S5VOUT}	I_{S5VOUT} = 0 mA	4.5	5.0	5.5	V	—
Output impedance	Z_{S5VOUT}	I_{S5VOUT} = –1.5 mA, –3.5 mA	—	18	27	Ω	—

*1 : Typical Value checked by design.
*2 : Refer to the “Usage Notes” (P.16) for the input current characteristics about PHA1, PHB1, PWMSW.

ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

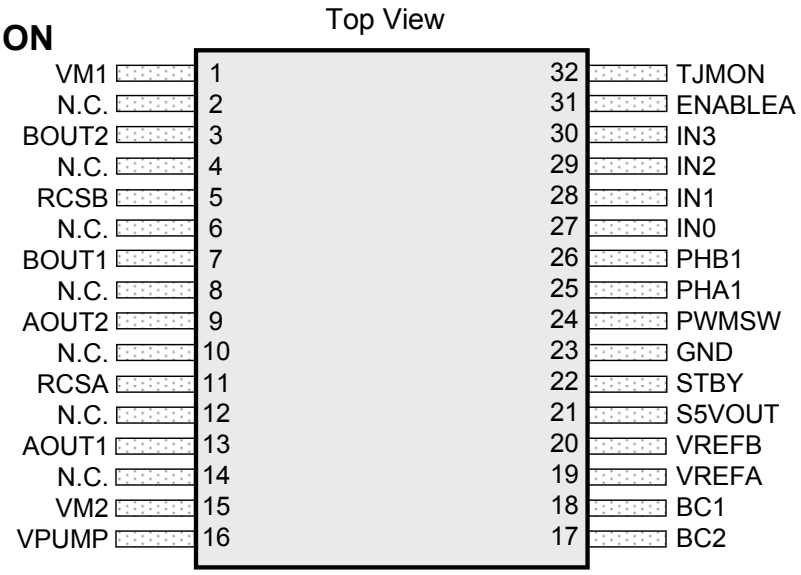
Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Thermal Protection							
Thermal protection operating temperature	TSD_{on}	—	—	150	—	°C	*1
Thermal protection hysteresis width	ΔTSD	—	—	40	—	°C	*1
VREF Block							
Input impedance	Z_{VREFA} Z_{VREFB}	V_{REFA} = 5 V V_{REFB} = 5 V	40	50	60	kΩ	*3
Input impedance precision	—	—	–20	—	20	%	*3

*1 : Typical Value checked by design.
*3 : Checked by design, not production tested.

Panasonic

AN44066A

PIN CONFIGURATION



PIN FUNCTIONS

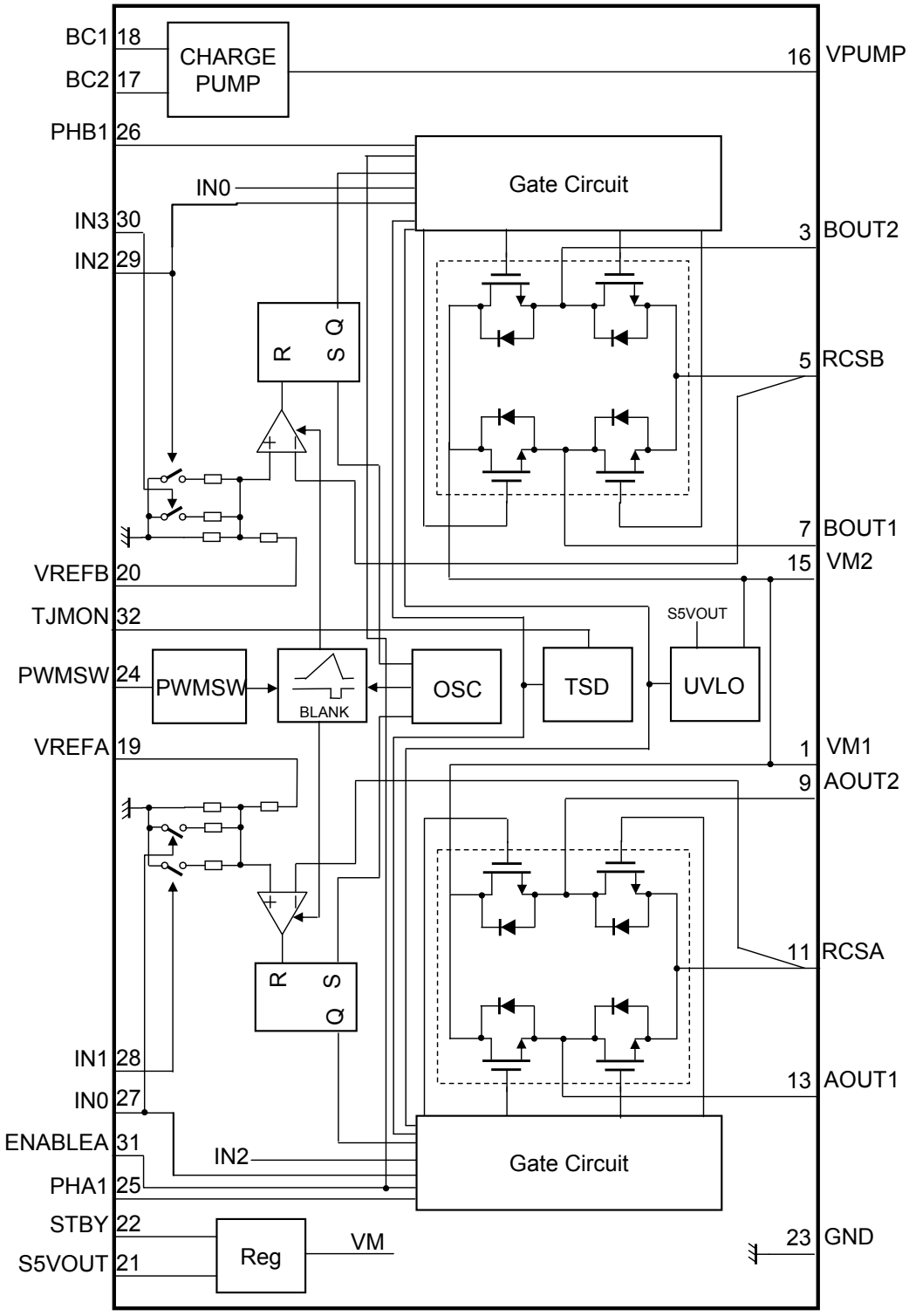
Pin No.	Pin name	Type	Description
1	VM1	Power supply	Motor power supply 1
2,4,6,8, 10,12,14	N.C.	—	No Connection
3	BOUT2	Output	Phase B motor drive output 2
5	RCSB	Input / Output	Phase B current detection
7	BOUT1	Output	Phase B motor drive output 1
9	AOUT2	Output	Phase A motor drive output 2
11	RCSA	Input / Output	Phase A current detection
13	AOUT1	Output	Phase A motor drive output 1
15	VM2	Power supply	Motor power supply 2
16	VPUMP	Output	Charge Pump circuit output
17	BC2	Output	Charge Pump capacitor connection 2
18	BC1	Output	Charge Pump capacitor connection 1
19	VREFA	Input	Phase A torque reference voltage input
20	VREFB	Input	Phase B torque reference voltage input
21	S5VOUT	Output	Internal reference voltage (5 V output)
22	STBY	Input	Standby setting
23	GND	Ground	Signal ground
24	PWMSW	Input	PWM frequency selection input
25	PHA1	Input	Phase A phase selection input
26	PHB1	Input	Phase B phase selection input
27	IN0	Input	Phase A output torque control 1
28	IN1	Input	Phase A output torque control 2
29	IN2	Input	Phase B output torque control 1
30	IN3	Input	Phase B output torque control 2
31	ENABLEA	Input	Phase A/B start/stop signal input
32	TJMON	Output	VBE monitor use

Note) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

Panasonic

AN44066A

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

OPERATION

Control mode

1.Truth table

1) Control/Charge pump circuit

STBY	ENABLE	Control/Charge pump circuit	Output transistor
High	—	OFF	OFF
Low	High	ON	OFF
Low	Low	ON	ON

2) Output polarity

ENABLEA	PHA1/PHB1	AOUT1/BOUT1	AOUT2/BOUT2
Low	High	High	Low
Low	Low	Low	High
High	—	OFF	OFF

3) Output current of 2-phase excitation / half step / 1-2 phase excitation

IN0	IN2	A-ch. Output Current	B-ch. Output Current
Low	Low	(VREF / 5) × (1 / Rs)	(VREF / 5) × (1 / Rs)
High	Low	0	(VREF / 5) × (1 / Rs)
Low	High	(VREF / 5) × (1 / Rs)	0
High	High	(VREF / 5) × (1 / Rs) × (2 / 3)	(VREF / 5) × (1 / Rs) × (2 / 3)

Notes) Rs : current detection region IN1 = IN3 = Low level

4) Output current of W1-2 phase excitation

A-ch. output

IN0	IN2	IN1	A-ch. Output Current
Low	Low	Low	(VREF / 5) × (1 / Rs)
Low	Low	High	(VREF / 5) × (1 / Rs) × (1 / 3)
High	Low	Don't care	0
Low	High	Low	(VREF / 5) × (1 / Rs)
High	High	Low	(VREF / 5) × (1 / Rs) × (2 / 3)

Note) Rs : current detection region

B-ch. output

IN0	IN2	IN3	B-ch. Output Current
Low	Low	Low	(VREF / 5) × (1 / Rs)
Low	Low	High	(VREF / 5) × (1 / Rs) × (1 / 3)
High	Low	Low	(VREF / 5) × (1 / Rs)
Low	High	Don't care	0
High	High	Low	(VREF / 5) × (1 / Rs) × (2 / 3)

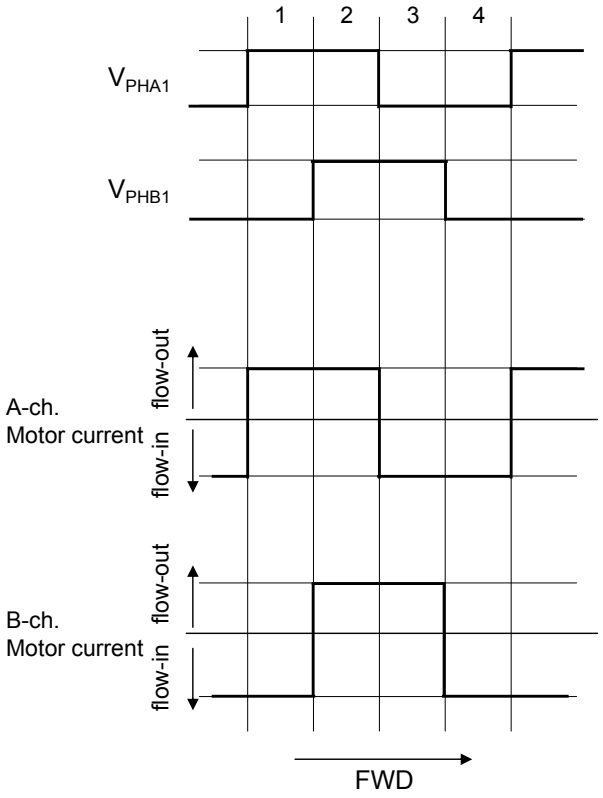
Note) Rs : current detection region

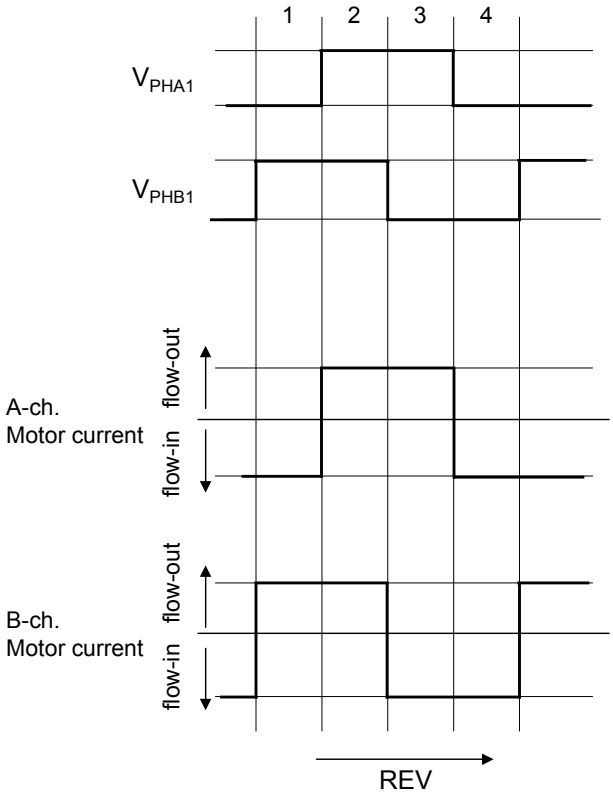
OPERATION (continued)

Control mode(continued)

2. Output wave

1) Drive of 2-phase excitation (4steps sequence)
(IN0 to IN3 = Low)





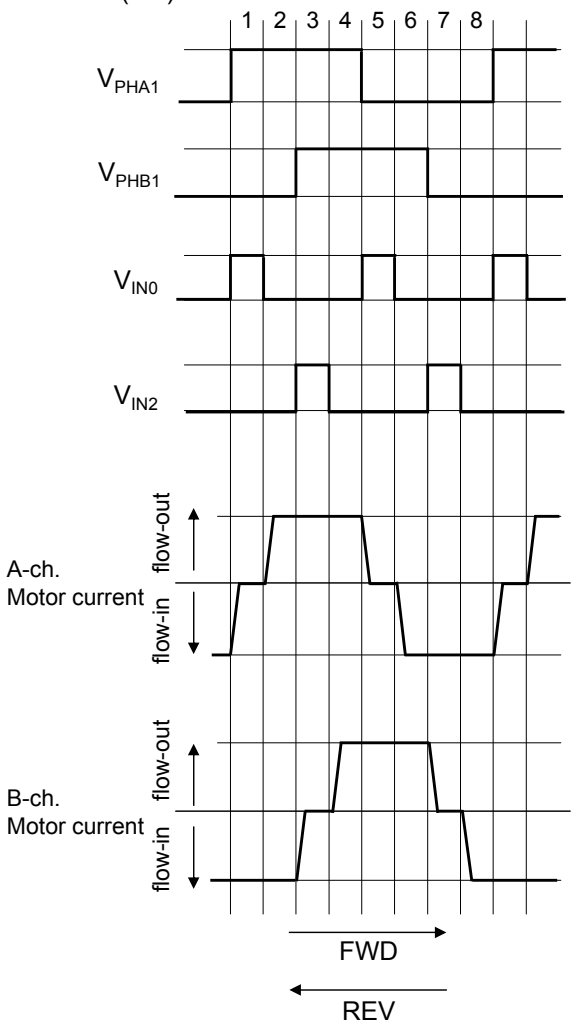
OPERATION (continued)

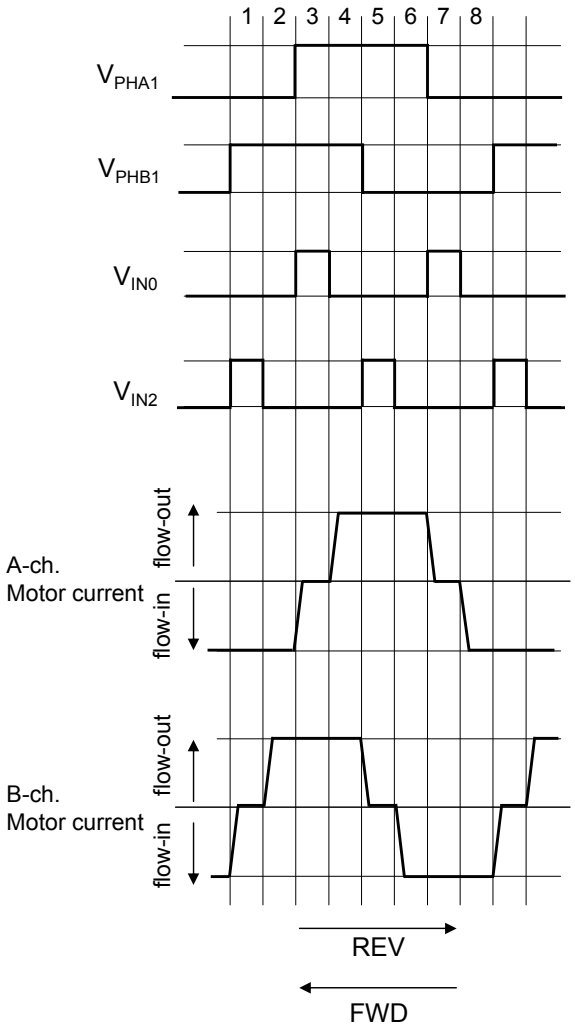
Control mode(continued)

2. Output wave (continued)

2) Drive of half step (8-steps sequence)
(IN1 = IN3 = Low)

(Ex.)





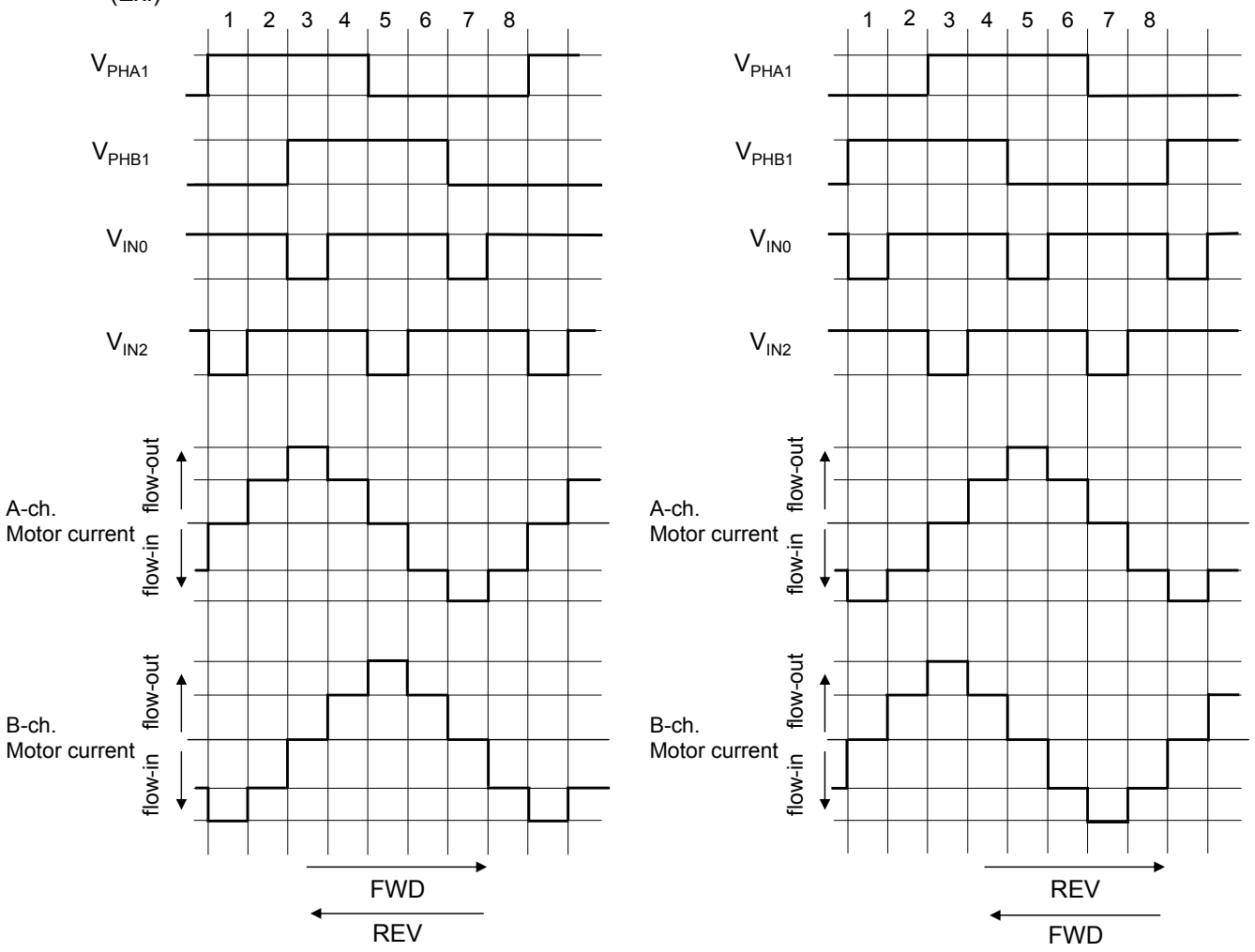
OPERATION (continued)

Control mode(continued)

2. Output wave (continued)

3) Drive of 1-2 phase excitation (8-steps sequence)
(IN1 = IN3 = Low)

(Ex.)

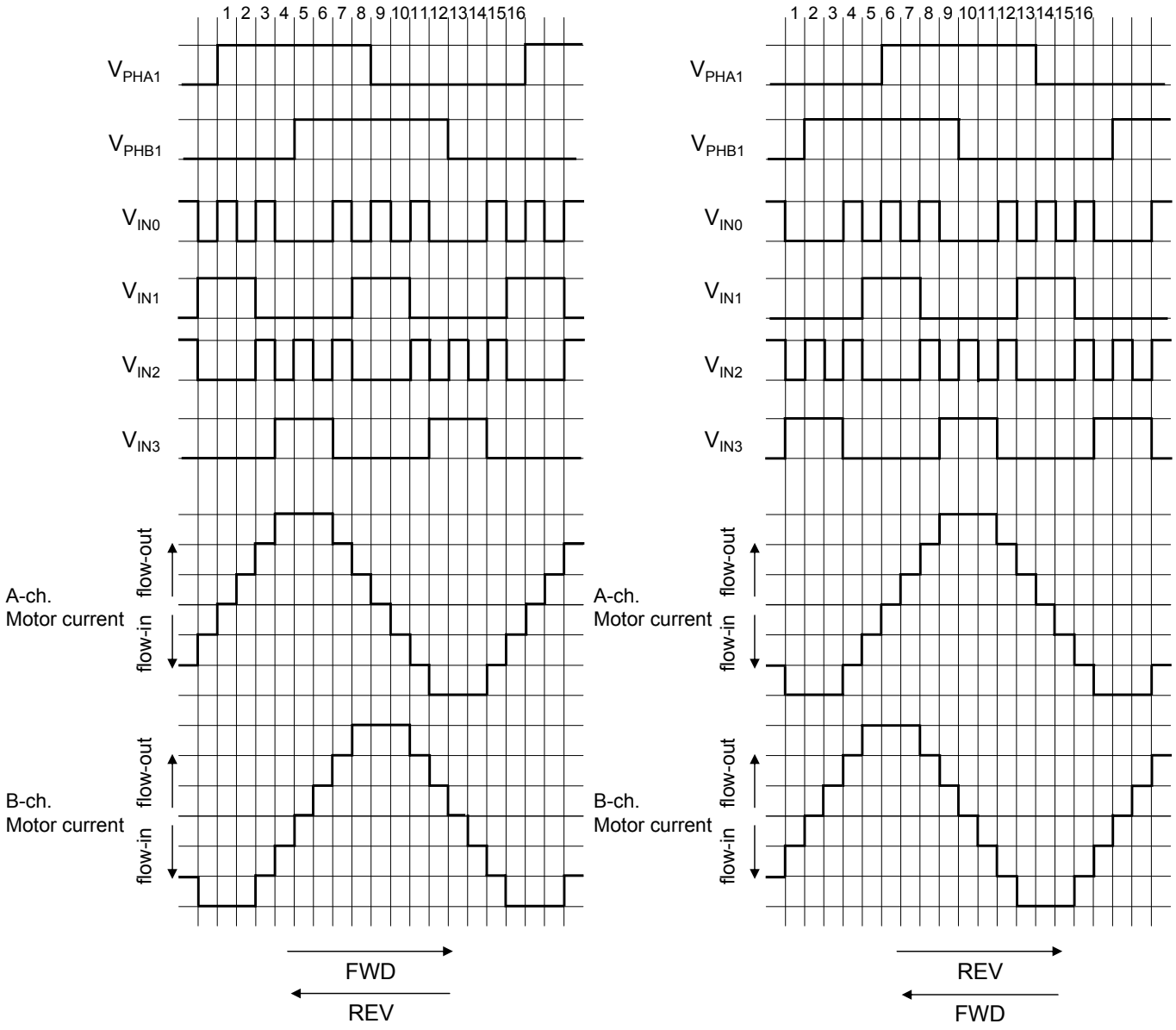


OPERATION (continued)

Control mode(continued)

2. Output wave (continued)

4) Drive of W1-2 phase excitation (16-steps sequence)



APPLICATIONS INFORMATION

Usage Notes

1) Pulse blanking time

In order to prevent mistakes in current detection resulting noise, this LSI is provided with a pulse blanking time of 0.75 μs (typ.).

The motor current will not be less than the current determined by the pulse blanking time. Pay utmost attention at the time of minute current control.

Fig.1 shows the relationship between the pulse blanking time and minimum current value.

The increase or decrease in the motor current is determined by a load and a resistance of a internal winding in the motor, induced voltage, and PWM on-duty.

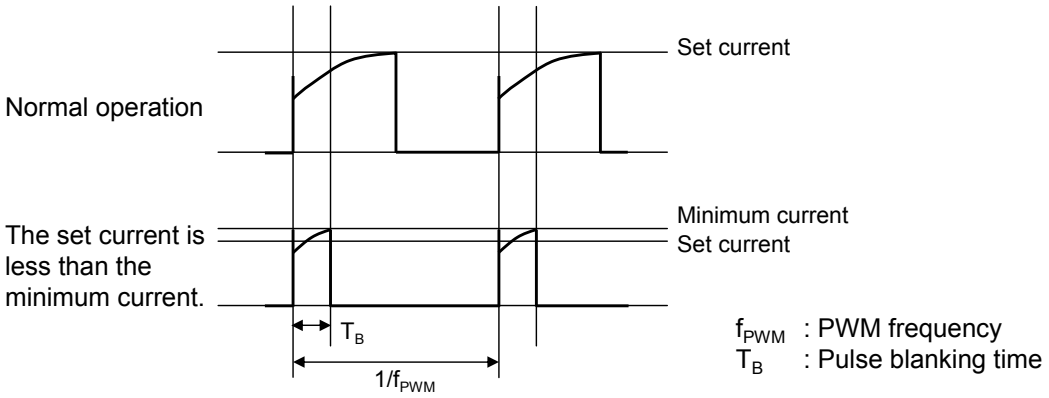


Fig. 1 RCS current waveform

2) VREF voltage

When VREF voltage is set to lower, an error detection of motor current might be caused by noise because Comp threshold voltage becomes low. Use this LSI after confirming there is no error detection when VREF voltage is less than the set value.

3) Notes on the interface

Absolute maximum ratings of Pin 19, 20, 22 and Pin 24 to Pin31 are –0.3 V to 6 V. When the current setting for a motor is large and the lead line of GND is long, the potential of GND in this LSI will rise. Take notice that there is a possibility that potential of the interface pin is negative compared with that of GND in this LSI even if 0 V is applied to the interface pin. At that time, pay attention so that the input voltage of these pins might not exceed the values which are set in the allowable voltage range.

APPLICATIONS INFORMATION (continued)

Usage Notes (continued)

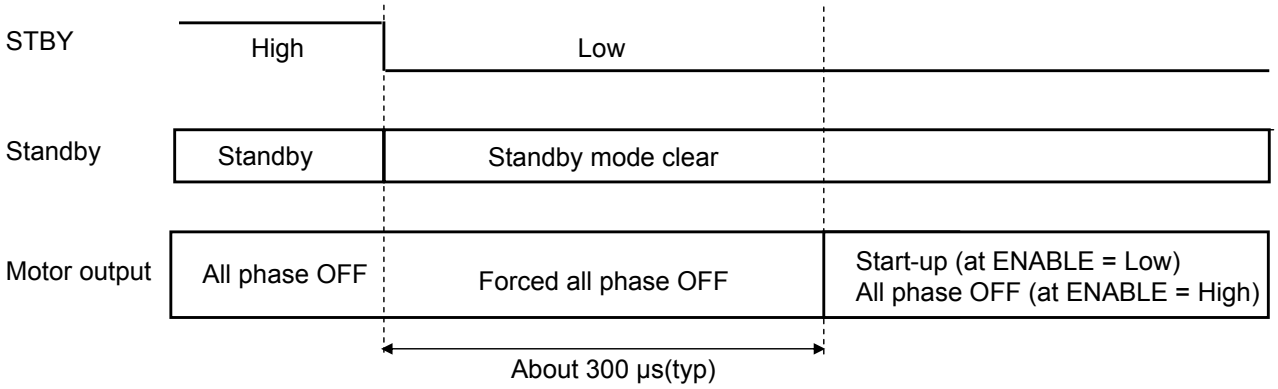
4) Notes at the clear of standby mode / the rise of VM supply

In this LSI, all phases are forced OFF for about 300 µs(typ) after the clear of standby mode or the rise of VM supply. (See the following figure.) This is why the operation mode can be started after the charge pump circuit voltage boosts efficiently at shift to operation mode from standby mode / VM supply = OFF, when the charge pump operation stops. Therefore, the excitation patterns input after the forced all phase OFF period are effect.

When the charge pump circuit rises slowly owing to that the capacitance value between VPUMP-GND is made large etc. and the booster voltage cannot rise efficiently for the forced all phase OFF, the LSI might overheat. In this case, clear the standby mode at ENABLE = High or restart after VM supply is turned ON, the booster voltage rises efficiently, and ENABLE is shifted to Low.

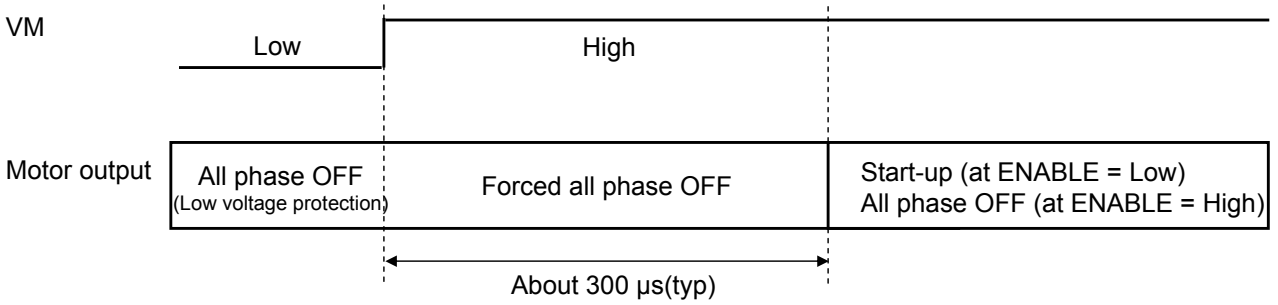
The thermal protection is same operation as that at VM supply OFF.

[In case that standby mode is cleared]



[In case that VM supply rises]

After VM supply exceeds threshold VM = 8.8 V(typ), all phases are forced OFF for about 300 µs(typ).



APPLICATIONS INFORMATION (continued)

Usage Notes(continued)

5) PWMSW, PHA1, PHB1 pins

Under conditions where VM power supply is shutdown in standby mode (STBY pin = High level), when applying approx. 0.7 V (TYP) or more to PWMSW (Pin 24), PHA1 (Pin 25), PHB1 (Pin 26), the current flows into above-mentioned pins owing to parasitic elements in the LSI and the current flowing into the above-mentioned pins varies from the current determined by pull down resistance. In addition, the current flowing into PHA1/PHA2 is 341.4 µA (impedance = approx. 9.1 kΩ) at 3.3 V, while that into PWMSW is 323.2 µA (impedance = approx. 9.7 kΩ) at 3.3 V. There is no problem that the voltage up to rating is applied to the above-mentioned pins. However, it is recommended to set the voltage applied to the above-mentioned to 0.7 V or less at shutdown of VM power supply in standby mode.

Also, in case of the voltage of above-mentioned pins > S5VOUT(Pin 21) – 0.2 V at power on to VM power supply, the current flows owing to parasitic elements in the LSI, and the current flowing into the above-mentioned pins varies (refer to Fig. 2, 3).

As the same as at standby, there is no problem that the voltage up to rating is applied to the above-mentioned pins. However, it is recommended to set the voltage applied to the above-mentioned pins to 4.3 V or less.

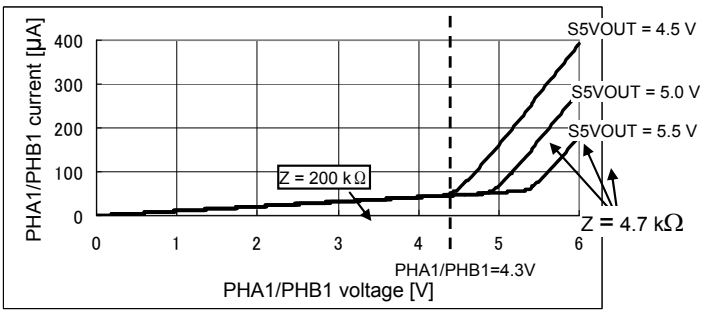


Fig. 2 Input impedance of PHA1/PHB1 at VM power supply power on

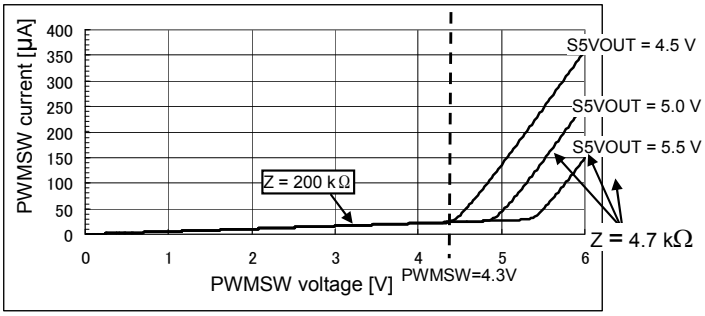
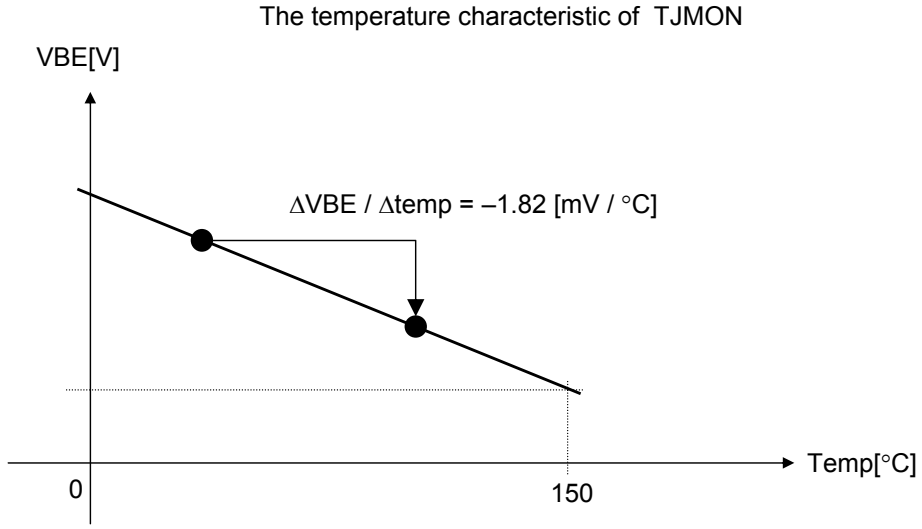


Fig. 3 Input impedance of PWMSW at VM power supply power on

APPLICATIONS INFORMATION (continued)

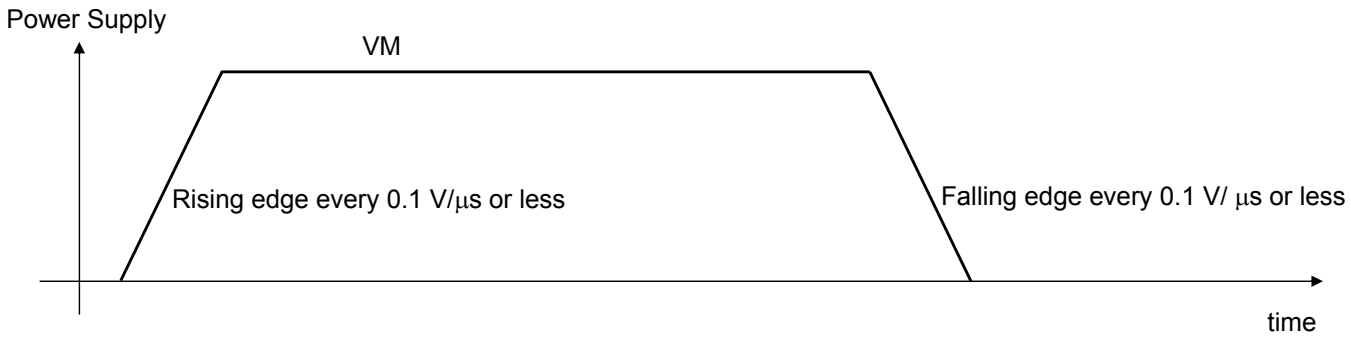
Usage Notes(continued)

6) In the case of measuring the chip temperature of the LSI, measure the voltage of TJMON (Pin 32) and presume chip temperature from following data. Use the following data as reference data. Before applying the LSI to a product, conduct a sufficient reliability test of the LSI along with the evaluation of the product with the LSI incorporated.



7) Power supply start up speed and shutdown speed

Set the rising speed to 0.1 V/μs or less for VM voltage at power on to VM (Pin 1, 15).
It is recommended that the falling speed of VM voltage is set to 0.1 V/μs or less on condition of STBY = High or ENABLE = High at shutdown. In case of shutdown at motor drive (STBY = Low and ENABLE = Low), the motor current might flow back to the power supply and supply voltage might not fall stably.
If the rising or falling speed of power supply is too high, which might cause malfunctions or destruction on the LSI. In this case, perform the long-term reliability test and confirm the sufficient evaluation for products.



APPLICATIONS INFORMATION (continued)

Usage Notes(continued)

8) RCS line

Take consideration in the following figure and the points and design PCB pattern.

(1) Point 1

Design so that the wiring to the current detection pins of this LSI (RCSA, RCSB) should be thick and short in order to lower the impedance. This is why the current cannot be detected correctly owing to the wiring impedance, and the current might not be supplied to a motor sufficiently.

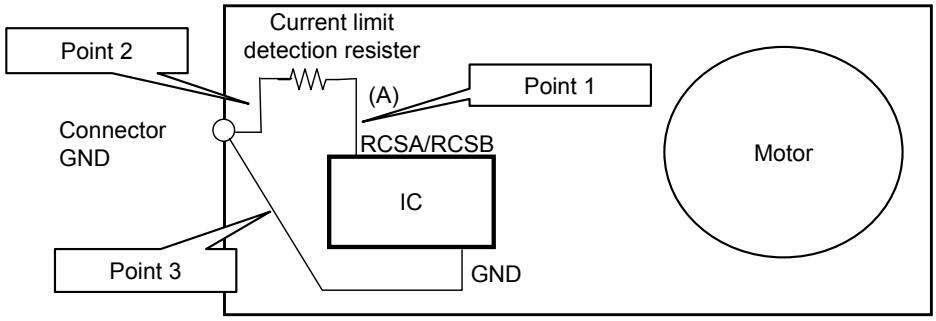
(2) Point 2

Design so that the wiring between the current detection resistor and the connector GND (Point 2 in the following figure) should be thick and short in order to lower the impedance. As the same as Point 1, a sufficient current might not be supplied due to the wiring impedance.

In addition, if there is a common impedance between GND and RCSA or RCSB, a peak detection may be detected by mistake. Therefore, connect the wiring between GND and RCSA or RCSB independently.

(3) Point 3

Connect the GND of this LSI to the connector on PCB independently. Separate the wiring which is a large current line (Point 2) from that of GND, and make these wirings with one-point shorted at the connector as the following figure. That can minimize the fluctuation of GND.



9) A high current flows into this LSI. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

A high current flows into the line between the VM1 (Pin 1) and VM2 (Pin 15) pins. Therefore, noise is generated with ease at the time of switching due to the inductance (L) of the line, which may result in the malfunctioning or destruction of the LSI. (Fig. 4)

As shown in the circuit diagram on the right-hand side, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the LSI. This makes it possible to suppress the direct VM pin voltage of the LSI. Make the settings as shown in the circuit diagram on Fig. 5 as much as possible.

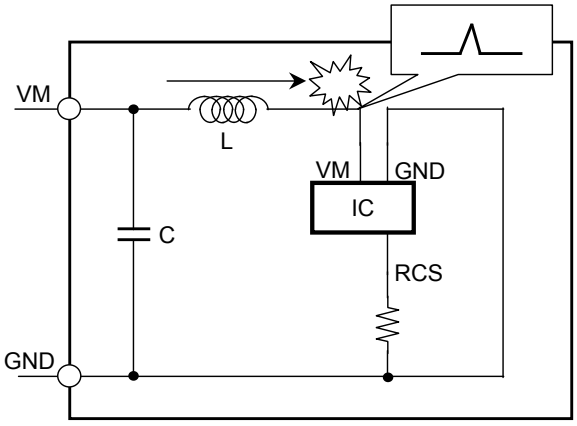


Fig. 4 Deprecated PCB

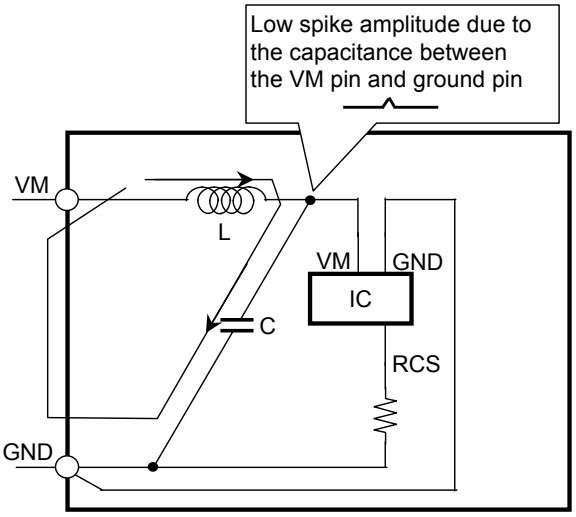


Fig. 5 Recommended PCB

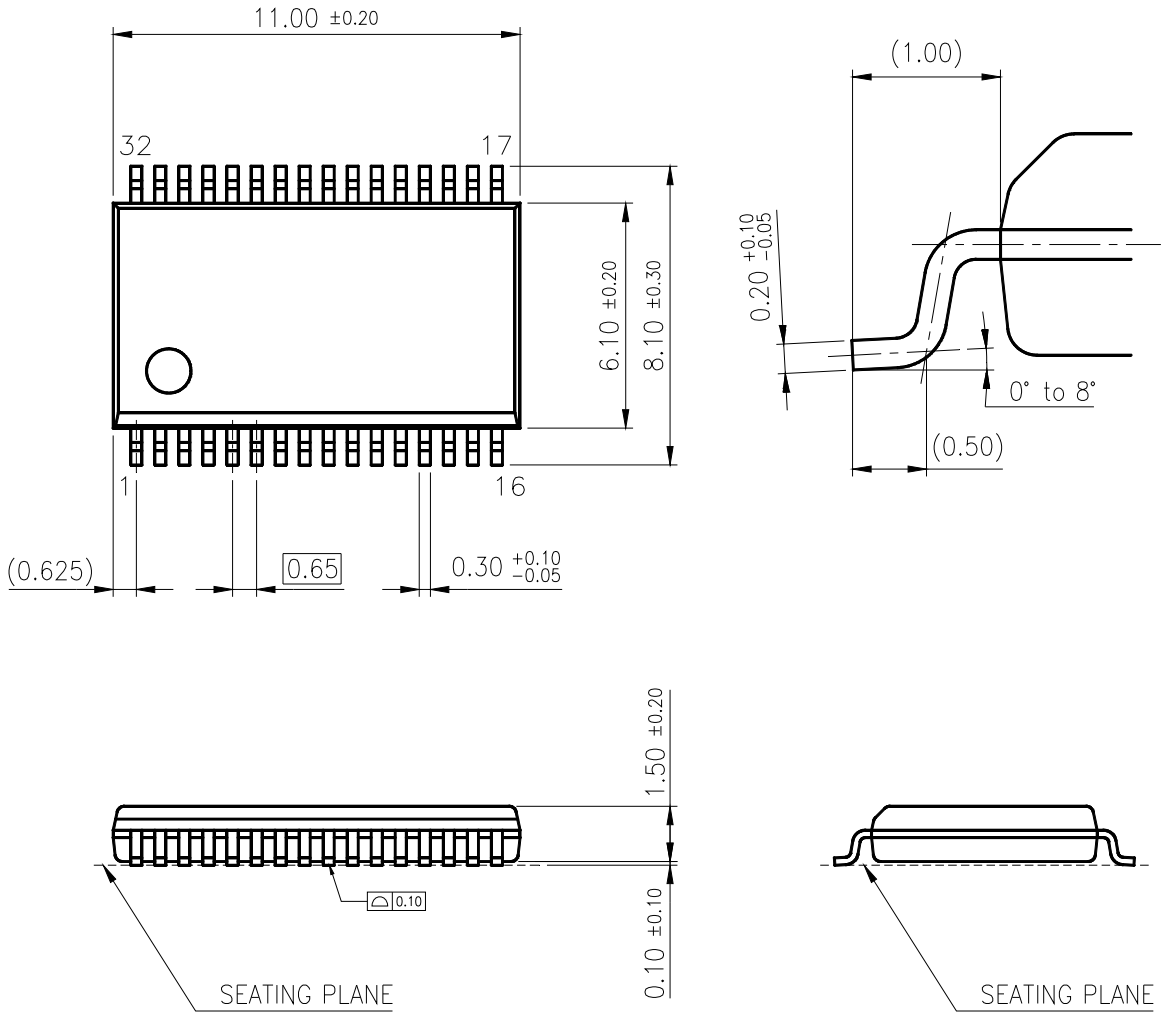
Panasonic

AN44066A

PACKAGE INFORMATION (Reference Data)

Package Code:SSOP032-P-0300B

unit:mm



Body Material	:	Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	SnBi Plating

IMPORTANT NOTICE

1.The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

2.When using the LSI for new models, verify the safety including the long-term reliability for each product.

3.When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.

4.The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

5.This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

6.This LSI is intended to be used for general electronic equipment.
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
Any applications other than the standard applications intended.
(1) Space appliance (such as artificial satellite, and rocket)
(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the LSI described in this book for any special application, unless our company agrees to your using the LSI in this book for any special application.

7.This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
Our company shall not be held responsible for any damage incurred by you or any third party as a result of or in connection with your using the LSI in automotive application, unless our company agrees to your using the LSI in this book for such application.

8.If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

9. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of your using the IC not complying with the applicable laws and regulations.

USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VM short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) . And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
Pay special attention to the following pins so that they are not short-circuited with the VM pin, ground pin, other output pin, or current detection pin.

(1) AOUT1 (Pin 13), AOUT2 (Pin 9), BOUT1 (Pin 7), BOUT2 (Pin 3)
(2) BC2 (Pin 17), VPUMP (Pin 16)
(3) VM1 (Pin 1), VM2 (Pin 15), S5VOUT(Pin 21)
(4) RCSA (Pin 11), RCSB (Pin 5)

The higher the current capacity of power supply is, the higher the possibility of the above destruction or smoke generation. Therefore, it is recommended to take safety countermeasures, such as the use of a fuse.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

10. Verify the risks which might be caused by the malfunctions of external components.

11. Perform thermal design work with consideration of a sufficient margin to keep the power dissipation based on supply voltage, load, and ambient temperature conditions. (The LSI is recommended that junctions are designed below 70% to 80% of Absolute Maximum Rating.)

USAGE NOTES (continued)

12. Set the value of the capacitor between the VPUMP and GND pins so that the voltage on the VPUMP (Pin 16) will not exceed 43 V in any case regardless of whether it is a transient phenomenon or not while the motor standing by is started.

13.This LSI employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the LSI is apt to generate noise that may cause the LSI to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the S5VOUT and GND pins must be 0.1 μF and the one for power supply stabilization between the VM and GND pins must be a minimum of 47 μF (recommendation) and as close as possible to the LSI so that PWM noise will not cause the LSI to malfunction or have fatal damage.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Please consult with our sales staff in advance for information on the following applications, moreover please exchange documents separately on terms of use etc.: Special applications (such as for in-vehicle equipment, airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, medical equipment and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
Unless exchanging documents on terms of use etc. in advance, it is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. We do not guarantee quality for disassembled products or the product re-mounted after removing from the mounting board.
When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) When reselling products described in this book to other companies without our permission and receiving any claim of request from the resale destination, please understand that customers will bear the burden.

No.010618