

1:4 Clock Fanout Buffer

Features

- Low-voltage operation
- $V_{DD} = 3.3\text{ V}$
- 1:4 fanout
- Single-input configurable for
 - LVDS, LVPECL, or LVTTTL
 - Four differential pairs of LVDS outputs
- Drives 50 or 100 Ω load (selectable)
- Low input capacitance
- 85 ps typical output-to-output skew
- < 4 ns typical propagation delay
- Does not exceed Bellcore 802.3 standards
- Operation at \Rightarrow 350 MHz – 700 Mbps
- Industrial versions available
- Packages available include TSSOP

Functional Description

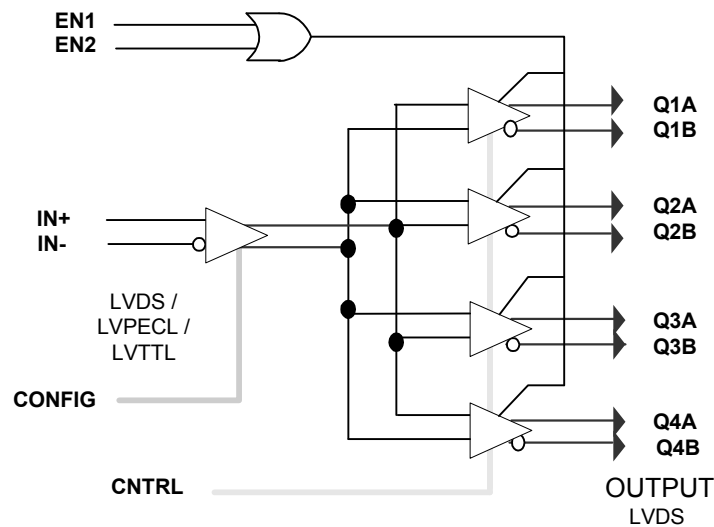
The Cypress CY2 series of network circuits is produced using advanced 0.35 micron CMOS technology, achieving the industry's fastest logic.

The Cypress CY2DL814 fanout buffer features a single LVDS, LVPECL, or LVTTTL compatible input and four LVDS output pairs.

Designed for data-communication clock management applications, the fanout from a single input reduces loading on the input clock.

The CY2DL814 is ideal for both level translations from single ended to LVDS and/or for the distribution of LVDS-based clock signals. The Cypress CY2DL814 has configurable input and output functions. The input can be selectable for LVPECL/LVTTTL or LVDS signals while the output driver's support standard and high drive LVDS. Drive either a 50 Ω or 100 Ω line with a single part number/device.

Logic Block Diagram

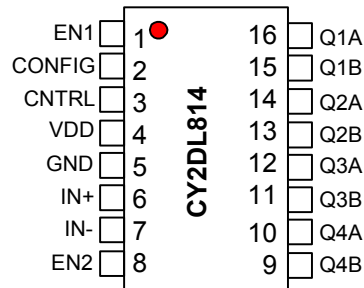


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Pin Configuration

Figure 1. 16-pin TSSOP pinout



Pin Description

Pin Number	Pin Name	Pin Standard Interface	Description
6,7	IN+, IN-	Configurable	Differential input pair or single line. LVPECL default. See config below.
3	CNTRL	LVTTL/LVCMOS	Converts into a High drive driver from a standard LVDS. Standard drive (logic = 0) B/High drive/Bus (logic = 1)
2	CONFIG	LVTTL/LVCMOS	Converts inputs (IN+/IN-), (EN, EN#) from the default LVPECL/LVDS (logic = 0) To LVTTL/LVCMOS (logic = 1)
1,8	EN1, EN2	LVTTL/LVCMOS	Enable/disable logic. See EN1 EN2 Function Table – Differential Input Mode on page 4 below for details.
16, 15, 14, 13, 12, 11, 10, 9	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B	LVDS	Differential outputs.
4	V _{DD}	POWER	Positive supply voltage
5	G _{ND}	POWER	Ground

Functional Overview

EN1 EN2 Function Table – Differential Input Mode

Enable Logic		Input		Outputs	
EN1	EN2	IN+	IN–	QnA	QnB
H	X	H	L	H	L
H	X	L	H	L	H
X	L	H	L	H	L
X	L	L	H	L	H
L	H	X	X	Z	Z

Output Drive Control for Standard and Bus/B/High Drive B

CNTRL Pin 3 Binary Value	Drive STD	Impedance	Output Voltage Value
0	Standard	100 Ω	V0 = Voutput
		50 Ω	V = 1/2 × V0
1	High Drive/Bus/B	100 Ω	V = 2 × V0
		50 Ω	V = V0

Input Receiver Configuration for Differential or LVTTTL/LVCMOS

CONFIG Pin 2 Binary Value	Input Receiver Family	Input Receiver Type
1	LVTTTL in LVCMOS	Single-ended, non-inverting, inverting, void of bias resistors
0	LVDS	Low-voltage differential signaling
	LVPECL	Low-voltage Pseudo (Positive) emitter coupled logic

Function Control of the TTL Input Logic Used to Accept or Invert the Input Signal

LVTTTL/LVCMOS Input Logic			
Input Condition		Input Logic	Output Logic Q Pins, Q1A or Q1
Ground	IN– Pin 7		
	IN+ Pin 6	Input	True
V _{CC}	IN– Pin 7		
	IN+ Pin 6	Input	Invert
Ground	IN+ Pin 6		
	IN– Pin 7	Input	True
V _{CC}	IN+ Pin 6		
	IN– Pin 7	Input	Invert

Maximum Ratings

Exceeding maximum ratings ^[1, 2] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature -40 °C to +85 °C

Supply voltage to ground potential
(Inputs and V_{CC} only) -0.3 V to 4.6 V

Supply voltage to ground potential
(Outputs only) -0.3 V to V_{DD} + 0.3 V

DC input voltage -0.3 V to V_{DD} + 0.3 V

DC output voltage -0.3 V to V_{DD} + 0.9 V

Power Supply Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I _{CCD}	Dynamic power supply current	V _{DD} = Max, Input toggling 50% duty cycle, Outputs open	–	1.5	2.0	mA/ MHz
I _C	Total power supply current	V _{DD} = Max, Input toggling 50% duty cycle, Outputs open, f _L = 100 MHz	–	90	100	mA

DC Electrical Characteristics

3.3 V – LVDS Input

Parameter	Description	Conditions		Min	Typ	Max	Unit
V _{ID}	Magnitude of differential input voltage			100	–	600	mV
V _{IC}	Common-mode of differential input voltage V _{ID} (min and max)			I _{VID} /2	2.4 – (I _{VID} /2)		V
V _{IH}	Input high voltage	Guaranteed logic high level	Config / Control pins	2	–	–	V
V _{IL}	Input low voltage	Guaranteed logic low level		–	–	0.8	V
I _{IH}	Input high current	V _{DD} = Max	V _{IN} = V _{DD}	–	±10	±20	µA
I _{IL}	Input low current	V _{DD} = Max	V _{IN} = V _{SS}	–	±10	±20	µA
I _I	Input high current	V _{DD} = Max, V _{IN} = V _{DD} (max)		–	–	±20	µA

DC Electrical Characteristics

3.3 V – LVPECL Input

Parameter	Description	Conditions		Min	Typ	Max	Unit
V _{ID}	Differential input voltage p-p	Guaranteed logic high level		400	–	2600	mV
V _{CM}	Common-mode voltage			1.65	–	2.25	V
I _{IH}	Input high current	V _{DD} = Max	V _{IN} = V _{DD}	–	±10	±20	µA
I _{IL}	Input low current	V _{DD} = Max	V _{IN} = V _{SS}	–	±10	±20	µA
I _I	Input high current	V _{DD} = Max, V _{IN} = V _{DD} (Max)		–	–	±20	µA

Notes

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Characteristics

3.3 V – LVTTTL/LVCMOS Input

Parameter	Description	Conditions		Min	Typ	Max	Unit
V _{IH}	Input high voltage	Guaranteed logic high level		2	–	–	V
V _{IL}	Input low voltage	Guaranteed logic low level		–	–	0.8	V
I _{IH}	Input high current	V _{DD} = Max	V _{IN} = 2.7 V	–	–	1	μA
I _{IL}	Input low current	V _{DD} = Max	V _{IN} = 0.5 V	–	–	–1	μA
I _I	Input high current	V _{DD} = Max, V _{IN} = V _{DD} (Max)		–	–	20	μA
V _{IK}	Clamp diode voltage	V _{DD} = Min, I _{IN} = –18 mA		–	–0.7	–1.2	V
V _H	Input hysteresis			–	80		mV

DC Electrical Characteristics

3.3 V – LVDS Output

Parameter	Description	Conditions		Min	Typ	Max	Unit
I _{V_{OD}}	Differential output voltage p-p	V _{DD} = 3.3 V, V _{IN} = V _{IH} or V _{IL}	RL = 100 ohm	0.25	–	0.45	V
VOC(SS)	Steady-state common-mode output voltage			–	–	226	mV
Delta VOC(SS)	Change in VOC(SS) between logic states			–50	3	50	mV
VOC(PP)	Peak to peak common mode output voltage			–	–	150	mV
I _{OS}	Output short circuit	QA = 0 V or QB = 0 V		–	–	–20	mA
V _{oh}	Output voltage high		RL = 100 ohm	–	–	1475	mV
V _{ol}	Output voltage low			925	–	–	mV

AC Parameters

Parameter	Description	Conditions		Min	Typ	Max	Unit
Rise time	Pin control (pin 3) logic is "FALSE" defaulting to 100 ohm output drivers. Differential 20% to 80%	CL=10 pF RL and CL to GND 3 CL = C _{intrinsic} and C _{external}	RL = 100 ohm	–	–	1.4	ns
Fall time				–	–	1.4	ns
Rise time	Pin control (pin 3) logic is "True" defaulting to 50 ohm output drivers. Differential 20% to 80%	CL=10 pF RL and CL to GND 3 CL = C _{intrinsic} and C _{external}	RL = 50 ohm Output boost	–	350	600	ps
Fall time				–	350	600	ps

AC Switching Characteristics

@ 3.3 V (V_{DD} = 3.3 V ± 5%, Temperature = –40 °C to +85 °C)

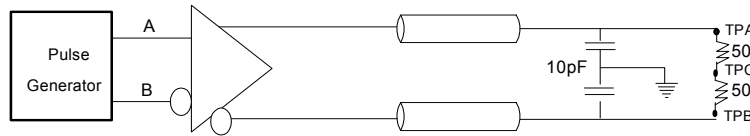
Parameter	Description	Conditions	Min	Typ	Max	Unit
IN [+,-] to Q[A,B] Data and Clock Speed						
t _{PLH}	Propagation delay – Low to High	V _{OD} = 100 mV	3	4	5	ns
t _{PHL}	Propagation delay – High to Low		3	4	5	ns
T _{pd}	Propagation delay		3	4	5	ns
IN [1,2] to Q[A,B] Control Speed						
T _{Pe}	Enable (EN) to functional operation		–	–	6	ns
T _{pd}	Functional operation to disable		–	–	5	ns
Q[A,B] Output Skews						
t _{SK(0)}	Output Skew: Skew between outputs of the same package (in phase)		–	0.085	0.2	ns
t _{SK(p)}	Pulse Skew: Skew between opposite transitions of the same output (t _{PHL} –t _{PLH})		–	0.2	–	ns
t _{SK(t)}	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	V _{ID} = 100 mV	–	–	1	ns

High Frequency Parametrics

Parameter	Description	Conditions	Min	Typ	Max	Unit
F _{max}	Maximum frequency V _{DD} = 3.3 V	50% duty cycle tW(50–50) Standard load circuit.	–	–	400	MHz
F _{max(20)}	Maximum frequency V _{DD} = 3.3 V	20% duty cycle tW(50–50) LVPECL input V _{IN} = V _{IH(Max)} /V _{IL(Min)} V _{OUT} = V _{OH(Min)} /V _{OL(Max)} (Limit)	–	–	200	MHz
TW	Minimum pulse V _{DD} = 3.3 V	LVPECL Input V _{IN} = V _{IH(Max)} /V _{IL(Min)} , F = 100 MHz V _{OUT} = V _{OH(Min)} /V _{OL(Max)} (Limit)	1	–	–	ns

Switching Waveforms

Figure 2. Differential Receiver to Driver Propagation Delay and Driver Transition Time [3, 4, 5, 6]



Standard Termination

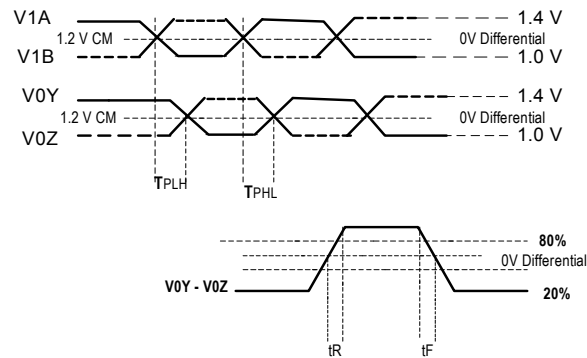
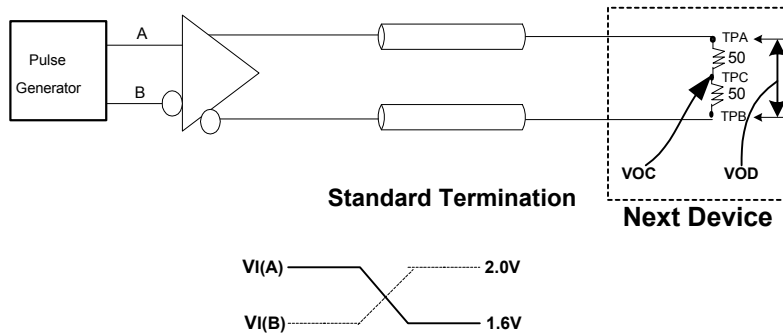


Figure 3. Test Circuit and Voltage Definitions for the Driver Common-mode Output Voltage [3, 4, 5, 6]

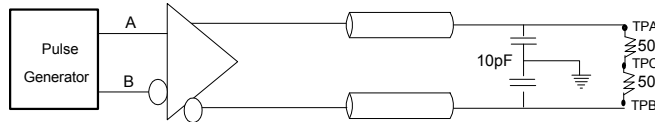


Notes

- All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse rate = 50 Mpps; pulse width = 10 ± 0.2 ns.
- $R_L = 50 \text{ ohm} \pm 1\%$ $Z_{line} = 50 \text{ ohm}$ 6".
- CL includes instrumentation and fixture capacitance within 6 mm of the UT.
- TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to $V_{DD} - 2$.

Switching Waveforms (continued)

Figure 4. Test Circuit and Voltage Definitions for the Differential Output Signal [7, 8, 9, 10]



Standard Termination

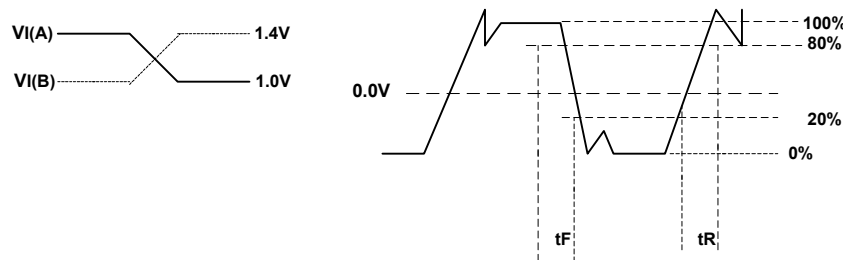


Figure 5. LVCMOS/LVTTL Single-ended Input Value [11]

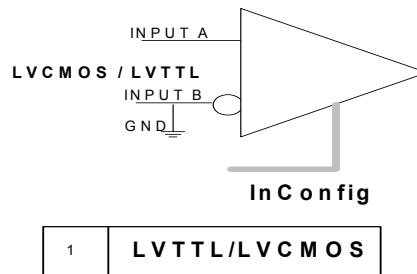
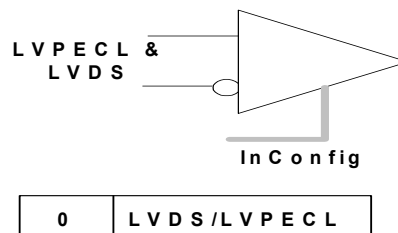


Figure 6. LVPECL or LVDS Differential Input Value [12]



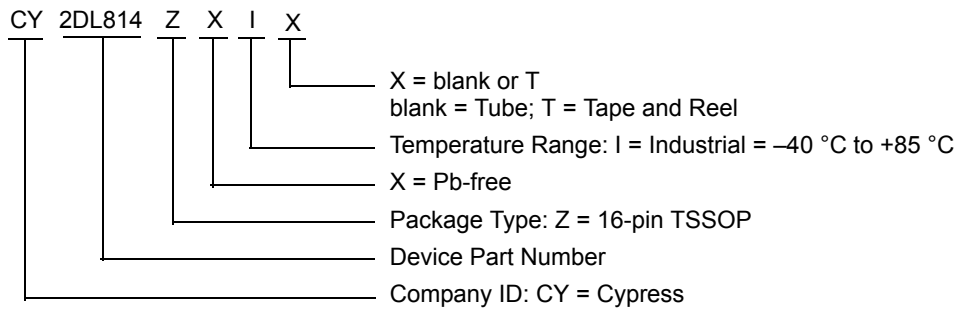
Notes

7. All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse rerate = 50 Mpps; pulse width = 10 ± 0.2 ns.
8. $R_L = 50 \text{ ohm} \pm 1\%$ $Z_{line} = 50 \text{ ohm}$ 6".
9. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
10. TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to V_{DD-2} .
11. LVCMOS/LVTTL single ended input value. Ground either input: when on the B side then non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See [Table](#) .
12. LVPECL or LVDS differential input value.

Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY2DL814ZXI	16-pin TSSOP	Industrial, -40 °C to 85 °C
CY2DL814ZXIT	16-pin TSSOP – Tape and Reel	Industrial, -40 °C to 85 °C

Ordering Code Definitions



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTTL	Low Voltage Transistor-Transistor Logic
TSSOP	Thin-Shrink Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DL814 ComLink™ Series, 1:4 Clock Fanout Buffer Document Number: 38-07057				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	115362	07/10/02	EHX	New data sheet.
*A	122744	12/14/02	RBI	Updated Maximum Ratings : Added Note 2 and referred the same note in “maximum ratings”.
*B	384077	See ECN	RGL	Updated AC Switching Characteristics : Added typical values. Updated Ordering Information : Updated part numbers.
*C	2899846	03/26/10	KVM	Updated Ordering Information : Updated part numbers. Updated Package Drawing and Dimensions : Removed spec 51-85068 *B. spec 51-85091 – Changed revision from *A to *B.
*D	3085165	11/12/2010	BASH	Added Ordering Code Definitions under Ordering Information . Updated Package Drawing and Dimensions : spec 51-85091 – Changed revision from *B to *C. Minor edits. Updated to new template.
*E	4203988	11/27/2013	CINM	Updated Package Drawing and Dimensions : spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*F	5563337	12/22/2016	TAVA	Updated Package Drawing and Dimensions : spec 51-85091 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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