NCP1601A, NCP1601B

Compact Fixed Frequency Discontinuous or Critical Conduction Voltage Mode Power Factor Correction Controller

The NCP1601 is a controller designed for Power Factor Correction (PFC) boost circuits. The device operates in fixed−frequency Discontinuous Conduction Mode (DCM) and variable−frequency Critical Conduction Mode (CRM) and takes advantages from both operating modes. DCM limits the maximum switching frequency. It simplifies the front−ended EMI filter design. CRM limits the maximum currents of the boost stage diode, MOSFET and inductor. It reduces the costs and improves the reliability of the circuit. This device substantially exhibits unity power factor while operating in DCM and CRM. The NCP1601 minimizes the required number of external components. It incorporates high safety protection features that make the NCP1601 suitable for robust and compact PFC stages.

Features

- Near−Unity Power Factor in DCM or CRM
- Voltage−Mode Operation
- Low Startup and Shutdown Current Consumption
- Programmable Switching Frequency for DCM
- Synchronization Capability
- Overvoltage Protection (107% of Nominal Output Level)
- Undervoltage Protection or Shutdown (8% of Nominal Output Level)
- Programmable Overcurrent Protection
- Thermal Shutdown with Hysteresis (95/140°C)
- Two V_{CC} Undervoltage Lockout Hysteresis Options: 4.75 V for NCP1601A and 1.5 V for NCP1601B
- Pb−Free Packages are Available

Typical Applications

- Electronic Light Ballast
- AC Adapters
- TV & Monitors
- Mid−Power Applications

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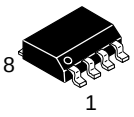
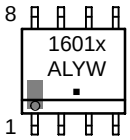
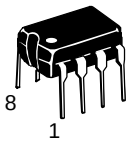
MARKING DIAGRAM

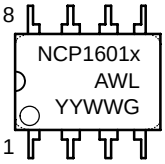


SOIC−8
D SUFFIX
CASE 751



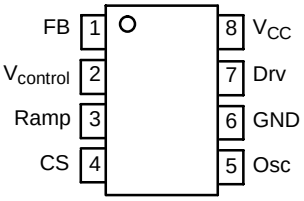


PDIP−8
N SUFFIX
CASE 626



x	= A or B
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪	= Pb−Free Package
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

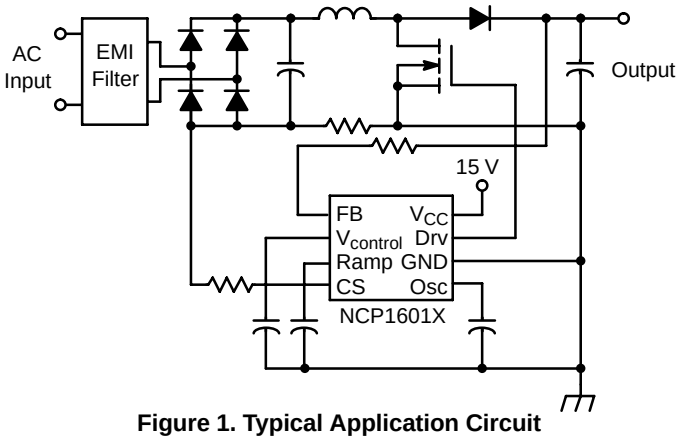


Figure 1. Typical Application Circuit

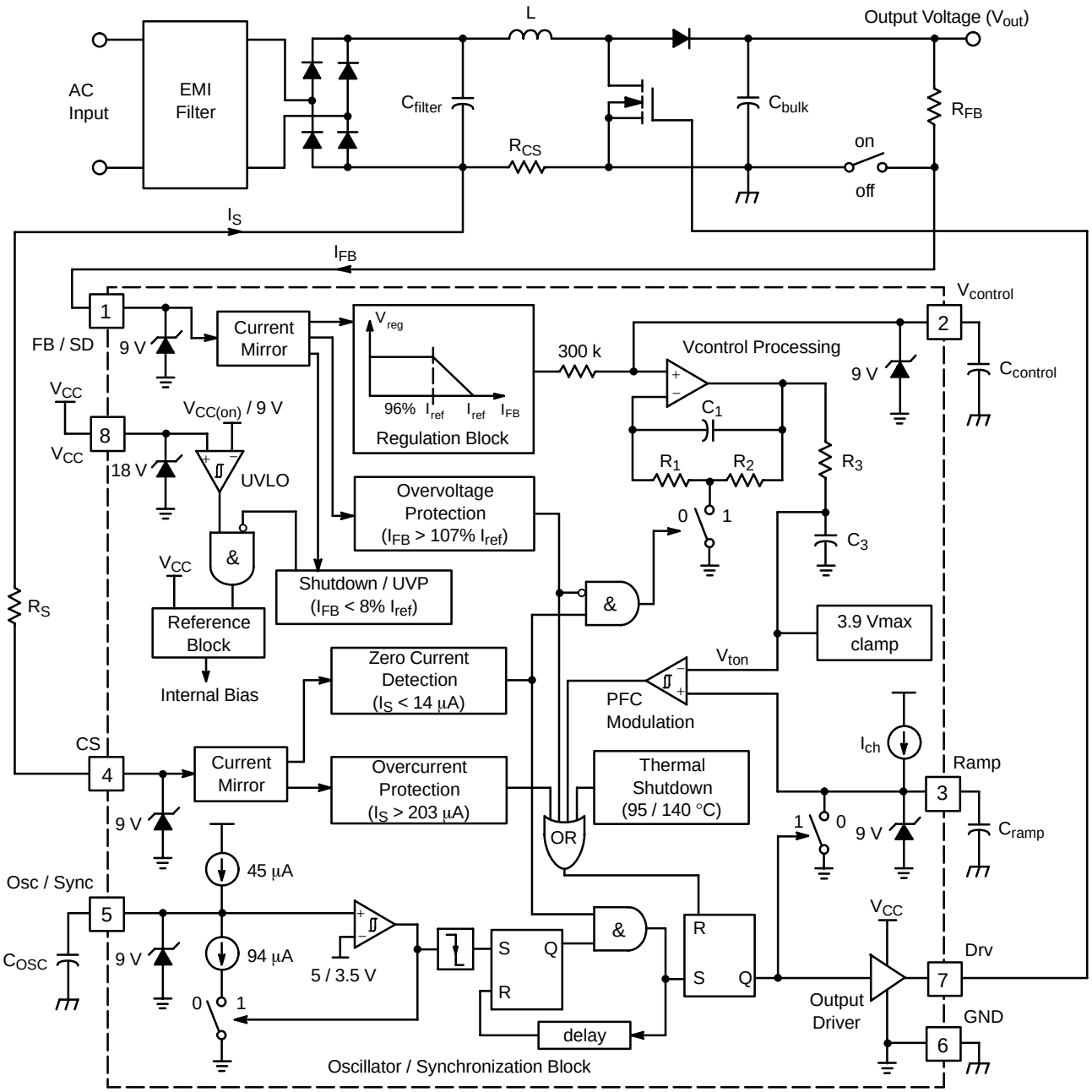


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function	Function
1	FB	Feedback / Shutdown	This pin receives a current I_{FB} which is proportional to the PFC circuit output voltage. The current is for the output regulation, output Overvoltage Protection (OVP), and output undervoltage protection (UVP). When I_{FB} goes above 107% I_{ref}, OVP is activated and the Drive Output is disabled. When I_{FB} goes below 8% I_{ref}, the device enters a low−current consumption shutdown mode.
2	$V_{control}$	Control	The voltage of this pin $V_{control}$ directly controls the input impedance and hence the power factor of the circuit. This pin is connected to an external capacitor to limit the control voltage $V_{control}$ bandwidth typically below 20 Hz to achieve Power Factor Correction.
3	Ramp	Ramp	This pin is connected to an external capacitor to set a ramp signal. The capacitor value directly affects the input impedance of the PFC circuit and hence the maximum input power.
4	CS	Current Sense	This pin sources a current I_S which depends on the inductor current and an offset voltage. The current is for Overcurrent Protection (OCP) and zero current detection. When I_S is above 200 μA, OCP is activated and the Drive Output is disabled. When I_S is below 14 μA, the circuit detects a zero current. This information is used by the on−time modulation arrangement and by the oscillator block.
5	Osc	Oscillator / Synchronization	In oscillator mode, this pin is connected to an external capacitor to set the oscillator frequency of the DCM operation. In synchronization mode, this pin is connected to an external driving signal. The positive edge of the drive output is synchronized to the negative edge of the external signal in DCM operation. If the inductor current is non−zero at the end of a switching period, the output drive is not allowed to turn on. CCM operation is prohibited. Instead, the circuit operates in CRM in this case.
6	GND	The IC ground	−
7	Drv	Drive Output	This pin provides an output to an external MOSFET.
8	V_{CC}	Supply Voltage	This pin is the positive supply of the device. The operating range is between 9 V and 18 V with UVLO start threshold 13.75 V for NCP1601A and 10.5 V for NCP1601B.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
FB, $V_{control}$, Ramp, CS, Osc Pins (Pins 1−5)			
Maximum Voltage Range	V_{max}	−0.3 to +9	V
Maximum Current	I_{max}	100	mA
Drive Output (Pin 7)			
Maximum Voltage Range	V_{max}	−0.3 to +18	V
Maximum Current Range (Note 2)	I_{max}	−500 to +750	mA
Power Supply Voltage (Pin 8)			
Maximum Voltage Range	V_{max}	−0.3 to +18	V
Maximum Current	I_{max}	100	mA
Power Dissipation and Thermal Characteristics			
P suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A=70 °C	P_D	800	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	100	°C/W
D suffix, Plastic Package, Case 751			
Maximum Power Dissipation @ T_A=70 °C	P_D	450	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	178	°C/W
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

A. This device series contains ESD protection and exceeds the following tests:
Pins 1−8: Human Body Model 2000 V per MIL−STD−883, Method 3015.
Machine Model Method 200 V.

B. This device contains Latchup protection and exceeds ±100 mA per JEDEC Standard JESD78.

1. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C. For min/max values, T_J = −40°C to +125°C, V_{CC} = 15 V, $V_{control}$ = 100 nF, Ramp = 100 pF, Osc = 220 pF unless otherwise specified)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Oscillator Frequency (Osc = 220 pF to GND)	5	f_{osc}	52	58	64	kHz
Internal Capacitance of the Oscillator Pin	5	$C_{osc(int)}$	−	36	−	pF
Maximum Oscillator Switching Frequency	5	$f_{osc(max)}$	−	405	−	kHz
Oscillator Discharge Current (Osc = 5.5 V)	5	I_{odch}	40	49	60	μA
Oscillator Charge Current (Osc = 3 V)	5	I_{och}	40	45	60	μA
Comparator Lower Threshold (Osc = 220 pF to GND) (Note 3)	5	$V_{sync(L)}$	3.0	3.5	4.0	V
Comparator Upper Threshold (Osc = 220 pF to GND)	5	$V_{sync(H)}$	4.5	5	5.5	V
Synchronization Pulse Width for Detection	5	$t_{sync(min)}$	500	−	−	ns
Synchronization Propagation Delay	5	$t_{sync(d)}$	−	371	−	ns
GATE DRIVE						
Gate Drive Resistor Output High and Draw 100 mA out of Drv Pin (I_{source} = 100 mA) Output Low and Insert 100 mA into Drv Pin (I_{sink} = 100 mA)	7	 R_{OH} R_{OL}	 5 2	 11.6 7.2	 20 18	 Ω Ω
Gate Drive Rise Time from 1.5 V to 13.5 V (Drv = 1 nF to GND)	7	t_r	−	53	−	ns
Gate Drive Fall Time from 13.5 V to 1.5 V (Drv = 1 nF to GND)	7	t_f	−	32	−	ns
FEEDBACK / OVERVOLTAGE PROTECTION / UNDERVOLTAGE PROTECTION						
Reference Current	1	I_{ref}	192	203	208	μA
Regulation Block Ratio	1	I_{regL} / I_{ref}	95	96	97	%
$V_{control}$ Pin Internal Resistor	2	$R_{control}$	−	300	−	kΩ
Maximum Control Voltage (I_{FB} = 100 μA)	2	$V_{control(max)}$	0.95	1.05	1.15	V
Feedback Pin Voltage (I_{FB} = 100 μA)	1	V_{FB1}	−	3	−	V
Overvoltage Protection Current Ratio	1	I_{OVP} / I_{ref}	104	107	−	%
Overvoltage Protection Current	1	I_{OVP}	−	217	225	μA
Undervoltage Protection Current Ratio	1	I_{UVP} / I_{ref}	4	8	15	%
CURRENT SENSE						
Current Sense Pin Offset Voltage (I_S = 100 μA)	4	V_S	−	4	−	mV
Overcurrent Protection Level	4	$I_{S(OCP)}$	190	203	210	μA
Current Sense Pin Offset Voltage at Overcurrent Level	4	$V_{S(OCP)}$	0	3.2	20	mV
Zero Current Detection Level	4	$I_{S(ZCD)}$	9	14	19	μA
Current Sense Pin Offset Voltage at Zero Current Level	4	$V_{S(ZCD)}$	0	7.5	20	mV
Zero Current Sense Resistor ($R_{S(ZCD)}$ = $V_{S(ZCD)}$ / $I_{S(ZCD)}$)	4	$R_{S(ZCD)}$	−	0.536	1	kΩ
RAMP						
Charging Current (Ramp = 0 V)	3	I_{ch}	95	100	105	μA
Maximum Power Resistance (R_{power} = $V_{control(max)}$ / I_{ch})	3	R_{power}	9.5	10.5	11.5	kΩ
Internal Clamping of Voltage V_{ton}	−	$V_{ton(max)}$	−	3.9	−	V
Internal Capacitance of the Ramp Pin	3	$C_{ramp(int)}$	−	20	−	pF
Ramp Pin Sink Resistance (Osc = 0 V, Ramp = 1 mA sourcing)	3	R_{ramp}	−	71.5	−	Ω
THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 4)	−	T_{SD}	140	−	−	°C
Thermal Shutdown Hysteresis	−	T_H	−	45	−	°C

2. Comparator lower threshold is also the synchronization threshold.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C. For min/max values, T_J = −40°C to +125°C, V_{CC} = 15 V, $V_{control}$ = 100 nF, Ramp = 100 pF, Osc = 220 pF unless otherwise specified)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
Startup Threshold (UVLO) – NCP1601A	8	$V_{CC(on)}$	12.5	13.75	15	V
Startup Threshold (UVLO) – NCP1601B			9.6	10.5	11.4	V
Minimum Voltage for Operation After Turn−On	8	$V_{CC(off)}$	8.25	9	9.75	V
UVLO Hysteresis – NCP1601A	8	$V_{CC(H)}$	4	4.75	−	V
UVLO Hysteresis – NCP1601B			1	1.5	−	V
Power Supply Current:	8					
Startup (V_{CC} = $V_{CC(on)}$ – 0.2 V)		I_{stup}	−	17	40	μA
Operating (V_{CC} = 15 V, Drv = open, Osc = 220 pF)		I_{CC1}	−	2.7	5	mA
Operating (V_{CC} = 15 V, Drv = 1 nF to GND, Osc = 220 pF)		I_{CC2}	−	3.7	5	mA
Shutdown (V_{CC} = 15 V, I_{FB} = 0 A)		I_{stdn}	−	24	50	μA

TYPICAL CHARACTERISTICS

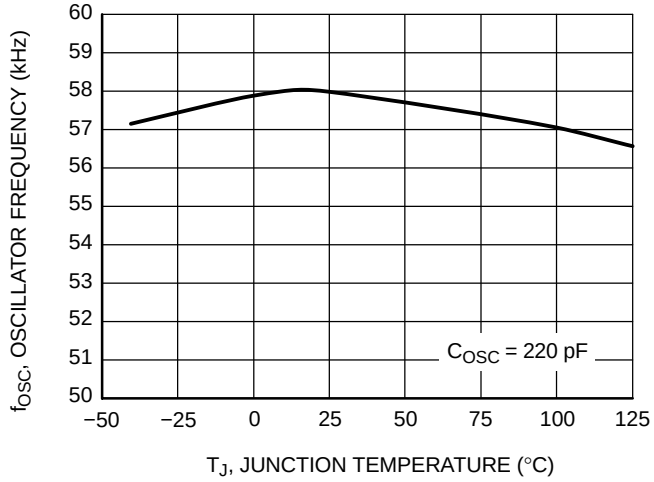


Figure 3. Oscillator Frequency vs. Temperature

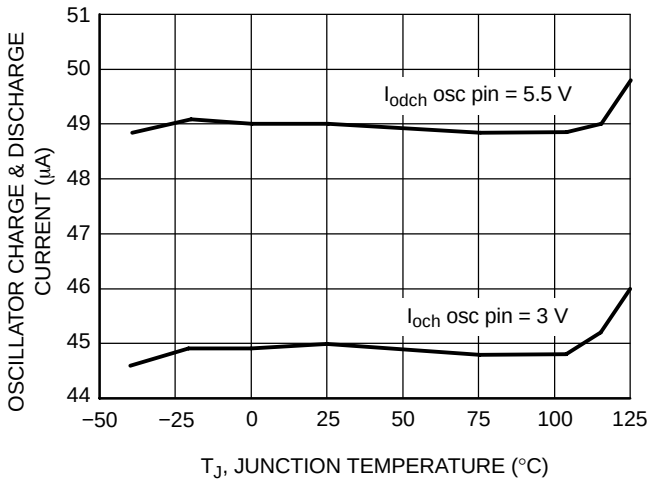


Figure 4. Oscillator Charge and Discharge Current vs. Temperature

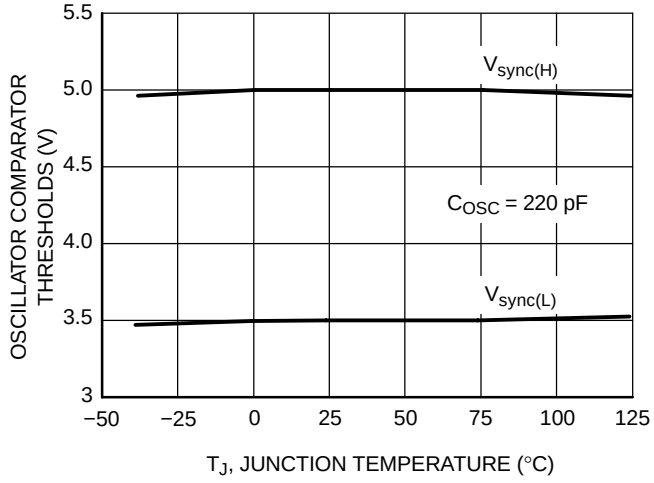


Figure 5. Oscillator Comparator Thresholds vs. Temperature

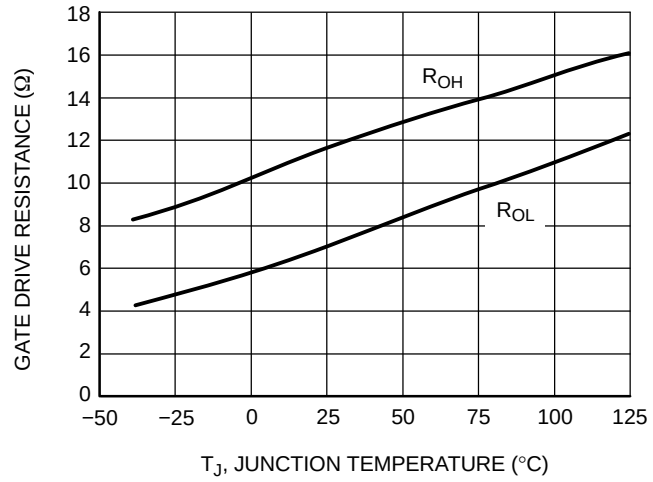


Figure 6. Drive Output Resistance vs. Temperature

TYPICAL CHARACTERISTICS

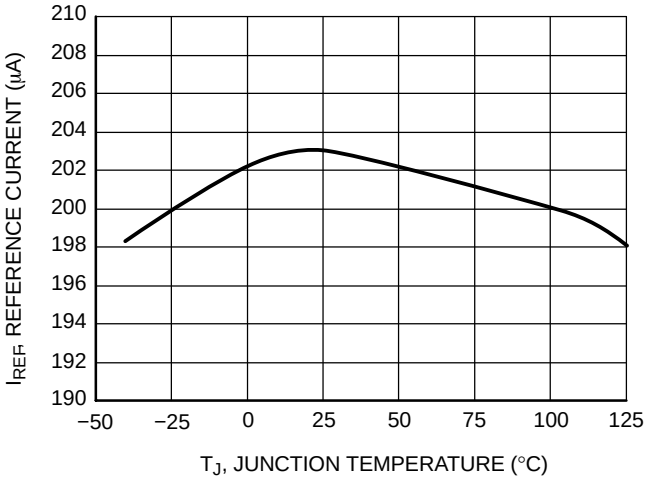


Figure 7. Reference Current vs. Temperature

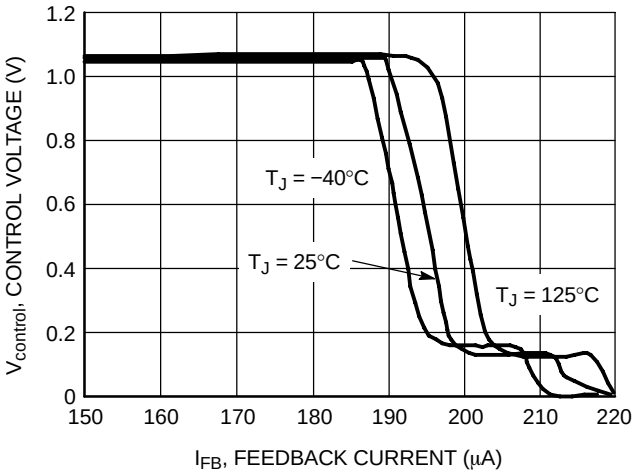


Figure 8. Regulation Block Transfer Function

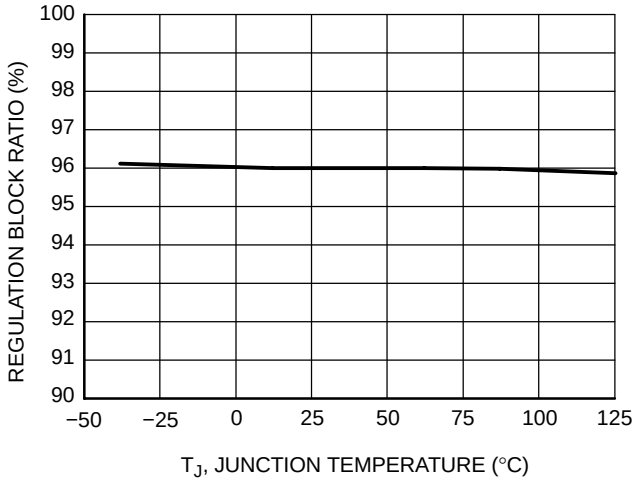


Figure 9. Regulation Block Ratio vs. Temperature

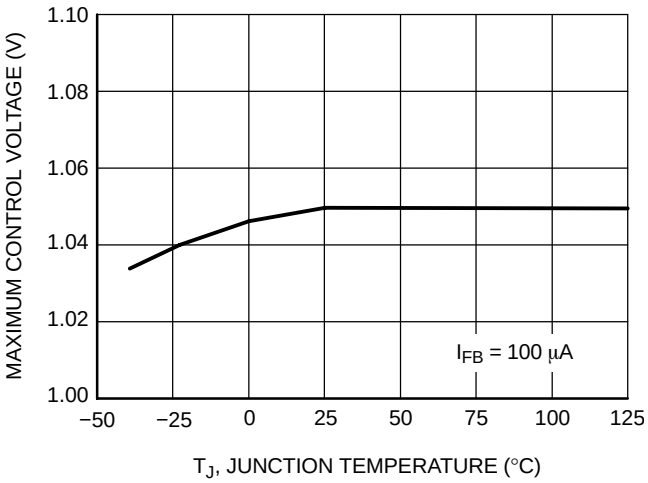


Figure 10. Maximum Control Voltage vs. Temperature

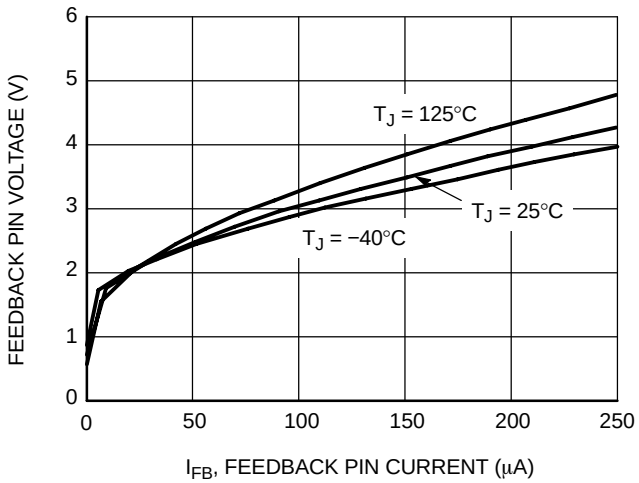


Figure 11. Feedback Pin Voltage vs. Feedback Current

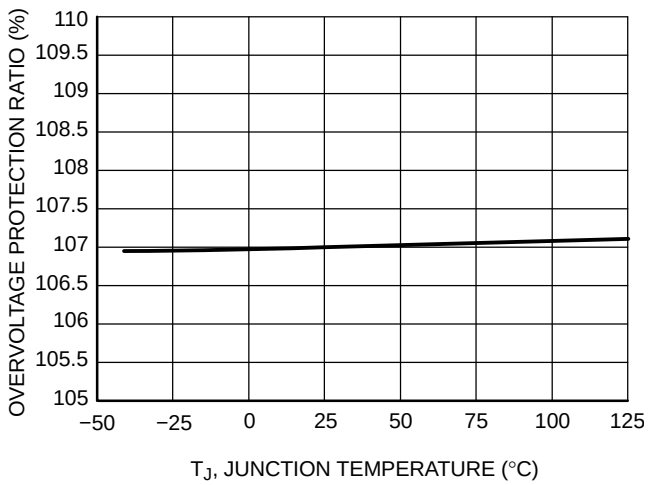


Figure 12. Overvoltage Protection Ratio vs. Temperature

TYPICAL CHARACTERISTICS

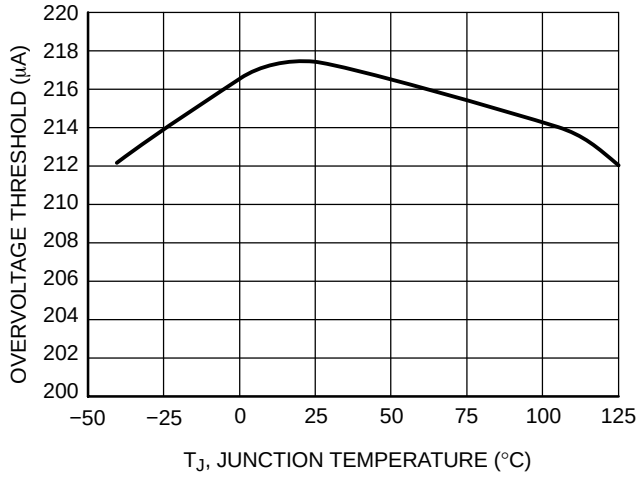


Figure 13. Overvoltage Protection Threshold vs. Temperature

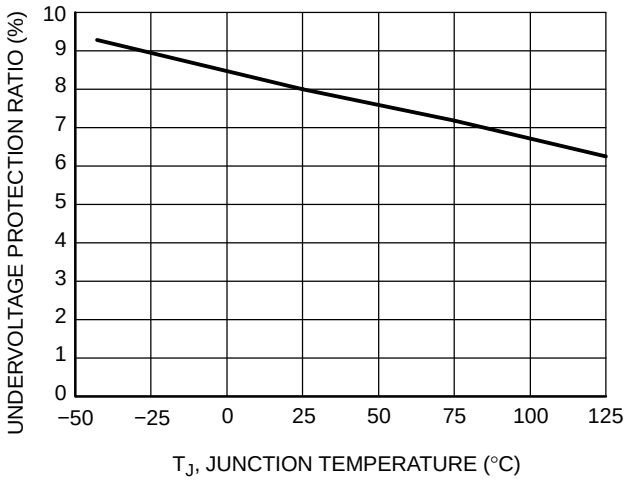


Figure 14. Undervoltage Protection Ratio vs. Temperature

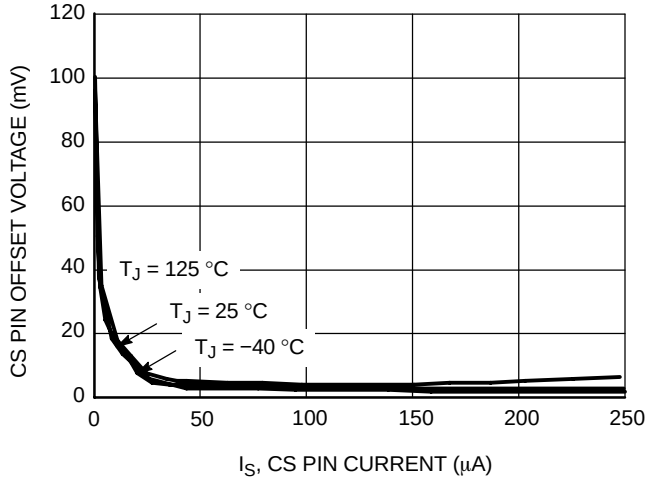


Figure 15. CS Pin Offset Voltage vs. Current

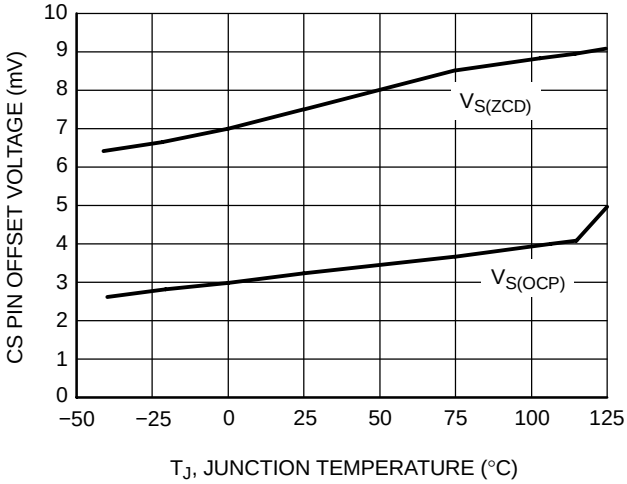


Figure 16. CS Pin Offset Voltage at OCP, ZCD vs. Temperature

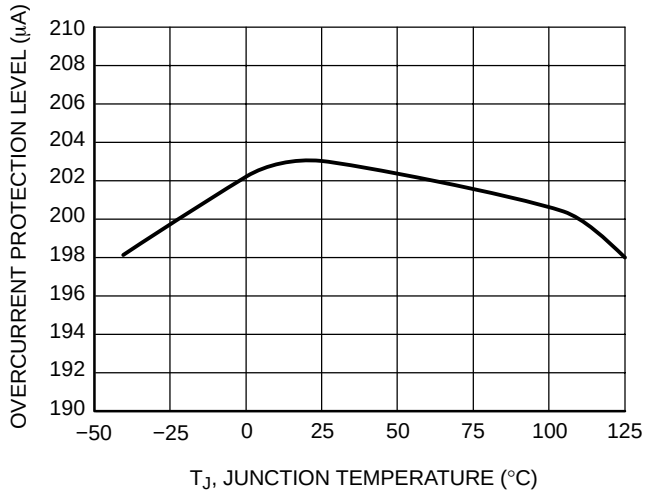


Figure 17. Overcurrent Protection Level vs. Temperature

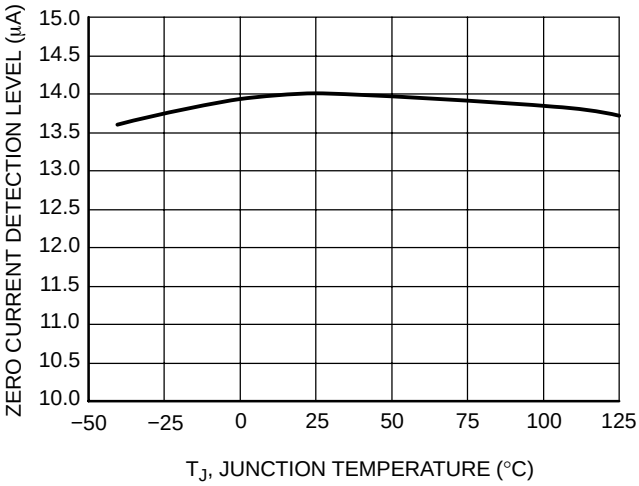


Figure 18. Zero Current Detection Level vs. Temperature

TYPICAL CHARACTERISTICS

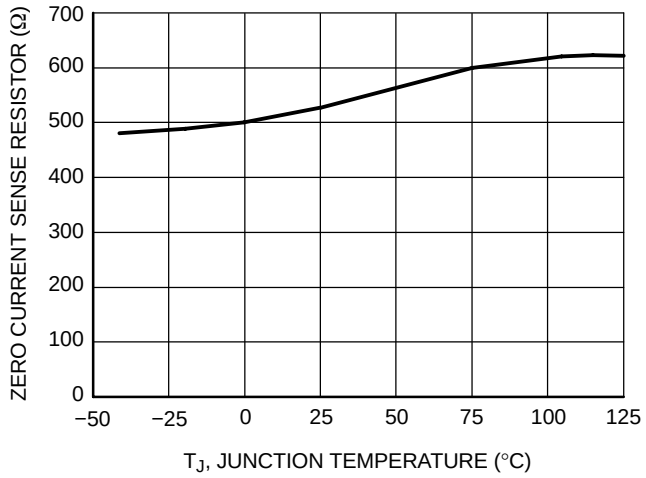


Figure 19. Zero Current Sense Resistor vs. Temperature

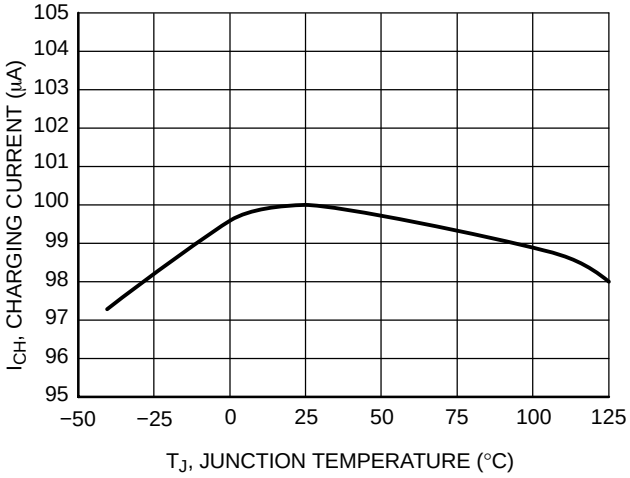


Figure 20. Charging Current vs. Temperature

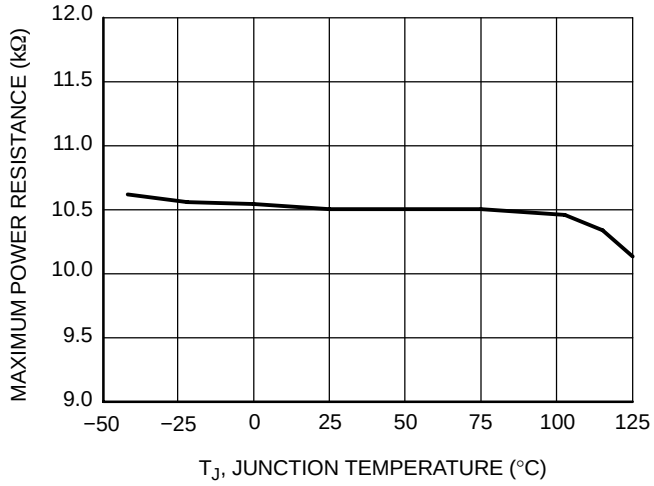


Figure 21. Maximum Power Resistance vs. Temperature

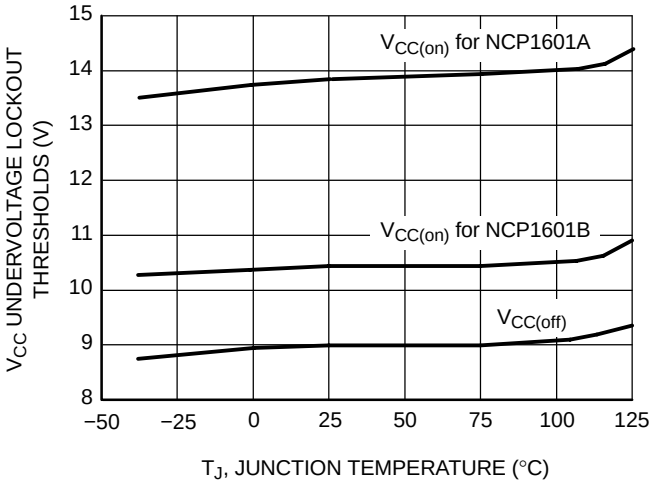


Figure 22. Supply Voltage Undervoltage Lockout Thresholds vs. Temperature

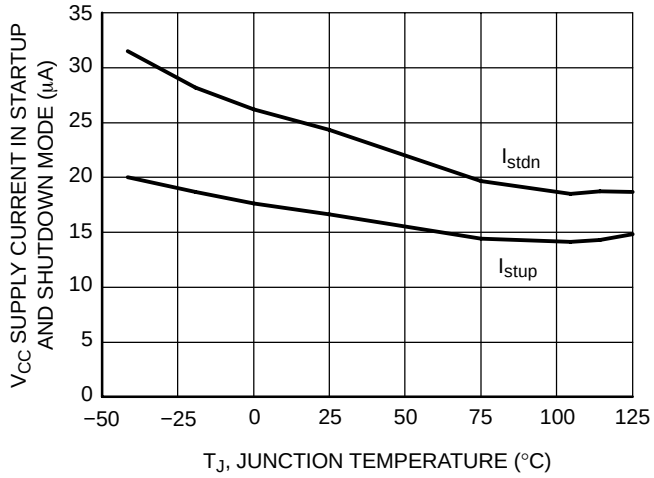


Figure 23. Supply Current in Startup and Shutdown Mode vs. Temperature

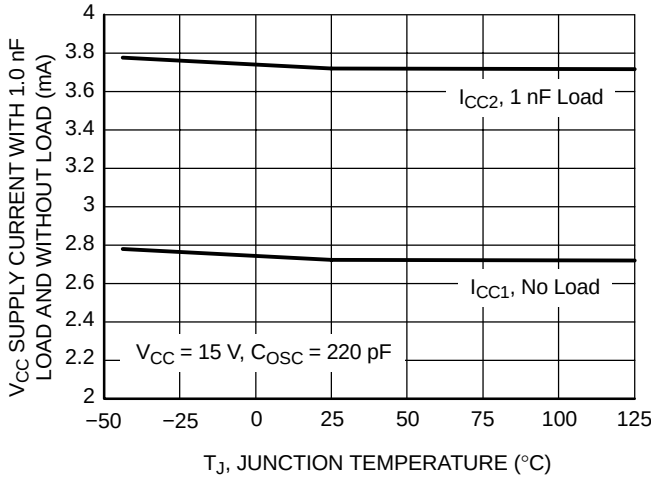


Figure 24. Supply Current vs. Temperature

FUNCTIONAL DESCRIPTION

Introduction

The NCP1601 is a Power Factor Correction (PFC) boost controller designed to operate in Discontinuous Conduction Mode (DCM) and Critical Conduction Mode (CRM). The fixed−frequency nature of DCM limits the maximum switching frequency. It limits the possible conducted and radiated EMI noise that may pollute surrounding systems. NCP1601 offers the simplest solution to PFC including fewer external circuit components and simple voltage−mode feedback. The diode turn−off switching loss is negligible and hence there is no need to use a low reverse−recovery time t_{rr} diode. On the other hand, the CRM feature is added to limit the maximum current stress to twice of the average current. The NCP1601 incorporates high safety protection features and combines the advantages of DCM and CRM so that the NCP1601 is suitable for robust and compact PFC stages.

The NCP1601 provides the following protection features:

1. **Overvoltage Protection (OVP)** is activated and the output drive goes low when the output voltage exceeds 107% of the nominal regulation level which is a user−defined value. The circuit automatically resumes operation when the output voltage becomes lower than 107%.
2. **Undervoltage Protection (UVP)** is activated and the device is shut down when the output voltage goes below 8% of the nominal regulation level. The circuit automatically resumes operation when the output voltage goes above 8% of the nominal regulation level. This feature also provides output open−loop protection and external shutdown feature.
3. **Overcurrent Protection (OCP)** is activated and the output device goes low when the inductor current exceeds a user−defined value. The operation automatically resumes when the inductor current becomes lower than this user−defined value at the next clock cycle.
4. **Thermal Shutdown (TSD)** is activated and the output drive is disabled when the junction temperature exceeds 140°C. The operation resumes when the junction temperature falls down by typical 45°C.

The NCP1601 is available in two versions. The NCP1601A has a typical 4.75 V undervoltage lockout (UVLO) hysteresis, while NCP1601B has a typical 1.5 V UVLO hysteresis. It allows the use of different V_{CC} biasing schemes.

Operating Modes of NCP1601

The NCP1601 is a PFC driver primarily designed to operate in fixed−frequency DCM. In the most stressful conditions, CRM can be an alternative option which is without power factor degradation. On the other hand, the NCP1601 can be viewed as a CRM controller with a frequency clamp (maximum switching frequency limit) alternative option which is also without power factor degradation. In summary, the NCP1601 can cover both CRM and DCM without power factor degradation. Based on the selections of the boost inductor and the oscillator frequency, the circuit is capable of the following three applications.

1. “Mostly in CRM” with a frequency clamp set by the oscillator or synchronization frequency.
2. “Mostly in fixed−frequency mode DCM” and only run in CRM at high load and low line.
3. “Fixed−frequency DCM” only.

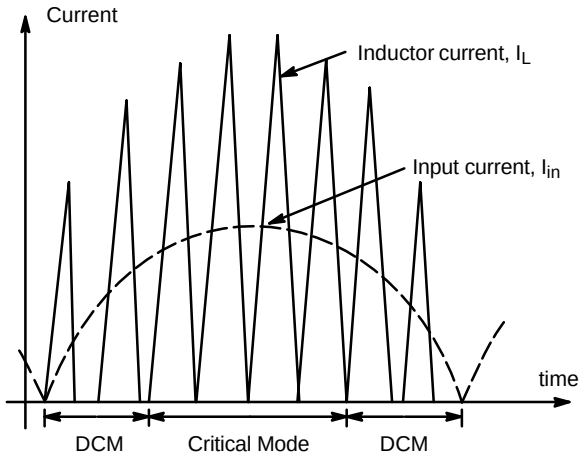


Figure 25. Operating Modes

DCM needs higher peak inductor current comparing to CRM in the same averaged input current. Hence, CRM is generally preferred at around the sinusoidal peak for lower the maximum current stress but DCM is also preferred at the non−peak region to avoid excessive switching frequencies. Because of the variable−frequency feature of the CRM and constant−frequency feature of DCM, switching frequency is the maximum in the DCM region and hence the minimum switching frequency will be found at the moment of the sinusoidal peak.

DCM PFC Circuit

A DCM/CRM PFC boost converter is shown in Figure 26. Input voltage is a rectified 50 or 60 Hz sinusoidal signal. The MOSFET is switching at a high frequency (typically around 100 kHz) so that the inductor current I_L basically consists of high−frequency and low−frequency components.

Filter capacitor C_{filter} is an essential and very small value capacitor in order to eliminate the high−frequency content of the DCM inductor current I_L. This filter capacitor cannot

be too bulky because it can pollute the power factor by distorting the rectified sinusoidal input voltage.

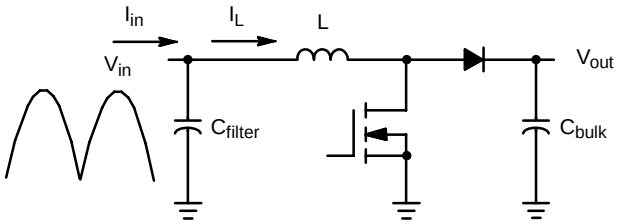


Figure 26. DCM/CRM PFC Boost Converter

PFC Methodology

NCP1601 uses a proprietary PFC methodology particularly designed for both DCM and CRM operation. The PFC methodology is described in this section.

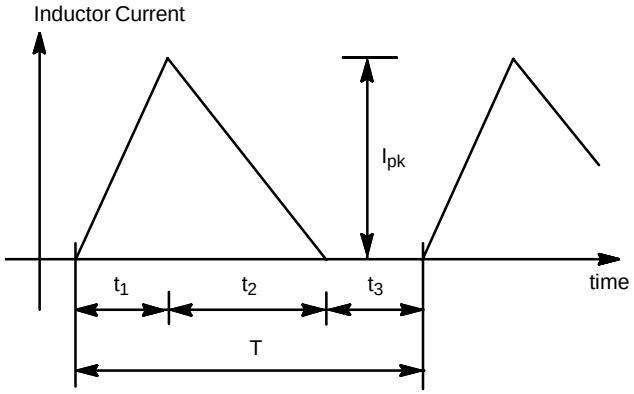


Figure 27. Inductor Current in DCM

As shown in Figure 27, the inductor current I_L of each switching cycle starts from zero in DCM. CRM is a special case of DCM when $t_3 = 0$. When the PFC boost converter MOSFET is on, the inductor current I_L increases from zero to I_{pk} for a time duration t_1 with inductance L and input voltage V_{in}. (eq.1) is formulated.

$$V_{in} = L\frac{I_{pk}}{t_1} \qquad \text{(eq.1)}$$

The input filter capacitor C_{filter} and the front−ended EMI filter absorb the high−frequency component of inductor current. It makes the input current I_{in} a low−frequency signal.

$$I_{in} = \frac{I_{pk}\,(t_1 + t_2)}{2\,T} \qquad \text{for DCM} \qquad \text{(eq.2a)}$$

$$I_{in} = \frac{I_{pk}}{2} \qquad \text{for CRM} \qquad \text{(eq.2b)}$$

From (eq.1) and (eq.2), the input impedance Z_{in} is formulated.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2TL}{t_1(t_1 + t_2)} \qquad \text{for DCM} \qquad \text{(eq.3a)}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2L}{t_1} \qquad \text{for CRM} \qquad \text{(eq.3b)}$$

Power factor is corrected when the input impedance Z_{in} in (eq.3) are constant or slowly varying.

The MOSFET on time t_1 or PFC modulation duty is generated by a feedback signal V_{ton} and a ramp. The PFC modulation circuit and timing diagram are shown in Figure 28. A relationship in (eq.4) is obtained.

$$t_1 = \frac{C_{ramp}\,V_{ton}}{I_{ch}} \qquad \text{(eq.4)}$$

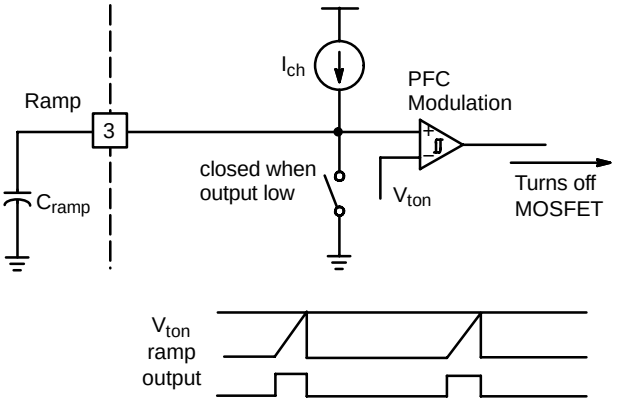


Figure 28. PFC Modulation Circuit and Timing Diagram

The charging current I_{ch} is constant 100 μA current and the ramp capacitor C_{ramp} is constant for a particular design. Hence, according to (eq.4) the MOSFET on time t_1 is proportional to V_{ton}.

In order to protect the PFC modulation comparator, the maximum voltage of V_{ton} is limited to internal clamp $V_{ton(max)}$ (3.9 V typical) and the ramp pin (Pin 3) is with a 9 V ESD Zener diode. The 3.9 V maximum limit of this V_{ton} indirectly limits the maximum on time.

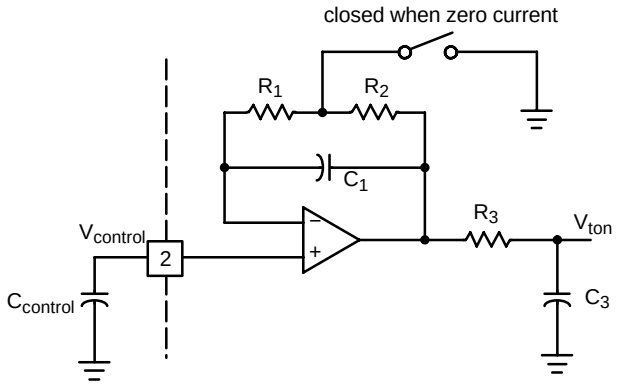


Figure 29. $V_{control}$ Processing Circuit

The $V_{control}$ processing circuit generates V_{ton} from control voltage $V_{control}$ and time information of zero inductor current. The circuit in Figure 29 makes (eq.5) where the value of resistor R_1 is much higher than the value of resistor R_2 ($R_1 >> R_2$).

$$V_{ton} = \frac{T\,V_{control}}{t_1 + t_2} \qquad \text{for DCM} \qquad \text{(eq.5a)}$$

$$V_{ton} = V_{control} \quad \text{for CRM} \qquad \text{(eq.5b)}$$

It is noted that V_{ton} is always greater than or equal to $V_{control}$ (i.e., $V_{ton} \geq V_{control}$).

In summary, the input impedance Z_{in} in (eq.6) is obtained from (eq.1)−(eq.5)

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2\ L\ I_{ch}}{C_{ramp}\ V_{control}} \qquad \text{(eq.6)}$$

Control voltage $V_{control}$ comes from the PFC output voltage V_{out} which is a slowly varying signal. The bandwidth of $V_{control}$ can be additionally limited by inserting an external capacitor $C_{control}$ to the $V_{control}$ pin (Pin 2) in Figure 28. The internal 300 kΩ resistor and the capacitor $C_{control}$ create a low−pass filter which has a bandwidth $f_{control}$ in (eq.7). It is generally recommended to limit the bandwidth below 20 Hz to achieve power factor correction. Typical value of $C_{control}$ is 0.1 μF.

$$C_{control} > \frac{1}{2\pi 300k\Omega\ f_{control}} \qquad \text{(eq.7)}$$

If the bandwidth of $V_{control}$ is much less than the 50 or 60 Hz line frequency, the input impedance Z_{in} is slowly varying or roughly constant. Then, the power factor correction is achieved in DCM and CRM.

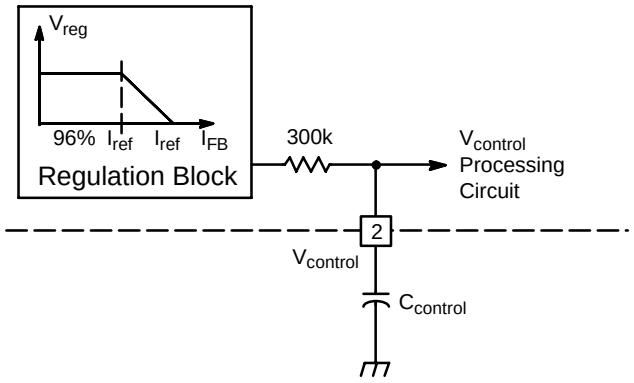


Figure 30. $V_{control}$ Low−Pass Filtering

Maximum Power

Input and output power (P_{in} and P_{out}) are derived in (eq.8) when the circuit efficiency η is obtained or assumed. The variable V_{ac} stands for the RMS input voltage.

$$P_{in} = \frac{V_{ac}^2}{Z_{in}} = \frac{V_{ac}^2 C_{ramp} V_{control}}{2 L I_{ch}} \qquad \text{(eq.8a)}$$

$$P_{out} = \eta\ P_{in} = \frac{\eta V_{ac}^2 C_{ramp} V_{control}}{2 L I_{ch}} \qquad \text{(eq.8b)}$$

From (eq.8), control voltage $V_{control}$ controls the amount of output power, input power, or input impedance. The maximum value of the control voltage $V_{control}$ is 1.05 V (i.e., $V_{control(max)}$ = 1.05 V). A parameter called maximum power resistor R_{power} (10.5 kΩ typical) is defined in (eq.9) and restricted to have a maximum ±10% variation (i.e., 9.5 kΩ ≤ R_{power} ≤ 11.5 kΩ) for defining the maximum power in an application.

$$R_{power} = \frac{V_{control(max)}}{I_{ch}} = \frac{1.05\ V}{100\ \mu A} = 10.5\ k\Omega \qquad \text{(eq.9)}$$

It means that the maximum input and output power ($P_{in(max)}$ and $P_{out(max)}$) are limited to ±10% variation.

$$P_{in(max)} = \frac{V_{ac}^2 C_{ramp} R_{power}}{2 L} \qquad \text{(eq.10a)}$$

$$P_{out(max)} = \frac{\eta V_{ac}^2 C_{ramp} R_{power}}{2 L} \qquad \text{(eq.10b)}$$

The maximum input current $I_{ac(max)}$ to deliver the maximum input power $P_{in(max)}$ is also derived in (eq.11). The suffix ac stands for RMS value.

$$I_{ac(max)} = \frac{P_{in(max)}}{V_{ac}} = \frac{V_{ac} C_{ramp} R_{power}}{2 L} \qquad \text{(eq.11)}$$

Output Feedback

The output voltage V_{out} of the PFC circuit is sensed as a feedback current I_{FB} flowing into the FB pin (Pin 1) of the device. The FB pin voltage V_{FB1} is typically less than 5 V referring to Figure 11. It is much lower than V_{out} which is typically 400 V. Therefore, V_{FB1} is generally neglected.

$$I_{FB} = \frac{V_{out} - V_{FB1}}{R_{FB}} \approx \frac{V_{out}}{R_{FB}} \qquad \text{(eq.12)}$$

where R_{FB} is the feedback resistor connected between the FB pin (Pin 1) and the output voltage referring to Figure 2.

Then, the feedback current I_{FB} represents the output voltage V_{out} and will be used in the output voltage regulation, Undervoltage Protection (UVP), and Overvoltage Protection (OVP).

Output Voltage Regulation

Feedback current I_{FB}, which presents output voltage V_{out}, is regulated with a reference current (I_{ref} = 203 μA typical) as shown in Figure 31.

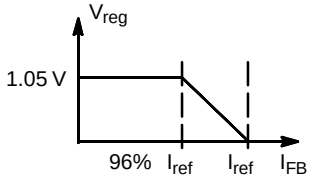


Figure 31. Regulation Block

When I_{FB} is lower than 96% of I_{ref}, the V_{reg} which is the output of the regulation block is as high as $V_{control(max)}$ (1.05 V typical) that gives the maximum value on V_{ton}. As a result, it gives the maximum MOSFET on time and V_{out} increases. When I_{FB} is higher than I_{ref}, the V_{reg} becomes 0 V that gives no MOSFET on time and V_{out} decreases. As a result, the output voltage V_{out} is regulated around the range between 96% and 100% of the nominal value of R_{FB} × I_{ref}.

Based on (eq.8) for a particular power level, the $V_{control}$ is inversely proportional to V_{ac}^2. Hence, in high V_{ac} condition $V_{control}$ is lower. It means that I_{FB} or output

voltage is higher based on the regulation block characteristic in Figure 31. On the other hand, the $V_{control}$ in the low V_{ac} condition is much higher than the high V_{ac} condition. In order to not over−design the circuit in the application, the $V_{control}$ in the low V_{ac} condition is usually very closed to $V_{control(max)}$. It makes the output voltage be almost 96% of the nominal value of $R_{FB} \times I_{ref}$ in low V_{ac} condition while the output voltage is almost 100% of the nominal value $R_{FB} \times I_{ref}$ in high V_{ac} condition.

The feedback resistor R_{FB} consists of two or three high precision resistors in order to set the nominal V_{out} precisely and safety purpose.

The regulation block output V_{reg} is connected to control voltage $V_{control}$ through an internal resistor $R_{control}$ (300 kΩ typical) for the low−pass filter in Figure 30. The $V_{control}$ and the time information of zero current are collected in the $V_{control}$ processing circuit to generate V_{ton} which is then compared to a ramp signal to generate the MOSFET on time t_1 for power factor correction.

Overvoltage Protection (OVP)

When the feedback current I_{FB} is higher than 107% of the reference current I_{ref} (i.e., the output voltage V_{out} is higher than 107% of its nominal value), the Drive Output pin (Pin 7) of the device goes low for protection and the switch of the $V_{control}$ processing circuit is kept off. The circuit automatically resumes operation when the output voltage is lower than 107%.

The maximum OVP threshold is limited to 225 μA which corresponds to 225 μA × 1.95 MΩ + 5 V = 443.75 V when R_{FB} = 1.95 MΩ (1.8 MΩ + 150 kΩ) and V_{FB1} = 5 V (for the worst case referring to Figure 11). Hence, it is generally recommended to use 450 V rating output capacitor to allow some design margin.

Undervoltage Protection (UVP)

When the feedback current I_{FB} is lower than 8% of the reference current I_{ref} (i.e., the output voltage V_{out} is lower than 8% of its nominal value), the device is shut down and consumes lower than 50 μA. In normal situation of boost converter configuration, the output voltage V_{out} is always higher than the input voltage V_{in} and the feedback current I_{FB} is always higher than 8% of the reference current I_{ref}. It enables the NCP1601 to operate. Hence, UVP happens when the output voltage is abnormally undervoltage, the FB pin (Pin 1) is opened, or the FB pin (Pin 1) is manually pulled low.

Current Sense

The device senses the inductor current I_L by the current sense scheme in Figure 32. This scheme has the advantages of: (1) the inrush current limitation by the resistor R_{CS}, and (2) the overcurrent protection and zero current detection implemented in the same pin.

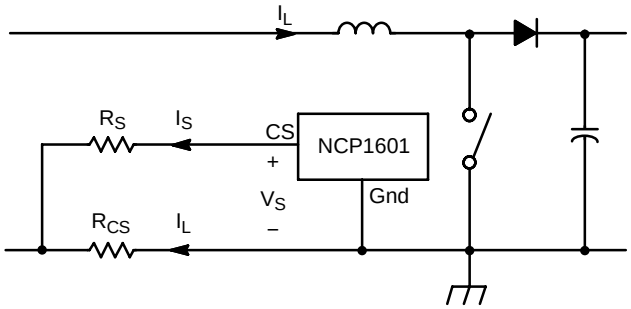


Figure 32. Current Sensing

Inductor current I_L passes through R_{CS} and creates a negative voltage. This voltage is measured by a current I_S flowing out of the CS pin (Pin 4). The CS pin has an offset voltage V_S. This offset voltage is studied in the setting of zero inductor current $I_{L(ZCD)}$ and the maximum inductor current $I_{L(OCP)}$ (i.e., overcurrent protection threshold). A typical variation of offset voltage V_S versus sense current I_S is shown in Figure 15. Higher the value of the offset voltage at low current region creates lower the zero current threshold for better accuracy. Based on Figure 32, (eq.13) is derived.

$$V_S - R_S I_S = -R_{CS} I_L \qquad \text{(eq.13)}$$

Zero Current Detection (ZCD)

The device recognizes zero inductor current when the CS pin (Pin 4) sense current I_S is lower than $I_{S(ZCD)}$ (14 μA typical). The offset voltage of the CS pin in this condition is $V_{S(ZCD)}$ (7.5 mV typical). It is illustrated in Figure 33. The inductor current $I_{L(ZCD)}$ at the ZCD condition is derived in (eq.14).

$$I_{L(ZCD)} = \frac{R_S I_{S(ZCD)} - V_{S(ZCD)}}{R_{CS}} \qquad \text{(eq.14)}$$

It is obvious that the $I_{L(ZCD)}$ is not always zero. In order to make it reasonably close to zero, the settings of R_S and R_{CS} are crucial.

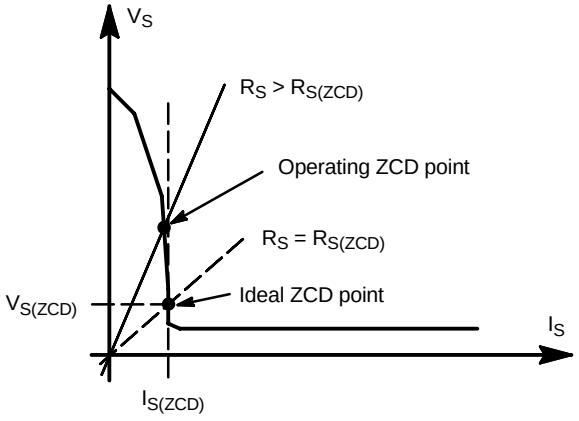


Figure 33. CS Pin Characteristic when I_L = 0

Based on the CS pin (Pin 4) characteristics in Figure 15, Figure 33 is studied. When the inductor current is exactly zero (i.e., $I_{L(ZCD)} = 0$), the ideal ZCD point in the Figure is reached where R_S is $R_{S(ZCD)}$ (536 Ω typical). Considering the tolerance, the actual sense resistor R_S is needed to be higher than the ideal value of $R_{S(ZCD)}$ to ensure that zero current signal is generated when sense current is smaller than the ZCD threshold (i.e., $I_S < I_{S(ZCD)}$). That is,

$$R_S > R_{S(ZCD)} = \frac{V_{S(ZCD)}}{I_{S(ZCD)}} \qquad \text{(eq.15)}$$

The higher value of R_S makes the longer distance between the operating and ideal ZCD points in Figure 33. Hence, R_S has to be as low as possible. The best recommended value of R_S is therefore the maximum of $R_{S(ZCD)}$ which is 1 kΩ.

Now that the R_S is set at a particular value which is greater than $R_{S(ZCD)}$. From (eq.13), the operating lines in (eq.16) with different inductor currents I_L of (eq.13) are studied.

$$V_S = R_S - R_{CS} I_L \qquad \text{(eq.16)}$$

These operating lines are added in Figure 33 to formulate Figure 34. When the inductor current I_L is lower than $I_{L(ZCD)}$, the sense current I_S is lower than $I_{S(ZCD)}$ and hence the zero current signal is generated.

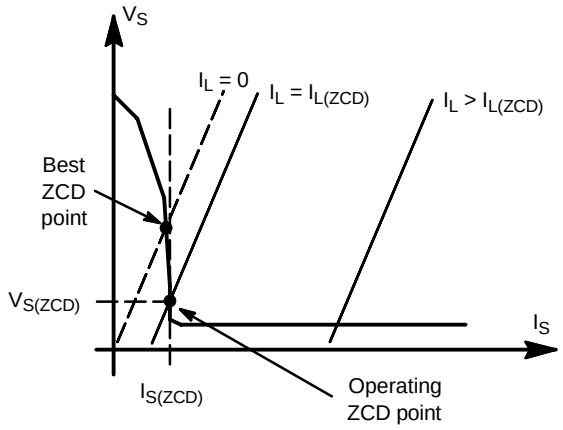


Figure 34. CS Pin Characteristic with Different Inductor Current

It is noted in Figure 34 and (eq.16) that when the (R_{CS} I_L) term is smaller the error or distance between the lines to the line $I_L = 0$ is smaller. Therefore, the value of the current sense resistor R_{CS} is also recommended to be as small as possible to minimize the error in the zero current detection.

Overcurrent Protection (OCP)

Overcurrent protection is reached when I_S is higher than $I_{S(OCP)}$ (200 μA typical). The offset voltage of the CS pin is $V_{S(OCP)}$ (3.2 mV typical) in this condition. That is

$$I_{L(OCP)} = \frac{R_S I_{S(OCP)} - V_{S(OCP)}}{R_{CS}} \qquad \text{(eq.17)}$$

When overcurrent protection threshold is reached, the Drive Output of the device goes low.

Oscillator / Synchronization Block

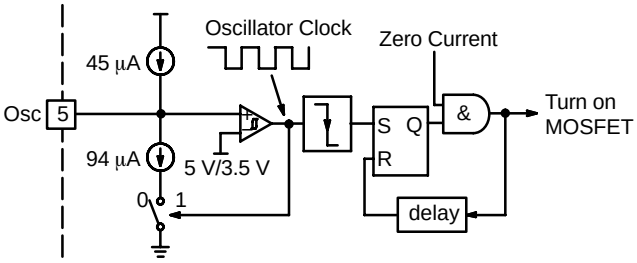


Figure 35. Oscillator / Synchronization Block

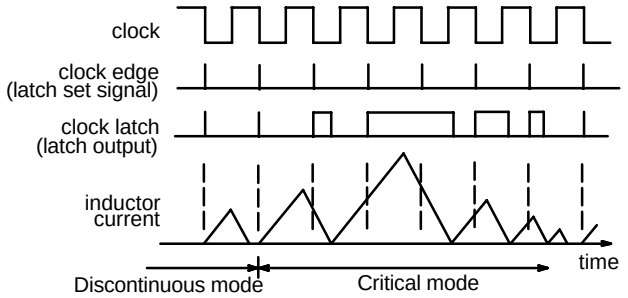


Figure 36. Oscillator Block Timing Diagram

The NCP1601 is a DCM / CRM PFC controller. In order to keep the operation in DCM or CRM only, the Drive Output cannot turn on as long as there is some inductor current flowing through the circuit. Hence, the zero current signal is provided to the oscillator / synchronization block in Figure 35. An input comparator monitors the Osc pin (Pin 5) voltage and generates a clock signal. The negative edge of the clock signal is stored in a RS latch. When zero current is detected, the RS latch will be reset and a set signal is sent to the output drive latch which turns on the MOSFET in the PFC boost circuit. Figure 36 illustrates a typical timing diagram of the oscillator block.

Oscillator Mode

The Osc pin (Pin 5) is connected to an external capacitor C_{osc}. When the voltage of this pin is above $V_{sync(H)}$ (5 V typical), the pin sinks a current I_{odch} (94 – 45 = 49 μA typical) and the external capacitor C_{osc} discharges. When the voltage reaches $V_{sync(L)}$ (3.5 V typical), the pin sources a current I_{och} (45 μA typical) and the external capacitor C_{osc} is charged. It is noted that there is a typical 300 ns propagation delay and the 3.5 V and 5 V threshold conditions are measured on 220 pF C_{osc} capacitor. Hence, the actual oscillator hysteresis is a slightly smaller.

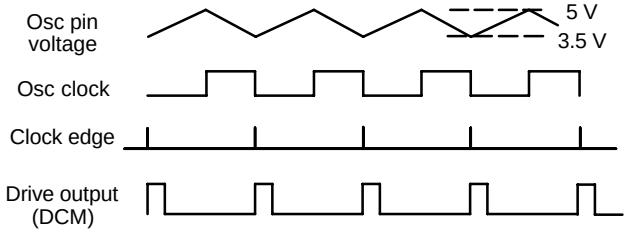


Figure 37. Oscillator Mode Timing Diagram in DCM

There is an internal capacitance $C_{osc(int)}$ (36 pF typical) in the oscillator pin and the oscillator frequency is to $f_{osc(max)}$ (405 kHz typical) when the Osc pin is opened. Hence, the oscillator switching frequency can be formulated in (eq.18) and represented in Figure 38.

$$C_{osc} = \frac{36\ pF \cdot 405\ kHz}{f_{osc}} - 36\ pF \qquad \text{(eq.18)}$$

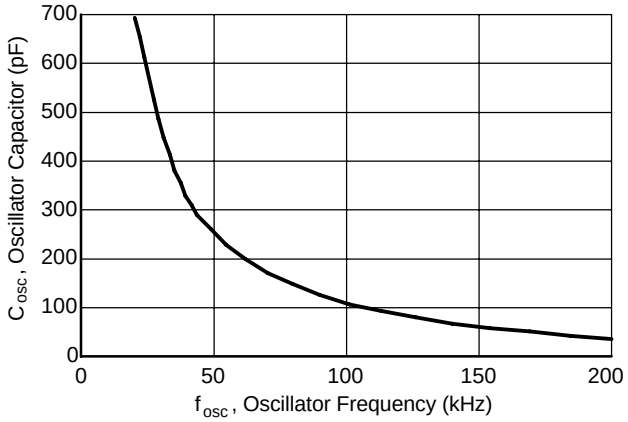


Figure 38. Osc Pin Frequency Setting

Synchronization Mode

The Osc pin (Pin 5) receives an external digital signal with level high defined to be higher than $V_{sync(H)}$ (5 V typical) and level low defined to be lower than $V_{sync(L)}$ (3.5 V typical). An internal 9 V ESD Zener diode is connected to the Osc pin and hence the maximum synchronization voltage is 9 V. The circuit recognizes a synchronization frequency by the time difference between two falling edge instants when the synchronization signal across the 3.5 V threshold points. The actual synchronization threshold point is a slightly higher than the 3.5 V threshold point. The minimum synchronization pulse width is 500 ns.

There is a typical 350 ns propagation delay from synchronization threshold point to the moment of output goes high and there is also a typical 300 ns propagation delay from the synchronization threshold point to the moment of crossing 3.5 V. Hence, the output goes high apparently when the sync signal turns to 3.5 V. A timing diagram of synchronization mode is summarized in Figure 39.

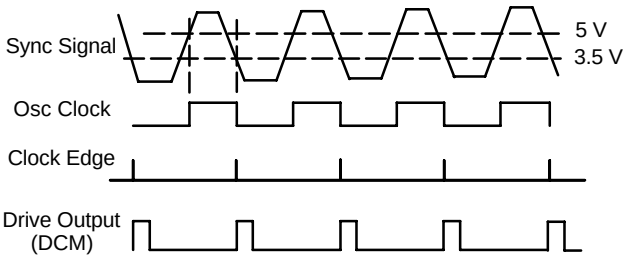


Figure 39. Synchronization Mode Timing Diagram in DCM

V_{CC} Undervoltage Lockout (UVLO)

There are two UVLO options. The device typically starts to operate when the supply voltage V_{CC} exceeds 13.75 V for NCP1601A and 10.5 V for NCP1601B. It turns off when the supply voltage V_{CC} goes below 9 V. An 18 V internal ESD Zener diode is connected to the V_{CC} pin (Pin 8). Hence, the operating range is 9 V to 18 V.

The 4.75 V UVLO hysteresis option of the NCP1601A and 14 μA low startup current make the self−supply design easier. The 1.5 V UVLO hysteresis option of NCP1601B makes it more flexible to match with the second−stage PWM controller biasing V_{CC} supply voltage.

Thermal Shutdown

An internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 140°C. The output stage is then enabled once the temperature drops below typically 95°C (i.e., 45°C hysteresis). The thermal shutdown is provided to prevent possible device failures that could result from an accidental overheating.

Output Drive

The output stage of the device is designed for direct drive of power MOSFET. It is capable of up to −500 mA and +750 mA peak drive current and has a typical rise and fall time of 53 and 32 ns with a 1.0 nF load.

Table 1. Power Factor Controller Test Data

V_{in} (Vac)	P_{in} (W)	V_{out} (V)	I_{out} (mA)	PF	THD (%)	Efficiency (%)
90	143.4	327	400	0.998	4	91.2
110	161.1	373	400	0.997	6	92.6
130	160.5	378	400	0.996	6	94.2
150	160.9	382	400	0.993	7	95.0
180	161.6	386	400	0.990	6	95.5
190	161.7	387	400	0.986	8	95.7
210	162.0	389	400	0.980	8	96.0
230	162.2	391	400	0.973	9	96.4
250	162.8	393	400	0.959	16	96.6

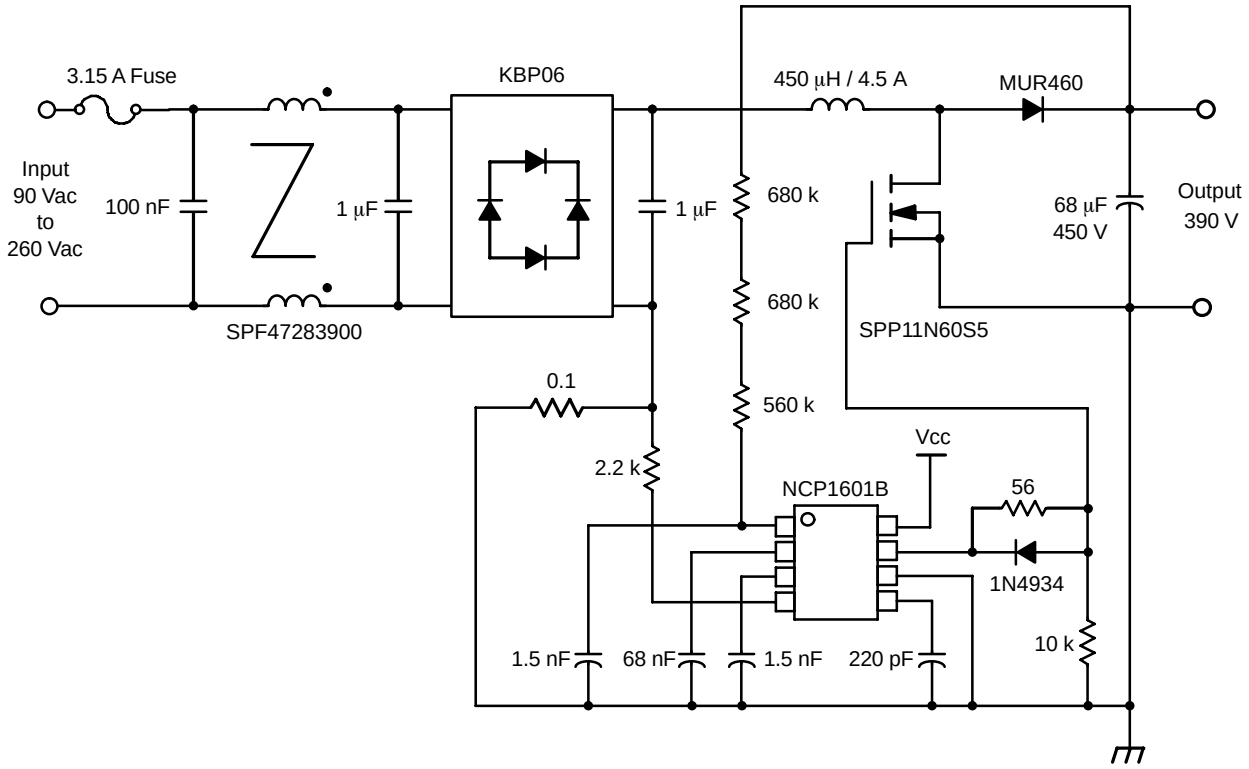


Figure 40. 130 W Power Factor Correction Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NCP1601AP	PDIP−8	50 Units / Rail
NCP1601APG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1601ADR2	SOIC−8	2500 Units / Tape & Reel
NCP1601ADR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCP1601BP	PDIP−8	50 Units / Rail
NCP1601BPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1601BDR2	SOIC−8	2500 Units / Tape & Reel
NCP1601BDR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

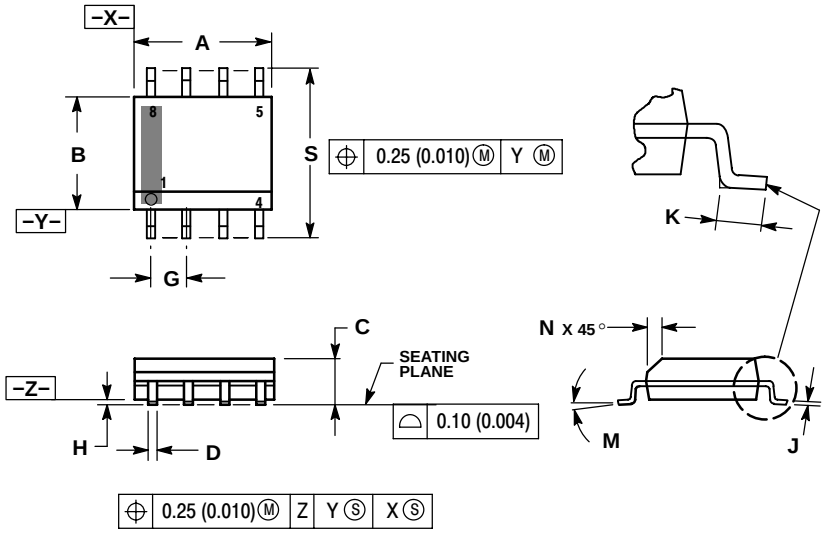
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Appendix I – Summary of Equations in NCP1601 Boost PFC

Description	Critical Mode (CRM)	Discontinuous Mode (DCM)
Boost converter	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$	$\frac{V_{out}}{V_{in}} = \frac{t_1 + t_2}{t_2}$ $\rightarrow \frac{V_{out} - V_{in}}{V_{out}} = \frac{t_1}{t_1 + t_2}$
Input current averaged by filter capacitor	$I_{in} = \frac{I_{pk}}{2}$	$I_{in} = \frac{t_1 + t_2}{T}\frac{I_{pk}}{2}$
Voltage for on time V_{ton}	$V_{ton} = V_{control}$	$V_{ton} = \frac{T}{t_1 + t_2}V_{control}$
MOSFET on−time t_1	$t_1 = \frac{LI_{pk}}{V_{in}}$, or $t_1 = \frac{C_{ramp}V_{control}}{I_{ch}}$ $\rightarrow$ t_1 is constant for unity PFC $\rightarrow$ $V_{control}$ is constant for unity PFC	$t_1 = \frac{LI_{pk}}{V_{in}}$, or $t_1 = \sqrt{\frac{V_{out} - V_{in}}{V_{out}}T\frac{C_{ramp}V_{control}}{I_{ch}}}$ $\rightarrow$ t_1 ($t_1 + t_2$) is constant for unity PFC $\rightarrow$ $V_{control}$ is constant for unity PFC
Switching period	$t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}}\frac{C_{ramp}V_{control}}{I_{ch}}$, or $t_1 + t_2 = \frac{V_{out}}{V_{out} - V_{in}}\frac{LI_{pk}}{V_{in}}$	$t_1 + t_2 = \frac{T}{t_1}\frac{C_{ramp}V_{control}}{I_{ch}}$, or $t_1 + t_2 = \sqrt{\frac{V_{out}}{V_{out} - V_{in}}T\frac{C_{ramp}V_{control}}{I_{ch}}}$
Minimum Inductor for CRM	$L > L_{(CRM)} = \frac{V_{out} - V_{in}}{V_{out}}\frac{V_{in}}{I_{pk}}\frac{1}{f}$	Same as CRM
Input impedance	$Z_{in} = \frac{2LI_{ch}}{C_{ramp}V_{control}}$	Same as CRM
Input power	$P_{in} = \frac{V_{ac}^2 C_{ramp}V_{control}}{2LI_{ch}}$	Same as CRM
Output power	$P_{out} = \eta P_{in} = \frac{\eta V_{ac}^2 C_{ramp}V_{control}}{2LI_{ch}}$	Same as CRM
Maximum input power when $V_{control}$ = 1 V	$P_{in\_max} = \frac{V_{ac}^2 C_{ramp}}{2LI_{ch}}$	Same as CRM
Minimum ramp capacitor when $V_{control}$ = 1 V	$C_{ramp} > \frac{P_{in}}{V_{ac}^2} \cdot 2LI_{ch}$	Same as CRM
Control voltage $V_{control}$	$V_{ctrl} = \frac{2LI_{ch}P_{in}}{C_{ramp}V_{ac}^2}$	Same as CRM

PACKAGE DIMENSIONS

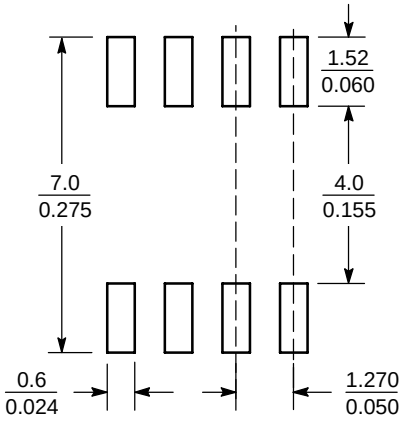
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

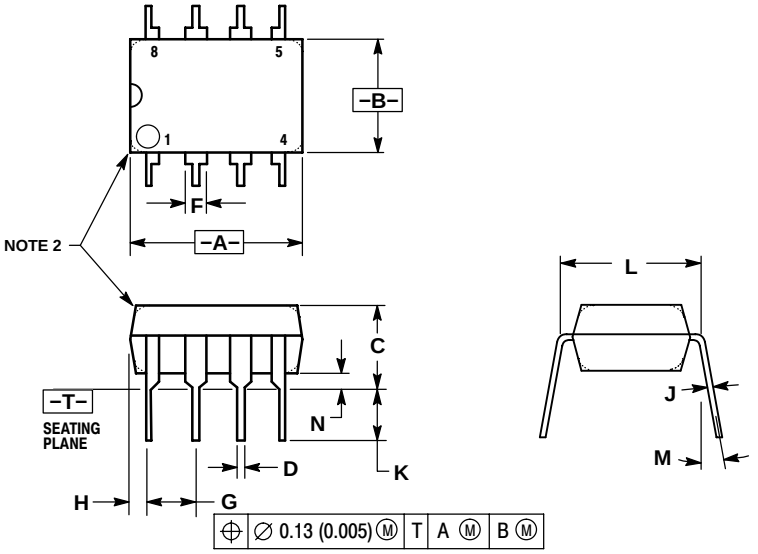


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−8
N SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

The products described herein (NCP1601A, NCP1601B), may be covered by the following U.S. patents: 6,271,735, 6,362,067, 6,970,365. There may be other patents pending.

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