

■Absolute Maximum Ratings

ltem	Symbol	Min	Max	Unit	Conditions · Note
Input voltage for DC/DC converter	V_{IN}	-0.3	28	Vdc	Between Vin(+) to Vin(-)
Minimum operating input voltage for DC/DC converter	V _{INMIN}	13	-	Vdc	
Input-side signal voltage	$V_{\rm SG}$	-0.3	5.2	V	INA, INB, XRST, RDY, FLT
Input-side signal maximum current	I_{SG}	-	5	mA	RDY, FLT
DESAT pin input voltage	V_{DESAT}	-0.3	V _{OUTH} +0.3	V	
CLAMP pin input voltage	V_{CLAMP}	$V_{OUTL}-0.3$	V _{OUTH} +0.3	V	
OUT pin output current(peak)	I _{OUTPEAK}	-	18	А	Guaranteed by design
Output power for DC/DC converter	P _{OUT}	-	3	W	By one circuit
Switching frequency	F _{sw}	-	200	kHz	
Operating temperature range	T _{OP}	-30	85	°C	See the derating curve
Operating humidity	RH _{OP}	20	95	%RH	No condensation
Storage temperature range	T _{STG}	-30	100	°C	
Storage humidity	RH_{STG}	5	95	%RH	No condensation

Recommended Operating Conditons

ltem	Symbol	Min	Max	Unit	Conditions.Note	
Input voltage range for DC/DC converter	V _{IN}	13.5	26.4	Vdc	Rated Input Voltage:24V	
Driver circuit number	Ν	-	2	-		
Logic high level input voltage	$V_{\rm SGH}$	2	5	V	INA, INB ,XRST	
Logic low level input voltage	$V_{\rm SGL}$	0	0.8	V	INA, INB ,XRST	
Source current of control signal	I_{SG}	20	-	mA	INA, INB, XRST, V _{SG} =5V	
Maximum gate drive capability(200kHz)	Q _{MAX}	-	650	nC	T_{OP} =55°C Reference value	
Maximum gate drive capability(50kHz)	Q _{MAX}	_	2600	nC	T _{OP} =55°C Reference value	
Minimum input pulse width	t _{INMSK}	-	60	ns		



■Electrical Specification (Ta=25°C)

DC/DC converter block

ltem	Symbol	Min	Тур	Max	Unit	Conditions.Note	
Start-up voltage	$V_{\rm START}$	-	11.5	12.5	V		
Efficiency	Effi	69	74	-	%	Rated Input Voltage, I _{OUTAVE} (CH1,2):100mA	
Standby power	P _{STBY}	-	0.7	1	W	Rated Input Voltage, No load	
		14.5	15.5	16.5	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 10-140mA$	
Output voltage(Hgih)	V ₁₊ ,V ₂₊	14.5	15.5	17.0	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 0-10mA$	
Output voltage(Low)	V ₁₋ ,V ₂₋	-6	-5	-4	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 0-140mA$	
Output voltage(5VDC)	$V_{\rm 5VDC}$	4.8	5.0	5.2	V		
Output Voltage(High)(Load imbalance)	V_{1^+}, V_{2^+}	-	-	22	V	I _{OUTAVE} (CH1):100mA,I _{OUTAVE} (CH2):0mA or I _{OUTAVE} (CH1):0mA,I _{OUTAVE} (CH2):100mA	
Output Voltage(Low)(Load imbalance)	V ₁₋ ,V ₂₋	-11	-	-	V		

Gate drive block

ltem	Symbol	Min	Тур	Max	Unit	Conditions.Note		
Logic								
Logic high level input voltage	V_{SGH}	2	-	$V_{\rm 5VDC}$	V	INA, INB ,XRST		
Logic low level input voltage	V_{SGL}	0	-	0.8	V	INA, INB ,XRST		
Logic pull-down resistance	R_{SGD}	-	270	-	Ω	INA, INB ,XRST		
Logic pull-up resistance	R_{SGU}	-	5100	-	Ω	RDY, FLT		
Logic input mask time	t _{INMSK}	-	-	60	ns	INA, INB		
Minimum XRST pulse width	t _{XRSTMIN}	800	_	_	ns			



■Electrical Specification - Continued (Ta=25°C)

Gate drive block - continued

	ltem	Symbol	Min	Тур	Max	Unit	Conditions·Note	
Output	Output							
Output pin volt	age(Hgih)	$V_{\rm OUTH}$	-	V _{DCDCOH} -0.5	-	V	No load	
Output pin volt	ago(Low)	V _{OUTL}	-	V _{DCDCOL} +0.5	-	V	No load, Miller clamp pin no used	
Ουτρατ ριπ νοπ	age(LOW)	V OUTL	-	V _{DCDCOL} +0.1	-	V	No load, Miller clamp pin used	
OUT ON resista	JT ON resistance(Source) R ₀₁		-	-	50	mΩ	Guaranteed by design	
OUT ON resista	ance(Sink)	R _{ONL}	-	-	50	mΩ	Guaranteed by design	
CLAMP ON res	sistance	R _{ONPRO}	0.2	0.5	0.9	Ω	I _{CLAMP} =40mA	
Low level CLA	MP current	I _{CLAMPL}	3	4.5	-	А	Guaranteed by design	
CLAMP ON thr	eshold voltage	V _{CLPON}	V _{OUTL} +1.8	V_{OUTL} +2	V _{OUTL} +2.2	V	Guaranteed by design	
Delay time	Turn ON time	t _{PON}	55	80	105	ns		
	Turn OFF time	t _{POFF}	55	80	105	ns		

Protection

DC/DC converter block

ltem	Symbol	Min	Тур	Max	Unit	Conditions · Note	
Overload protection	-	6	-	-	W	Auto recovery	
Overheat protection	-	120	-	150	°C	Internal temperature	

Gate drive block

ltem	Symbol	Min	Тур	Max	Unit	Conditions · Note
5VDC UVLO OFF voltage	$V_{\rm UVL05VH}$	3.35	3.50	3.65	V	Guaranteed by design
5VDC UVLO ON voltage	V _{UVL05VL}	3.25	3.40	3.55	V	Guaranteed by design
5VDC UVLO UVLO mask time	T _{UVLO5VMSł}	1.0	2.5	5.0	US	Guaranteed by design
OUT(H) UVLO OFF voltage	V _{UVLOOHH}	11.3	12.3	13.3	V	Guaranteed by design
OUT(H) UVLO ON voltage	V _{UVLOOHL}	10.3	11.3	12.3	V	Guaranteed by design
OUT(H) UVLO mask time	T _{UVLOOHMS} ł	1.0	2.0	3.0	US	Guaranteed by design
DESAT source current	I _{desat}	450	500	550	uA	
DESAT threshold voltage	V_{DESAT}	8.5	9	9.5	V	
DESAT filter time	t _{desatfil}	0.16	0.25	0.34	US	Guaranteed by design
DESAT delay time(OUT)	t _{desatout}	0.31	0.38	0.45	US	Guaranteed by design
DESAT delay time(FLT)	t _{desatflt}	0.34	0.42	0.5	us	Guaranteed by design
DESAT low voltage	V_{DESATL}	-	0.1	0.22	V	I _{DESAT} =1mA
DESAT leading edge blanking	t _{DESTLEB}	0.28	0.4	0.52	us	Guaranteed by design
RDY output low voltage	V_{RDYL}	-	0.08	0.15	V	I _{RDY} =5mA
FLT output low voltage	V_{FLTL}	-	0.08	0.15	V	I _{FLT} =5mA

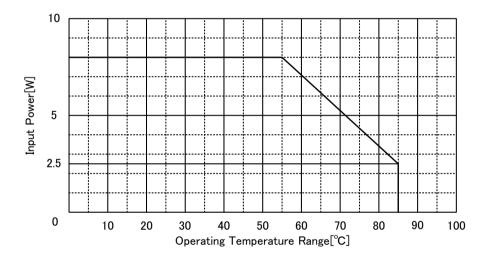


■Insulation

ltem	Specification	Conditions · Note
Between Input-Output	•	
Dielectric withstand voltage	AC2500V	1min, Cutoff 2mA
Test dielectric withstand voltage	AC2500V	1sec, Cutoff 2mA
Insulation resistance	$100M\Omega$ or more	DC500V
Minimum clearance distances	6mm	
Minimum creepage distances	6mm	
Between Ch1-Ch2		
Dielectric withstand voltage	AC2500V	1min, Cutoff 2mA
Test dielectric withstand voltage	AC2500V	1sec, Cutoff 2mA
Insulation resistance	$100M\Omega$ or more	DC500V
Minimum clearance distances	6mm	
Minimum creepage distances	6mm	

■Ambient Temperature Derating Curve

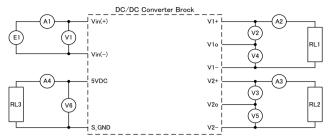
Reduce the input power according to the following temperature derating table.





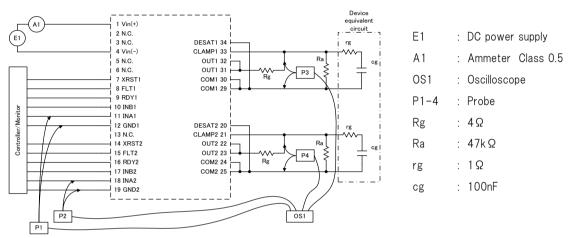
■Measure Circuit

[DC/DC converter]

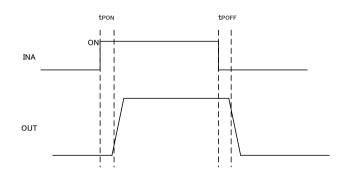


E1 : DC power supply A1-4 : Ammeter Class 0.5 RL1-3 : Electronic load V1-6 : Voltmeter Class 0.5

[Gate drive]

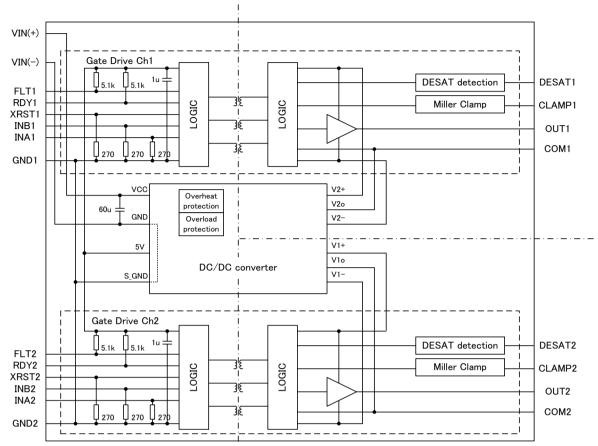


[Rising waveform/Falling waveform]





■Block Diagram





■Pin Connection

See the next section for details of pin functions

Input side

Pin No.	Name	CH	Explanation of pins
1	Vin(+)	Common	Power supply pin for DC/DC converter(+)
2	N.C.	-	Unused pin *Don't connect with other circuits.
3	N.C.	-	Unused pin *Don't connect with other circuits.
4	Vin(-)	Common	Power supply pin for DC/DC converter(-)
5	N.C.	-	Unused pin *Don't connect with other circuits.
6	N.C.	-	Unused pin *Don't connect with other circuits.
7	XRST1	1	Reset input pin
8	FLT1	1	Fault output pin
9	RDY1	1	Ready output pin
10	INB1	1	Opposite driver's control input pin
11	INA1	1	Control input pin
12	GND1	1	Ground pin for control circuit
13	N.C.	-	Unused pin *Don't connect with other circuits.
14	XRST2	2	Reset input pin
15	FLT2	2	Fault output pin
16	RDY2	2	Ready output pin
17	INB2	2	Opposite driver's control input pin
18	INA2	2	Control input pin
19	GND2	2	Ground pin for control circuit

Output side

Pin No.	Name	CH	Explanation of pins
20	DESAT2	2	Desaturation protection pin
21	CLAMP2	2	Miller clamp pin
22	OUT2	2	Gate drive pin
23	OUT2	2	Gate drive pin
24	COM2	2	Common pin
25	COM2	2	Common pin
26	NONE	-	None
27	NONE	-	None
28	NONE	-	None
29	COM1	1	Common pin
30	COM1	1	Common pin
31	OUT1	1	Gate drive pin
32	OUT1	1	Gate drive pin
33	CLAMP1	1	Miller clamp pin
34	DESAT1	1	Desaturation protection pin



Terminal Function

 \cdot Vin(+), Vin(-) (Power supply pin for DC/DC converter)

 \cdot GND(Ground pin for drive curcuit)

·INA, INB, XRST(Control input pin, XRST input pin)

The INA, INB and XRST pin is a pin used to determine output logic.

And XRST is in charge of setting back the FLT pin.

XRST	INB	INA	OUT
L	Х	Х	L
Н	Н	Х	L
Н	L	L	L
Н	L	Н	Н

FLT(Fault output pin)

The FLT pin is an open drain pin used to output a fault signal when desaturation function is activated, and will be cleared at the rising edge of FLT.

Status					
While in normal operation	Н				
When desaturation function is activated	L				

·RDY(Ready output pin)

The RDY pin shows the status of three internal protection features which are 5VDC UVLO, OUT(H) UVLO, and output state

feedback (OSFB). The term 'output state feedback' shows whether output internal logic is high or low corresponds to input logic or not.

Status					
While in normal operation	Н				
5VDC UVLO or OUT(H) UVLO or Output internal logic feedback	L				

$\cdot \text{OUT}(\text{Output pin})$

The OUT pin is a pin used to drive the gate of a power device.

·CLAMP(Miller clamp pin)

The CLAMP pin is a pin for preventing increase in gate voltage due to the miller current of the power device connected to OUT pin.

·DESAT(Desaturation protection pin)

The DESAT pin is a pin used to detect desaturation of IGBT/MOSFET. When the DESAT pin voltage exceeds V_{DESAT}, the DESAT function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the DESAT pin to the COM pin if the desaturation protection is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{DESATFIL} is set.

·COM(Common pin)

COM pin is a pin to be connected to the emitter / source of the power device.



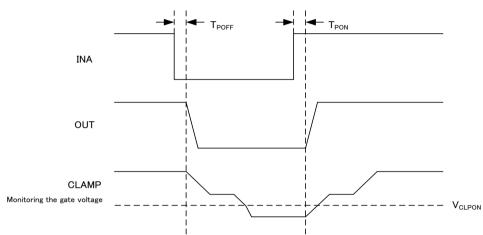


Description Of Protection

1. Gate voltage rise prevention function

If OUT=L and the CLAMP pin voltage < VCLPO	N, the internal MOSFET of the CLAMP pin turns on.
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OUT	CLAMP	Internal MOSFET of the CLAMP pin
L	Less than C_{CLPON}	ON
L	Not less than C_{CLPON}	OFF
Н	Х	OFF



Timing chart of Miller clamp function

2. Undervoltage Lockout (UVLO) function

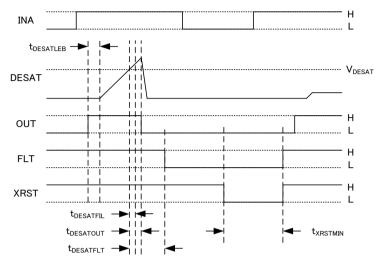
The control circuit incorporates the undervoltage lockout (UVLO) function both on the 5VDC and the OUT(H) sides. When the 5VDC or the OUT(H) voltage drops to the UVLO ON voltage, the OUT pin and the RDY pin both will output the "L"signal. When the 5VDC or the OUT(H) voltage rises to the UVLO OFF voltage, these pins will be reset. To prevent malfunctions due to noises, mask time t_{UVLO1MSK} and t_{UVLO2MSK} are set on both input and output sides.



3. Desaturation protection function(DESAT), Fault signal output function

When the DESAT pin voltage exceeds VDESAT, the DESAT function will be activated.

When the DESAT function is activated, the OUT pin voltage will be set to the "L" level, and then the FLT pin voltage to the "L" level. When the rising edge is put in the XRST pin, the DESAT function will be released.



DESAT Operation Timing Chart

No.	Status						Output					
INO.	Status	$\rm V_{5VDC}$	$V_{\rm OUTH}$	DESAT	XRST	INB	INA	CLAMP	OUT	CLAMP	FLT	RDY
1	V _{5VDC} UVLO	UVLO	Х	Х	Х	Х	Х	Н	L	Hi–Z	Η	L
2	V 5VDC UVLU	UVLO	Х	Х	Х	Х	Х	L	L	L	Η	L
3		0	UVLO	L	Х	Х	Х	Η	L	Hi-Z	Η	L
4	V _{OUTH} UVLO	0	UVLO	L	Х	Х	Х	L	L	L	Η	L
5	VOUTH OVEO	0	UVLO	Η	Х	Х	Х	Н	L	Hi-Z	L	L
6		0	UVLO	Η	Х	Х	Х	L	L	L	L	L
7	DESAT	0	0	Η	Х	Х	Х	Н	L	Hi-Z	L	H(*)
8	DEGAT	0	0	Η	Х	Х	Х	L	L	L	L	H(*)
9	XRST	0	0	L	L	Х	Х	Н	L	Hi-Z	Η	H(*)
10	XIXOT	0	0	L	L	Х	Х	L	L	L	Η	H(*)
11		0	0	L	Н	Н	Х	Н	L	Hi-Z	Н	H(*)
12	Normal operation	0	0	L	Η	Н	Х	L	L	L	Н	H(*)
13		0	0	L	Н	L	L	Η	L	Hi-Z	Η	H(*)
14		0	0	L	Η	L	L	L	L	L	Η	H(*)
15		0	0	L	Η	L	Н	Х	Н	Hi-Z	Н	H(*)

■I/O Condition Table

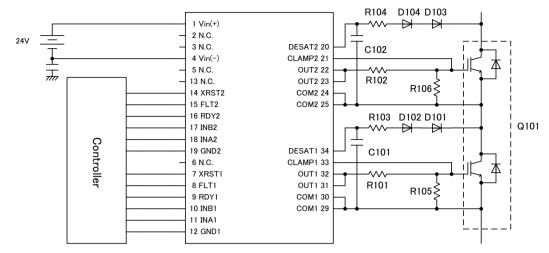
 \bigcirc : 5VDC or OUT(H) UVLO > UVLO, X : Don't care

(*) If the internal logic of high voltage side doesn't become the expected value, the RDY pin will become "L". And this stage is cleared automatically if the internal logic of high voltage side becomes the expected value.



Application

[Circuit example]



[Configuration example]

Symbol	Description	Part No.	Manufacturer		
Q101	IGBT				
D101-104	Diode	CMF05	TOSHIBA		
C101,102	Capacitor	100pF 25V			
R101,102	Resistor	**Ω 6W			
R103,104	Resistor	1kΩ			
R105,106	Resistor	47k Ω			



■Reliability

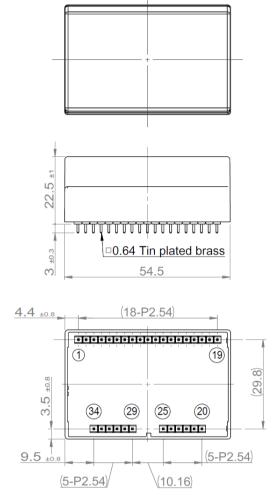
ltem	Test condition and acceptance criterion					
Exposure in high temperature	100℃, 240H, ※					
Exposure in low temperature	-30℃, 240H, ※					
Exposure in high temperature and high humidity	60℃, 90~95%RH, 240H, ※					
Thermal shock	30°C/30min to 100°C/30min, 500cycles, X					
Low temperature operation	Input voltage:DC24V, Output current:Rated Load					
	−30°C, 240H,					
High temperature operation	Input voltage:DC24V, Output current:Rated Load					
	85°C, 240H, 💥					
high temperature	Input voltage:DC24V, Output current:Rated Load					
and high humidity operation	60℃, 90~95%RH, 240H, ※					
Vibration	Vibration amplitude:1.5mm(peak to peak), Vibration Frequency:10 to 55Hz, Sweeping:1min.					
	In each X, Y and Z direction:once, 120min. 💥					
Impact	Acceleration:490m/s ² (50G), Operating time:11ms					
	In each \pm X, Y and Z direction:3 times, $~\%$					
Drop test for packaged freights	Dorp to concrete. Height:40cm					
	Dorp surface:1 corner, 3 spines, 6 surfaces, 1 time each.					
Solderblity	Sample shall be dipped into the solution of Methanol and Rosin					
	(having 75% Methanol and having 25% Rosin by weight measuring)					
	and shall be dippend into the solder bath having the solder Sn-3Ag-0.5Cu					
	of $250\pm5^\circ$ C to the position to 3mm from the end of terminal for 3.0 ± 0.5 seconds,					
	and pulled up. After above treatment, the sample shall be coveredby solder uniformly					
	at more than 75% of circumference and shall not show any unusual appearance.					
Resistance to soldering heat	Sample shall be dipped into the solution of Methanol and Rosin					
	(having 75% Methanol and having 25% Rosin by weight measuring)					
	and shall be dippend into the solder bath having the solder Sn-3Ag-0.5Cu					
	of 260 $\pm5^\circ\!\!\mathrm{C}$ to the position to 3mm from the end of terminal for 10.0 \pm 0.5					
	seconds, and pulled up. After that sample shall be replace in normal ambient					
	for 1 \sim 2 hours and shall not show any unusual appearance.					

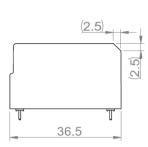
%After each test, exposure at room temperature and humidity condition for 24 hours.

There shall be no abnormality on the electrical specification and appearance.



■Outline Dimensional Drawing





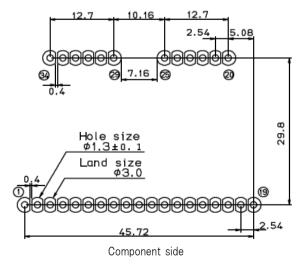
Note :1.The dimensional tolerance without directions is \pm 0.5mm.

Unit:mm

■Product Weight

75g(TYP)

■Recommended Hole Diameter And Land Size



 $\ensuremath{\mathbbmm{X}}\xspace$ The round pulling out figure is a pin numbering.

Unit:mm



■Recommended Soldering Condition

·Flow soldering condition

255±3°C Less than 5sec
 Temperature of preheating 110°C~130°C
 End temperature of preheating 110°C±10°C
 350°C(MAX) Less than 4sec

 $\cdot \, \text{Soldering}$ condition of hand work

Storage Conditions

ltem	Min	Max	Unit	Conditions.Note
Storage temperature	-25	60	°C	A packing state

%If you want to use past the long period there is a concern that the solder non-wetting by terminal oxidation to occur. Therefore, please use from taking enough tests.

■Usage Cautions

Always mount fuse on the plus side of input for ensuring safety because the fuse is not built-in the product.
 Please select the fuse considering conditions such as steady current, inrush current, and ambient temperature.
 When using a fuse having large rated current or high capacity input electrolytic condenser, by combining another converter and input line and input electrolytic condenser, fuse may not blow off in the case of abnormality.
 Do not combine high voltage line and fuse.

- This product is designed to be best when it drives two devices to have the same gate capacitance simultaneously.
 Because it leads to the "output unstable" and "output accuracy deterioration".
 If you want to use to drive only one of the devices, because of the output voltage accuracy deterioration prevention, please configure the dummy gate circuit (resistor and capacitor) to consume the equivalent of the power and the drive side.
- This product is to transmit the signal of the insulating part by the magnetic coupling.
 Therefore, if you use this product in a strong magnetic field in, there is a possibility of malfunction.
 In that case, connect the capacitor between the GND terminal of this product and a metal enclosure.
- Make sure the rise/fall time of the input signal is 500ns or less.



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 - · Use that involves exposure to direct sunlight, outdoor exposure, or dusty conditions.
 - · Use in locations where corrosive gases such as salt air, C12, H2S, NH3, SO2, or NO2, are present.
 - · Use in environments with strong static electricity or electromagnetic radiation.
 - · Use that involves placing inflammable material next to the product.
 - · Use of this product either sealed with a resin filling or coated with resin.
 - \cdot Use of water or a water soluble detergent for flux cleaning.
 - \cdot $\,$ Use in locations where condensation is liable to occur.
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