| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Convert to standardized military drawing format. Technical changes to table I. Editorial changes throughout. | 89-11-16 | M. A. Frye |
| B | Technical changes in 1.4 and table I. Editorial changes throughout. | 91-12-16 | M. A. Frye |
| C | Corrected title on sheet 1 to reflect actual device function. Update boilerplate to MIL-PRF-38535 requirements. – jak | 01-12-20 | Thomas M. Hess |
| D | Update boilerplate to MIL-PRF-38535 requirements. - LTG | 07-12-17 | Thomas M. Hess |

## Current CAGE CODE is 67268

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV STATUS | | | | REV | | | D | D | D | D | D | D | D | D | D | D | D | D | D | |
| OF SHEETS | | | | SHEET | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

PMIC N/A

PREPARED BY
Monica L. Poelking

CHECKED BY
Monica L. Poelking

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-01-14

REVISION LEVEL
D

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, HIGH-SPEED CMOS, DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR, MONOLITHIC SILICON

| SIZE | CAGE CODE | |
|---|---|---|
| A | **14933** | **5962-86847** |

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

| 5962-86847 | 01 | E | A |
|---|---|---|---|
| Drawing number | Device type (see 1.2.1) | Case outline (see 1.2.2) | Lead finish (see 1.2.3) |

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54HC123 | Dual retriggerable monostable multivibrator |
| 02 | 54HC123A | Dual retriggerable monostable multivibrator |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range ($V_{CC}$) ..... -0.5 V dc to +7.0 V dc
DC input voltage range ..... -0.5 V dc to $V_{CC}$ +0.5 V dc
DC output voltage range ..... -0.5 V dc to $V_{CC}$ +0.5 V dc
DC input diode current ..... ±20 mA
DC output diode current ..... ±20 mA
DC output current (per pin) ..... ±25 mA
DC $V_{CC}$ or GND current (per pin) ..... ±50 mA
Maximum power dissipation ($P_D$) ..... 500 mW 2/
Lead temperature (soldering, 10 seconds) ..... +260°C
Thermal resistance, junction-to-case ($\theta_{JC}$) ..... See MIL-STD-1835
Junction temperature ($T_J$) ..... +175°C
Storage temperature range ($T_{STG}$) ..... -65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range ($V_{CC}$) ..... +2.0 V dc to +6.0 V dc
Input voltage range ($V_{IN}$) ..... 0.0 V dc to $V_{CC}$
Output voltage range ($V_{OUT}$) ..... 0.0 V dc to $V_{CC}$
Case operating temperature range ($T_C$) ..... -55°C to +125°C
Input rise or fall time:
$V_{CC}$ = 2.0 V ..... 0 to 1000 ns
$V_{CC}$ = 4.5 V ..... 0 to 500 ns
$V_{CC}$ = 6.0 V ..... 0 to 400 ns

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For $T_C$ = +100°C to +125°C, derate linearly at 12 mW/°C.

1.4 Recommended operating conditions – Continued.

Minimum triggering pulse width, $\overline{An}$ Bn or $\overline{CLRn}$ ($t_{w1}$):
$T_C$ = +25°C:
$V_{CC}$ = 2.0 V ..... 123 ns
$V_{CC}$ = 4.5 V ..... 30 ns
$V_{CC}$ = 6.0 V ..... 21 ns
$T_C$ = -55°C/+125°C:
$V_{CC}$ = 2.0 V ..... 157 ns
$V_{CC}$ = 4.5 V ..... 42 ns
$V_{CC}$ = 6.0 V ..... 30 ns

Minimum output pulse width ($t_{w2}$):
Device type 01, $T_C$ = +25°C, $C_{EXT}$ = 10 nF:
$V_{CC}$ = 5.0 V dc, $R_{EXT}$ = 10kΩ ..... 40 µs to 50 µs
Device type 02, $T_C$ = +25°C, $C_{EXT}$ = 28 pF:
$V_{CC}$ = 2.0 V dc, $R_{EXT}$ = 6 kΩ ..... 0.85 µs
$V_{CC}$ = 4.5 V dc, $R_{EXT}$ = 2 kΩ ..... 220 ns
$V_{CC}$ = 6.0 V dc, $R_{EXT}$ = 2 kΩ ..... 170 ns

Minimum removal time, $\overline{CLRn}$ to $\overline{An}$, $\overline{CLRn}$ to Bn ($t_{REM}$):
Device type 01, $T_C$ = -55°C/+125°C:
$V_{CC}$ = 2.0 V ..... 75 ns
$V_{CC}$ = 4.5 V ..... 15 ns
$V_{CC}$ = 6.0 V ..... 13 ns
Device type 02, $T_C$ = -55°C/+125°C:
$V_{CC}$ = 2.0 V ..... 0 ns
$V_{CC}$ = 4.5 V ..... 0 ns
$V_{CC}$ = 6.0 V ..... 0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Test conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| High-level output voltage | $V_{OH}$<br>2/ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | 1.9 | | V |
| | | | $V_{CC} = 4.5$ V | | | 4.4 | | |
| | | | $V_{CC} = 6.0$ V | | | 5.9 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 4.0$ mA | $V_{CC} = 4.5$ V | | | 3.7 | | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 5.2$ mA | $V_{CC} = 6.0$ V | | | 5.2 | | |
| Low-level output voltage | $V_{OL}$<br>2/ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 20\ \mu A$ | $V_{CC} = 2.0$ V | All | 1, 2, 3 | | 0.1 | V |
| | | | $V_{CC} = 4.5$ V | | | | 0.1 | |
| | | | $V_{CC} = 6.0$ V | | | | 0.1 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 4.0$ mA | $V_{CC} = 4.5$ V | | | | 0.4 | |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$\lvert I_O \rvert \le 5.2$ mA | $V_{CC} = 6.0$ V | | | | 0.4 | |
| High-level input voltage | $V_{IH}$<br>3/ | | $V_{CC} = 2.0$ V | All | 1, 2, 3 | 1.5 | | V |
| | | | $V_{CC} = 4.5$ V | | | 3.15 | | |
| | | | $V_{CC} = 6.0$ V | | | 4.2 | | |
| Low-level input voltage | $V_{IL}$<br>3/ | | $V_{CC} = 2.0$ V | 01 | 1, 2, 3 | | 0.5 | V |
| | | | $V_{CC} = 4.5$ V | | | | 1.35 | |
| | | | $V_{CC} = 6.0$ V | | | | 1.8 | |
| | | | $V_{CC} = 2.0$ V | 02 | 1, 2, 3 | | 0.3 | |
| | | | $V_{CC} = 4.5$ V | | | | 0.9 | |
| | | | $V_{CC} = 6.0$ V | | | | 1.2 | |
| Quiescent supply current (standby) | $I_{CC1}$ | $V_{IN} = V_{CC}$ or GND<br>$I_{OUT} = 0\ \mu A$ | $V_{CC} = 6.0$ V | All | 1, 2, 3 | | 160 | µA |
| Active supply current (per monostable) | $I_{CC2}$ | $V_{IN} = V_{CC}$ or GND<br>$R/C_{EXT} = V_{CC/4}$<br>4/ 5/ | $V_{CC} = 2.0$ V | 01 | 1, 2, 3 | | 130 | µA |
| | | | $V_{CC} = 4.5$ V | | | | 1.6 | mA |
| | | | $V_{CC} = 6.0$ V | | | | 3.2 | |
| | | $V_{IN} = V_{CC}$ or GND<br>$R/C_{EXT} = 0.5\ V_{CC}$ | $V_{CC} = 2.0$ V | 02 | 1, 2, 3 | | 130 | µA |
| | | | $V_{CC} = 4.5$ V | | | | 1.6 | mA |
| | | | $V_{CC} = 6.0$ V | | | | 3.2 | |
| Input current | $I_{IN}$ | $V_{IN} = V_{CC}$ ($R/C_{EXT}$) 6/ | $V_{CC} = 6.0$ V | | 1, 2, 3 | | 5.0 | µA |
| | | $V_{IN} = GND$ ($R/C_{EXT}$) 6/ | | | | | -5.0 | |
| | | $V_{IN} = V_{CC}$ (all other pins) | | | | | 1.0 | |
| | | $V_{IN} = GND$ (all other pins) | | | | | -1.0 | |
| Functional tests | | See 4.3.1d | | | | 7 | | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Test conditions $-55°C \le T_C \le +125°C$ 1/ unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| Trigger propagation delay time, (An to Qn, Bn to Qn, $\overline{CLR}$n to Qn) | $t_{PLH1}$ 2/ | $C_L$ = 50 pF minimum See figure 4 | $V_{CC}$ = 2.0 V | 01 | 9 | | 300 | ns |
| | | | | | 10, 11 | | 450 | |
| | | | | 02 | 9 | | 169 | |
| | | | | | 10, 11 | | 210 | |
| | | | $V_{CC}$ = 4.5 V | 01 | 9 | | 60 | |
| | | | | | 10, 11 | | 90 | |
| | | | | 02 | 9 | | 42 | |
| | | | | | 10, 11 | | 57 | |
| | | | $V_{CC}$ = 6.0 V | 01 | 9 | | 51 | |
| | | | | | 10, 11 | | 76 | |
| | | | | 02 | 9 | | 32 | |
| | | | | | 10, 11 | | 44 | |
| Trigger propagation delay time, (An to Qn, Bn to $\overline{Qn}$, $\overline{CLR}$n to $\overline{Qn}$) | $t_{PHL1}$ 2/ | $C_L$ = 50 pF minimum See figure 4 | $V_{CC}$ = 2.0 V | 01 | 9 | | 320 | ns |
| | | | | | 10, 11 | | 480 | |
| | | | | 02 | 9 | | 197 | |
| | | | | | 10, 11 | | 250 | |
| | | | $V_{CC}$ = 4.5 V | 01 | 9 | | 64 | |
| | | | | | 10, 11 | | 96 | |
| | | | | 02 | 9 | | 48 | |
| | | | | | 10, 11 | | 67 | |
| | | | $V_{CC}$ = 6.0 V | 01 | 9 | | 54 | |
| | | | | | 10, 11 | | 82 | |
| | | | | 02 | 9 | | 38 | |
| | | | | | 10, 11 | | 51 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Test conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Propagation delay time, $\overline{CLR}n$ to Qn) | $t_{PLH2}$ 2/ | $C_L$ = 50 pF minimum<br>See figure 4 | $V_{CC}$ = 2.0 V | 01 | 9 | | 215 | ns |
| | | | | | 10, 11 | | 325 | |
| | | | | 02 | 9 | | 114 | |
| | | | | | 10, 11 | | 143 | |
| | | | $V_{CC}$ = 4.5 V | 01 | 9 | | 43 | |
| | | | | | 10, 11 | | 65 | |
| | | | | 02 | 9 | | 34 | |
| | | | | | 10, 11 | | 45 | |
| | | | $V_{CC}$ = 6.0 V | 01 | 9 | | 37 | |
| | | | | | 10, 11 | | 55 | |
| | | | | 02 | 9 | | 28 | |
| | | | | | 10, 11 | | 36 | |
| Propagation delay time, $\overline{CLR}n$ to $\overline{Qn}$) | $t_{PHL2}$ 2/ | $C_L$ = 50 pF minimum<br>See figure 4 | $V_{CC}$ = 2.0 V | 01 | 9 | | 215 | ns |
| | | | | | 10, 11 | | 325 | |
| | | | | 02 | 9 | | 116 | |
| | | | | | 10, 11 | | 147 | |
| | | | $V_{CC}$ = 4.5 V | 01 | 9 | | 43 | |
| | | | | | 10, 11 | | 65 | |
| | | | | 02 | 9 | | 36 | |
| | | | | | 10, 11 | | 46 | |
| | | | $V_{CC}$ = 6.0 V | 01 | 9 | | 37 | |
| | | | | | 10, 11 | | 55 | |
| | | | | 02 | 9 | | 29 | |
| | | | | | 10, 11 | | 37 | |

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Test conditions<br>$-55°C \le T_C \le +125°C$ 1/<br>unless otherwise specified | | Device type | Group A subgroups | Limits | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Output pulse width (standby) | $t_{WQ}$<br>2/, 5/ | $C_L$ = 50 pF minimum<br>$R_{EXT}$ = 10 kΩ, $C_{EXT}$ = 0.1 μF<br>See figure 4 | $V_{CC}$ = 5.0 V | 01 | 9 | 0.4 | 0.5 | ms |
| | | | | | 10, 11 | 0.38 | 0.52 | |
| | | | $V_{CC}$ = 4.5 V | 02 | 9 | 0.9 | 1.2 | |
| | | | | | 10, 11 | 0.70 | 1.15 | |
| Output rise and fall time | $t_{THL}$,<br>$t_{TLH}$<br>5/ | $C_L$ = 50 pF minimum<br>See figure 4 | $V_{CC}$ = 2.0 V | All | 9 | | 75 | ns |
| | | | | | 10, 11 | | 110 | |
| | | | $V_{CC}$ = 4.5 V | | 9 | | 15 | |
| | | | | | 10, 11 | | 22 | |
| | | | $V_{CC}$ = 6.0 V | | 9 | | 13 | |
| | | | | | 10, 11 | | 19 | |
| Maximum input capacitance | $C_{IN}$ | R/$C_{EXT}$, See 4.3.1c | | All | 4 | | 20 | pF |
| | | Other inputs, See 4.3.1c | | | | | 10 | |

1/ For a power supply of 5.0 V ±10% the worst-case output voltage ($V_{OH}$ and $V_{OL}$) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case $V_{IN}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V, respectively. (The $V_{IH}$ value at $V_{CC}$ = 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$ and $I_{CC}$) occur for CMOS at the higher voltage so the 6.0 V values should be used.

2/ Testing at $V_{CC}$ = 2.0 V and $V_{CC}$ = 6.0 V shall be guaranteed, if not tested, to the specified limit in table I.

3/ $V_{IH}$ and $V_{IL}$ tests are not required if applied as forcing functions for the $V_{OH}$ and $V_{OL}$ tests.

4/ Limit current to $I_{OL}$ or use a suitable series resistor ≥ 500Ω; perform test while Q is high.

5/ Guaranteed, if not tested, to the limits specified in table I.

6/ When testing $I_{IL}$, the Q output must be high, if Q is low (device not triggered) the pull-up P device will be on and the low resistance path from $V_{DD}$ to the test pin will cause a current far exceeding the specification.

| Device types | 01 and 02 | |
|---|---|---|
| Case outlines | E | 2 |
| Terminal number | Terminal symbol | |
| 1 | $\overline{A1}$ | NC |
| 2 | B1 | $\overline{A1}$ |
| 3 | $\overline{CLR1}$ | B1 |
| 4 | $\overline{Q1}$ | $\overline{CLR1}$ |
| 5 | Q2 | $\overline{Q1}$ |
| 6 | $C_{EXT}2$ | NC |
| 7 | $R_{EXT}2,C_{EXT}$ | Q2 |
| 8 | GND | $C_{EXT}2$ |
| 9 | $\overline{A2}$ | $R_{EXT}2,C_{EXT}$ |
| 10 | B2 | GND |
| 11 | $\overline{CLR2}$ | NC |
| 12 | $\overline{Q2}$ | $\overline{A2}$ |
| 13 | Q1 | B2 |
| 14 | $C_{EXT}1$ | $\overline{CLR2}$ |
| 15 | $R_{EXT}1$, $C_{EXT}$ | $\overline{Q2}$ |
| 16 | $V_{CC}$ | NC |
| 17 | - - - | Q1 |
| 18 | - - - | $C_{EXT}1$ |
| 19 | - - - | $R_{EXT}1$, $C_{EXT}$ |
| 20 | - - - | $V_{CC}$ |

FIGURE 1. Terminal connections.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{CLRn}$ | $\overline{An}$ | Bn | Qn | $\overline{Qn}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⎍ | ⎌ |
| H | ↓ | H | ⎍ | ⎌ |
| ↑ | L | H | ⎍ | ⎌ |

H = High voltage level
L = Low voltage level
X = Irrelevant
↓ = High to low clock transition
↑ = Low to high clock transition
⎍ = One high level pulse
⎌ = One low level pulse

FIGURE 2. Truth table.

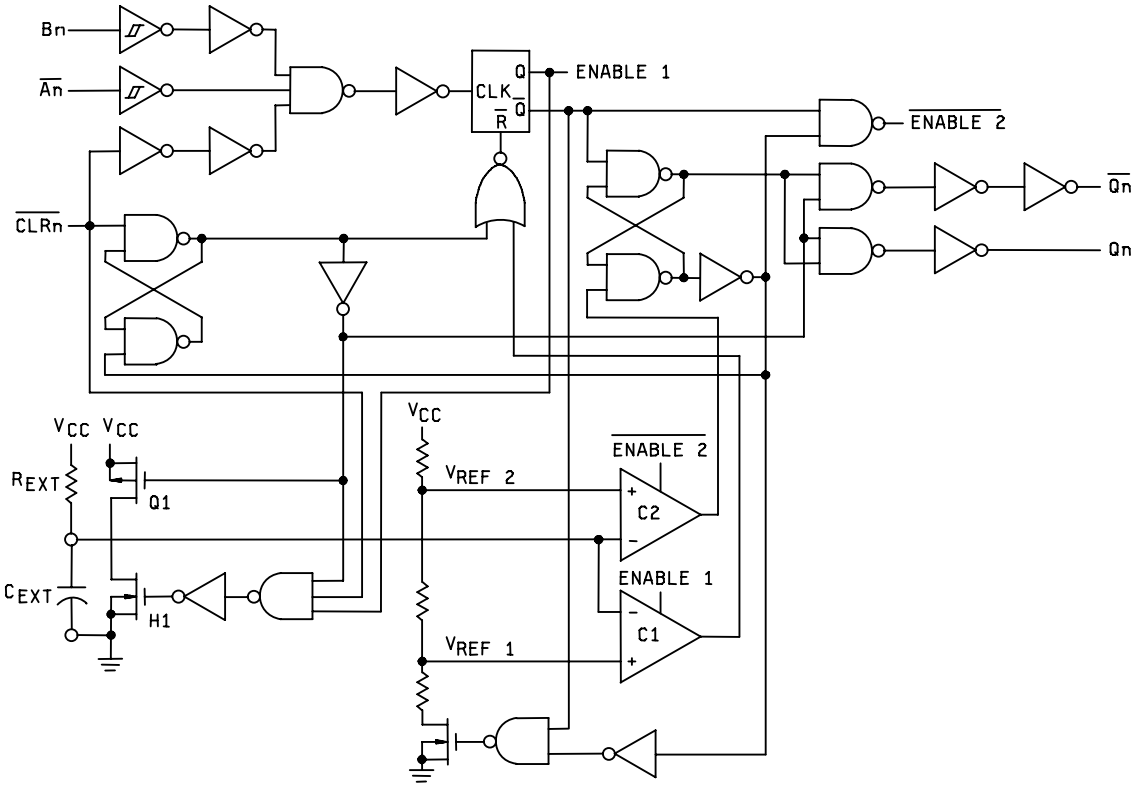
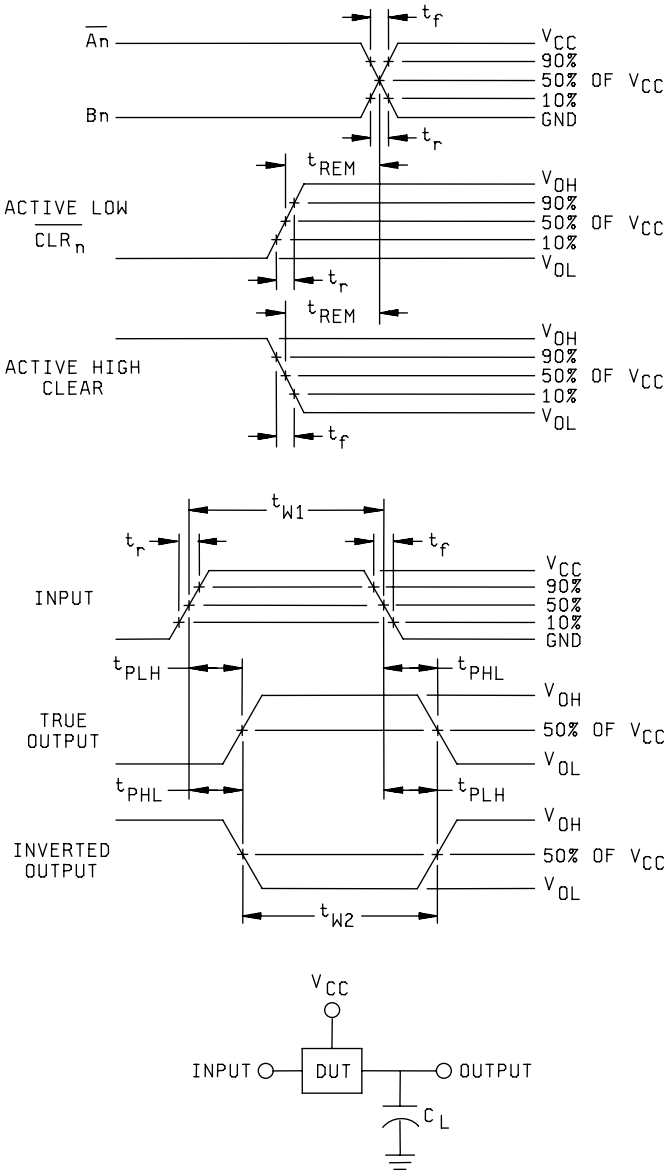



FIGURE 3. Logic diagram.




NOTES:

1. $C_L$ = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50Ω, $t_r$ = 6.0 ns, $t_f$ = 6.0 ns.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | 1 |
| Final electrical test parameters (method 5004) | 1, 2, 3, 7, 9 1/ |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 9, 10, 11 2/ |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_{IN}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-12-17

Approved sources of supply for SMD 5962-86847 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-8684701EA | 01295 | CD54HC123F3A |
| 5962-8684702EA | 0C7V7 | MM54HC123AJ/883 |
| 5962-86847022A | 0C7V7 | MM54HC123AE/883 |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments Incorporated<br>Semiconductor Group<br>8505 Forest Lane<br>P.O. Box 660199<br>Dallas, TX 75243<br>Point of contact: U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.