REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add logic diagram as shown in figure 3. Redraw switching waveforms and test circuit as shown in figure 4. Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. – jak	06-05-02	Thomas M. Hess

REV																			
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REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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DRAWING APPROVAL DATE
90-03-05

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, OCTAL D-TYPE FLIP-FLOP WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89658**

SHEET 1 OF 12

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89658	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT534	Octal D-type flip-flop with three-state outputs, TTL compatible inputs
02	54ACT11534	Octal D-type flip-flop with three-state outputs, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
Input clamp diode current (I_{IK}) ..... ±20 mA
Output clamp diode current (I_{OK}) ..... ±50 mA
DC V_{CC} or GND current (per pin) (I_{CC}, I_{GND}) ..... ±100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) 2/ ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... 0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... 0.0 V dc to V_{CC}
Case operating temperature range (T_C) ..... -55°C to +125°C
Input rise or fall time (t_r and t_f):
V_{CC} = 4.5 V and 5.5 V ..... 8 ns/V

1/ Unless other wise specified, all voltages are referenced to ground.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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1.4 Recommended operating conditions - Continued.

Minimum setup time, Dn to CP (t_s):
Device type 01:
T_C = +25°C, V_{CC} = 4.5 V ..... 4.5 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 5.0 ns
Device type 02:
T_C = +25°C, V_{CC} = 4.5 V ..... 3.0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 3.0 ns
Minimum hold time, Dn to CP (t_h):
Device type 01:
T_C = +25°C, V_{CC} = 4.5 V ..... 2.5 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 3.0 ns
Device type 02:
T_C = +25°C, V_{CC} = 4.5 V ..... 5.5 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 5.5 ns
Minimum pulse width, CP (t_w):
Device type 01:
T_C = +25°C, V_{CC} = 4.5 V ..... 5.0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 5.0 ns
Device type 02:
T_C = +25°C, V_{CC} = 4.5 V ..... 9.0 ns
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 9.0 ns
Maximum clock frequency (f_{MAX}):
Device type 01:
T_C = +25°C, V_{CC} = 4.5 V ..... 95 MHz
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 85 MHz
Device type 02:
T_C = +25°C, V_{CC} = 4.5 V ..... 55 MHz
T_C = -55°C to +125°C, V_{CC} = 4.5 V ..... 55 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH} 1/	V_{IN} = 2.0 V or 0.8 V I_{OH} = -50 µA	4.5 V	All	1, 2, 3	4.4		V
			5.5 V			5.4		
		V_{IN} = 2.0 V or 0.8 V I_{OH} = -24 mA	4.5 V			3.7		V
			5.5 V			4.7		
		V_{IN} = 2.0 V or 0.8 V I_{OH} = -50 mA	5.5 V			3.85		V
Low level output voltage	V_{OL} 1/	V_{IN} = 2.0 V or 0.8 V I_{OL} = 50 µA	4.5 V	All	1, 2, 3		0.1	V
			5.5 V				0.1	
		V_{IN} = 2.0 V or 0.8 V I_{OL} = 24 mA	4.5 V				0.5	V
			5.5 V				0.5	
		V_{IN} = 2.0 V or 0.8 V I_{OL} = 50 mA	5.5 V				1.65	V
High level input voltage	V_{IH} 2/		4.5 V	All	1, 2, 3	2.0		V
			5.5 V			2.0		
Low level input voltage	V_{IL} 2/		4.5 V	All	1, 2, 3		0.8	V
			5.5 V				0.8	
Input leakage current	I_{IL}	V_{IN} = 0.0 V	5.5 V	All	1, 2, 3		-1.0	µA
	I_{IH}	V_{IN} = 5.5 V			1, 2, 3		1.0	
Additional quiescent supply current, TTL input levels	ΔI_{CC}	Any one input, V_{IN} = 3.4 V Other inputs, V_{IN} = V_{CC} or GND	5.5 V	All	1, 2, 3		1.6	mA
Quiescent supply current	I_{CCH}	V_{IN} = V_{CC} or GND	5.5 V	All	1, 2, 3		160	µA
	I_{CCL}						160	
	I_{CCZ}						160	
Three-state output leakage current	I_{OZH}	V_{IN} = 2.0 V or 0.8 V V_{OUT} = V_{CC} or GND	5.5 V	All	1, 2, 3		10.0	µA
	I_{OZL}				1, 2, 3		-10.0	
Input capacitance	C_{IN}	See 4.3.1c, T_C = +25°C		All	4		8.0	pF
Power dissipation capacitance	C_{PD} 3/	See 4.3.1c, T_C = +25°C		01	4		50	pF
				02			115	
Functional tests		See 4.3.1d	4.5 V and 5.5 V	All	7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Device type	Group A subgroups	Limits		Unit
						Min	Max	
Propagation delay time, CP to $\overline{Qn}$	t_{PHL} 4/	R_L = 500Ω C_L = 50 pF See figure 4	4.5 V	01	9	1.0	10.5	ns
					10, 11	1.0	13.0	
			4.5 V	02	9	1.5	13.3	ns
					10, 11	1.5	16.3	
	t_{PLH} 4/		4.5 V	01	9	1.0	11.5	ns
					10, 11	1.0	14.0	
			4.5 V	02	9	1.5	12.7	ns
					10, 11	1.5	15.7	
Propagation delay time, output enable, $\overline{OE}$ to Qn	t_{PZH} 4/	R_L = 500Ω C_L = 50 pF See figure 4	4.5 V	01	9	1.0	12.0	ns
					10, 11	1.0	14.0	
			4.5 V	02	9	1.5	12.0	ns
					10, 11	1.5	14.2	
	t_{PZL} 4/		4.5 V	01	9	1.0	11.0	ns
					10, 11	1.0	13.0	
			4.5 V	02	9	1.5	12.2	ns
					10, 11	1.5	14.5	
Propagation delay time, output disable, $\overline{OE}$ to Qn	t_{PHZ} 4/	R_L = 500Ω C_L = 50 pF See figure 4	4.5 V	01	9	1.0	12.5	ns
					10, 11	1.0	14.5	
			4.5 V	02	9	1.5	12.9	ns
					10, 11	1.5	13.9	
	t_{PLZ} 4/		4.5 V	01	9	1.0	10.5	ns
					10, 11	1.0	11.5	
			4.5 V	02	9	1.5	11.2	ns
					10, 11	1.5	12.5	

1/ The V_{OH} and v_{OL} tests will be tested at V_{CC} = 4.5 V. V_{CC} = 5.5 V will be guaranteed, if not tested, to the limits in table I. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum.

2/ The V_{IH} and V_{IL} tests are not required, and shall be used as forcing functions for the V_{OH} and V_{OL} tests.

3/ Power dissipation capacitance (C_{PD}) determines the dynamic power consumption (P_D) and the dynamic current consumption (I_S) where:

$P_D = (C_{PD} + C_L)V_{CC}^2 f + (V_{CC} \times I_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L)V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$

f is the frequency of the input signal; n is the number of device inputs at TTL levels; d is duty cycle of the input signal; and C_L is the external output load capacitance.

4/ AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits are guaranteed for V_{CC} = 5.5 V by guardbanding V_{CC} = 4.5 V limits to 1.5 ns minimum.

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Device types	01	02	
Case outlines	R, S, and 2	L	3
Terminal number	Terminal symbol		
1	$\overline{OE}$	$\overline{Q0}$	NC
2	$\overline{Q0}$	$\overline{Q1}$	V_{CC}
3	D0	$\overline{Q2}$	D3
4	$\overline{D1}$	$\overline{Q3}$	D2
5	$\overline{Q1}$	GND	D1
6	$\overline{Q2}$	GND	$\overline{D0}$
7	D2	GND	$\overline{OE}$
8	$\overline{D3}$	GND	$\overline{NC}$
9	$\overline{Q3}$	$\overline{Q4}$	$\overline{Q0}$
10	GND	$\overline{Q5}$	$\overline{Q1}$
11	$\overline{CP}$	$\overline{Q6}$	$\overline{Q2}$
12	$\overline{Q4}$	$\overline{Q7}$	$\overline{Q3}$
13	D4	CP	GND
14	$\overline{D5}$	D7	GND
15	$\overline{Q5}$	D6	NC
16	$\overline{Q6}$	D5	GND
17	D6	D4	GND
18	$\overline{D7}$	V_{CC}	$\overline{Q4}$
19	$\overline{Q7}$	V_{CC}	$\overline{Q5}$
20	V_{CC}	D3	$\overline{Q6}$
21	- - -	D2	$\overline{Q7}$
22	- - -	D1	NC
23	- - -	D0	CP
24	- - -	$\overline{OE}$	D7
25	- - -	- - -	D6
26	- - -	- - -	D5
27	- - -	- - -	D4
28	- - -	- - -	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Inputs			Outputs
Dn	CP	$\overline{OE}$	$\overline{Qn}$
H	↑	L	L
L	↑	L	H
X	L	L	$\overline{Q0}$
X	X	H	Z

H = High voltage level
L = Low voltage level
Z = High impedance
↑ = Low-to-high transition of the clock
$\overline{Q0}$ = Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

FIGURE 2. Truth table.

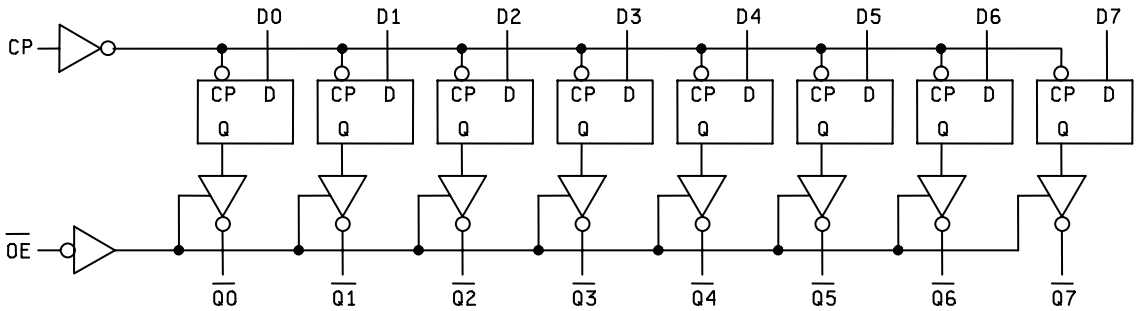

FIGURE 3. Logic diagram.

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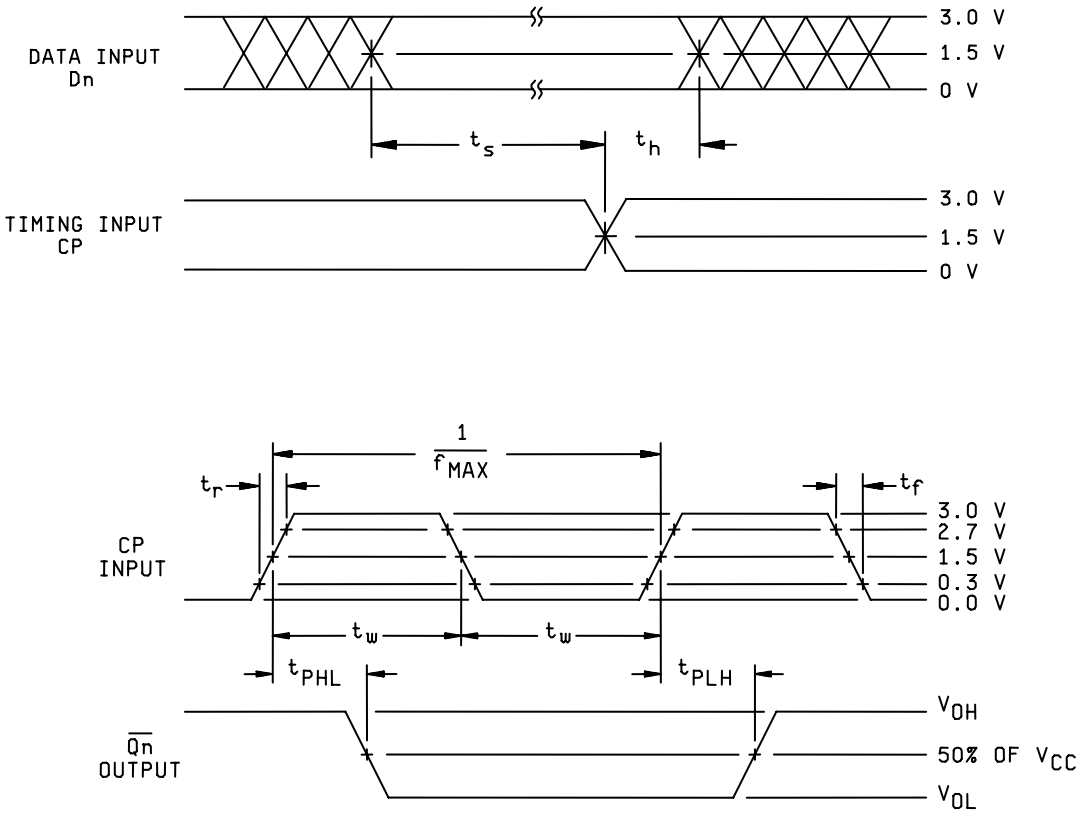

FIGURE 4. Switching waveforms and test circuit.

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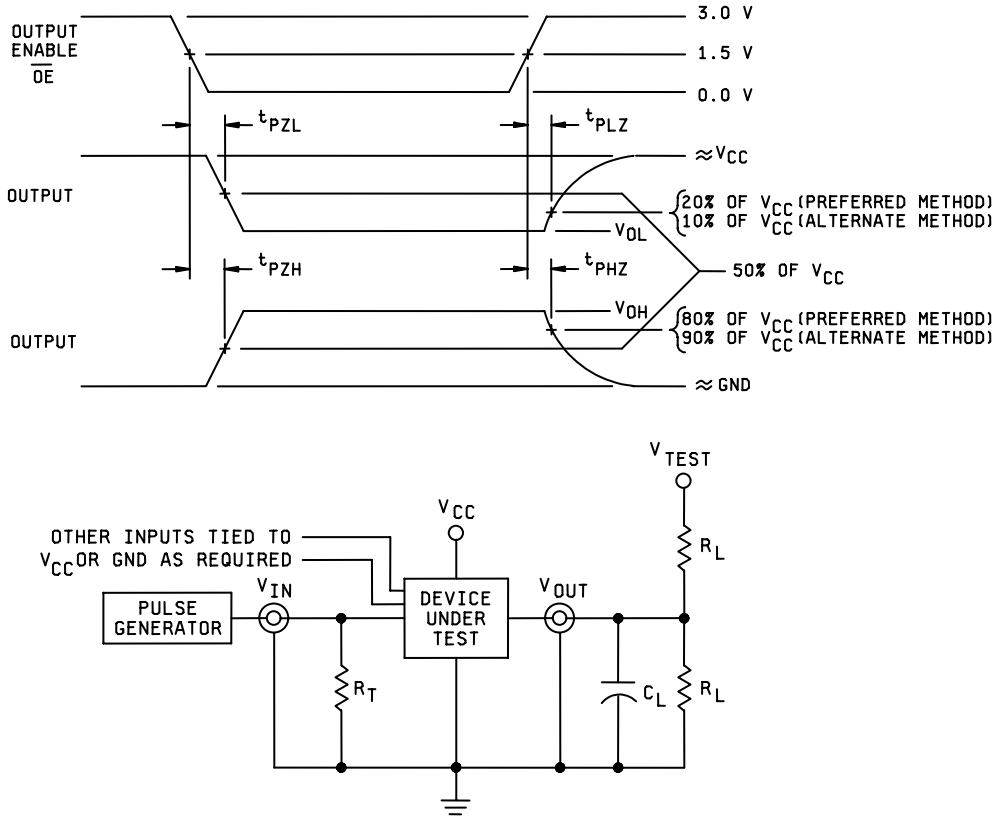

NOTES:

1. Preferred method:

   When measuring t_{PHZ} and r_{PZH}: V_{TEST} = GND.

   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 x V_{CC}.

   When measuring t_{PLH} and t_{PHL}: V_{TEST} = open.

   Alternating method:

   When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 2 x V_{CC}.

   When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = open.
2. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
3. R_T = 50Ω or equivalent, R_L = 500Ω or equivalent.
4. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{PD} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 and 8 tests shall include verification of the truth table as specified on figure 2.

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-05-02

Approved sources of supply for SMD 5962-89658 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8965801RA	27014 0C7V7	54ACT534DMQB 54ACT534DMQB
5962-8965801SA	27014 0C7V7	54ACT534FMQB 54ACT534FMQB
5962-89658012A	27014 0C7V7	54ACT534LMQB 54ACT534LMQB
5962-8965802LA	3V146	54ACT11534/BLA
5962-89658023A	3V146	54ACT11534/B3A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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