

8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUT REGISTERS

Check for Samples: [SN54HC595](#) [SN74HC595](#)

FEATURES

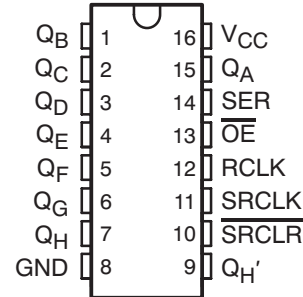
- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads
- Low Power Consumption: 80- μ A (Max) I_{CC}
- $t_{pd} = 13$ ns (Typ)
- ± 6 -mA Output Drive at 5 V
- Low Input Current: 1 μ A (Max)
- Shift Register Has Direct Clear

DESCRIPTION

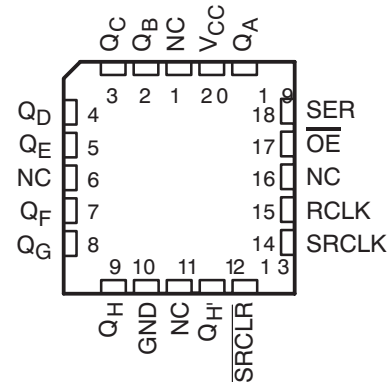
The 'HC595 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, the outputs are in the high-impedance state.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

SN54HC595...J OR W PACKAGE
SN74HC595...D, DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC595...FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

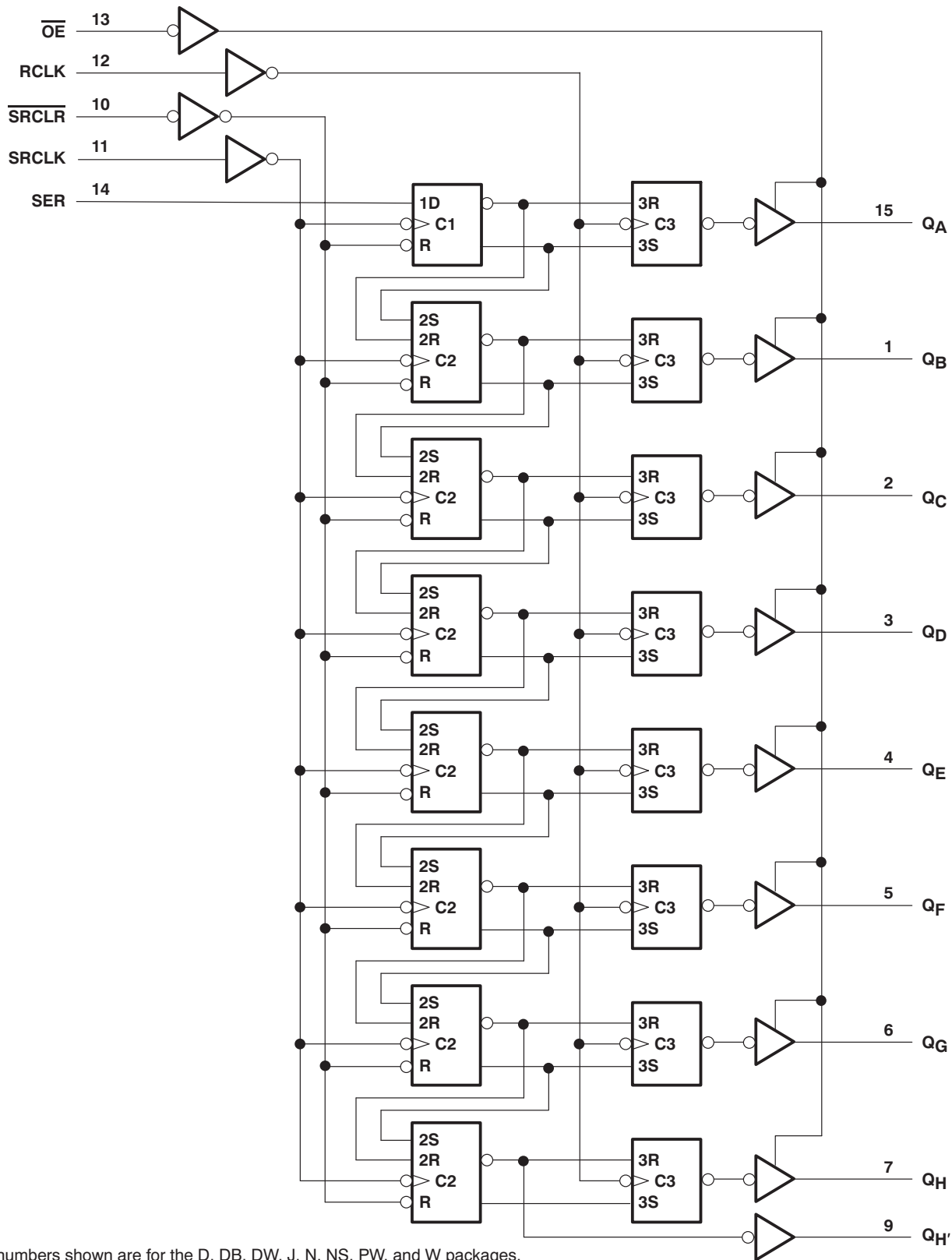
| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube of 25 | SN74HC595N | SN74HC595N |
| | SOIC – D | Tube of 40 | SN74HC595D | HC595 |
| | | Reel of 2500 | SN74HC595DR | |
| | | Reel of 250 | SN74HC595DT | |
| | SOIC – DW | Tube of 40 | SN74HC595DW | HC595 |
| | | Reel of 2000 | SN74HC595DWR | |
| | SOP – NS | Reel of 2000 | SN74HC595NSR | HC595 |
| | SSOP – DB | Reel of 2000 | SN74HC595DBR | HC595 |
| | TSSOP – PW | Tube of 90 | SN74HC595PW | HC595 |
| | | Reel of 2000 | SN74HC595PWR | |
| -55°C to 125°C | CDIP – J | Tube of 25 | SNJ54HC595J | SNJ54HC595J |
| | CFP – W | Tube of 150 | SNJ54HC595W | SNJ54HC595W |
| | LCCC – FK | Tube of 55 | SNJ54HC595FK | SNJ54HC595FK |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Table 1. FUNCTION TABLE

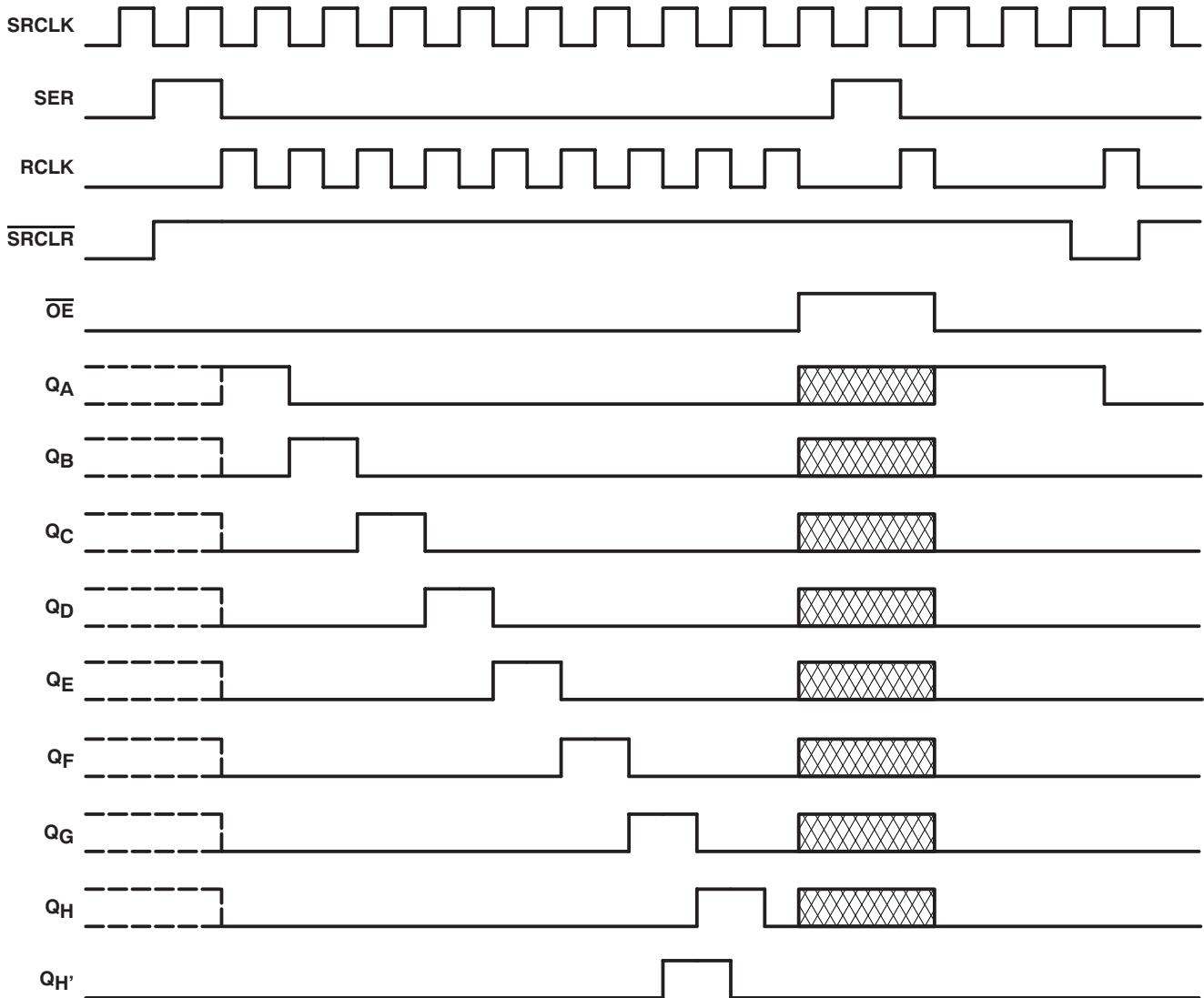
| INPUTS | | | | | FUNCTION |
|--------|-------|-------|------|----|--|
| SER | SRCLK | SRCLR | RCLK | OE | |
| X | X | X | X | H | Outputs Q _A –Q _H are disabled. |
| X | X | X | X | L | Outputs Q _A –Q _H are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | ↑ | X | Shift-register data is stored in the storage register. |


LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the D, DB, DW, J, N, NS, PW, and W packages.

TIMING DIAGRAM



NOTE:  implies that the output is in 3-State mode.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | |
|---------------|--|-----------------------------|----------------|
| V_{CC} | Supply voltage range | | -0.5 V to 7 V |
| I_{IK} | Input clamp current ⁽²⁾ | $V_I < 0$ or $V_I > V_{CC}$ | ±20 mA |
| I_{OK} | Output clamp current ⁽²⁾ | $V_O < 0$ or $V_O > V_{CC}$ | ±20 mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | ±35 mA |
| | Continuous current through VCC or GND | | ±70 mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | D package | 73°C/W |
| | | DB package | 82°C/W |
| | | DW package | 57°C/W |
| | | N package | 67°C/W |
| | | NS package | 64°C/W |
| | | PW package | 108°C/W |
| T_{stg} | Storage temperature range | | -65°C to 150°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | SN54HC595 | | | SN74HC595 | | | UNIT |
|---------------------|--|------------------|------|----------|-----------|------|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | 1.5 | | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | 3.15 | | | |
| | | $V_{CC} = 6$ V | 4.2 | | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | | 0.5 | | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | | 1.35 | | |
| | | $V_{CC} = 6$ V | | 1.8 | | 1.8 | | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time ⁽²⁾ | $V_{CC} = 2$ V | | 1000 | | 1000 | | ns |
| | | $V_{CC} = 4.5$ V | | 500 | | 500 | | |
| | | $V_{CC} = 6$ V | | 400 | | 400 | | |
| T_A | Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) If this device is used in the threshold region (from $V_{ILmax} = 0.5$ V to $V_{IHmin} = 1.5$ V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_i = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT |
|--|---|--------------------------|--|-----------------------|-------|------|-----------|------|-----------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | 4.5 V | Q _H ', I _{OH} = -4 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | Q _A -Q _H , I _{OH} = -6 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | 6 V | Q _H ', I _{OH} = -5.2 mA | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| Q _A -Q _H , I _{OH} = -7.8 mA | 5.48 | | 5.8 | | 5.2 | | 5.34 | | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | Q _H ', I _{OL} = 4 mA | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | | Q _A -Q _H , I _{OL} = 6 mA | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | 6 V | Q _H ', I _{OL} = 5.2 mA | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| Q _A -Q _H , I _{OL} = 7.8 mA | | | 0.15 | 0.26 | | 0.4 | | 0.33 | | | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA | |
| I _{OZ} | V _O = V _{CC} or 0, Q _A -Q _H | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | | 160 | | 80 | μA | |
| C _i | | 2 V to 6 V | | | 3 | 10 | | 10 | | 10 | pF |

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC595 | | SN74HC595 | | UNIT |
|--------------------|---|---------------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | 4.5 V | | 31 | | 21 | | 25 | |
| | | 6 V | | 36 | | 25 | | 29 | |
| t _w | Pulse duration | SRCLK or RCLK high or low | 2 V | 80 | | 120 | | 100 | ns |
| | | | 4.5 V | 16 | | 24 | | 20 | |
| | | | 6 V | 14 | | 20 | | 17 | |
| | $\overline{\text{SRCLR}}$ low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | Setup time | SER before SRCLK↑ | 2 V | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | |
| | | | 6 V | 17 | | 25 | | 21 | |
| | SRCLK↑ before RCLK↑ ⁽¹⁾ | 2 V | 75 | | 113 | | 94 | | |
| | | 4.5 V | 15 | | 23 | | 19 | | |
| | | 6 V | 13 | | 19 | | 16 | | |
| | $\overline{\text{SRCLR}}$ low before RCLK↑ | 2 V | 50 | | 75 | | 65 | | |
| | | 4.5 V | 10 | | 15 | | 13 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| | $\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑ | 2 V | 50 | | 75 | | 60 | | |
| | | 4.5 V | 10 | | 15 | | 12 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| t _h | Hold time, SER after SRCLK↑ | 2 V | | 0 | | 0 | | ns | |
| | | 4.5 V | | 0 | | 0 | | | |
| | | 6 V | | 0 | | 0 | | | |

- (1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC595 | | SN74HC595 | | UNIT |
|-----------|---------------------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 26 | | 4.2 | | 5 | MHz | |
| | | | 4.5 V | 31 | 38 | | 21 | | 25 | | |
| | | | 6 V | 36 | 42 | | 25 | | 29 | | |
| t_{pd} | SRCLK | $Q_{H'}$ | 2 V | | 50 | 160 | | 240 | | 200 | ns |
| | | | 4.5 V | | 17 | 32 | | 48 | | 40 | |
| | | | 6 V | | 14 | 27 | | 41 | | 34 | |
| | RCLK | Q_A-Q_H | 2 V | | 50 | 150 | | 225 | | 187 | |
| | | | 4.5 V | | 17 | 30 | | 45 | | 37 | |
| | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| t_{PHL} | $\overline{\text{SRCLR}}$ | $Q_{H'}$ | 2 V | | 51 | 175 | | 261 | | 219 | ns |
| | | | 4.5 V | | 18 | 35 | | 52 | | 44 | |
| | | | 6 V | | 15 | 30 | | 44 | | 37 | |
| t_{en} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 40 | 150 | | 255 | | 187 | ns |
| | | | 4.5 V | | 15 | 30 | | 45 | | 37 | |
| | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t_{dis} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 42 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 20 | 34 | | 51 | | 43 | |
| t_t | | Q_A-Q_H | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |
| | | $Q_{H'}$ | 2 V | | 28 | 75 | | 110 | | 95 | |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted)

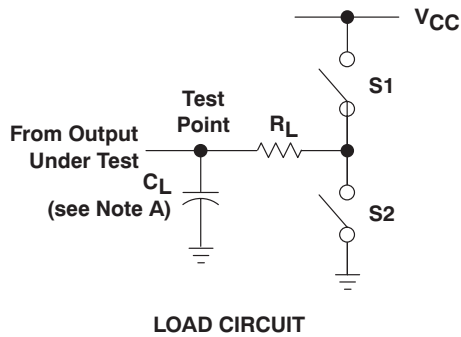
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC595 | | SN74HC595 | | UNIT |
|-----------|------------------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | RCLK | Q_A-Q_H | 2 V | | 60 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 22 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t_{en} | $\overline{\text{OE}}$ | Q_A-Q_H | 2 V | | 70 | 200 | | 298 | | 250 | ns |
| | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t_t | | Q_A-Q_H | 2 V | | 45 | 210 | | 315 | | 265 | ns |
| | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | 6 V | | 13 | 36 | | 53 | | 45 | |

OPERATING CHARACTERISTICS

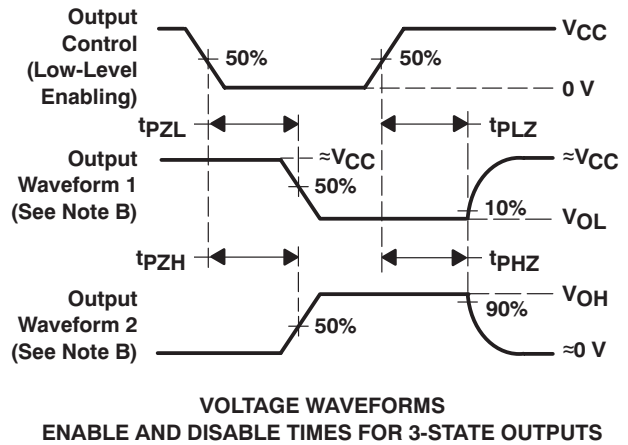
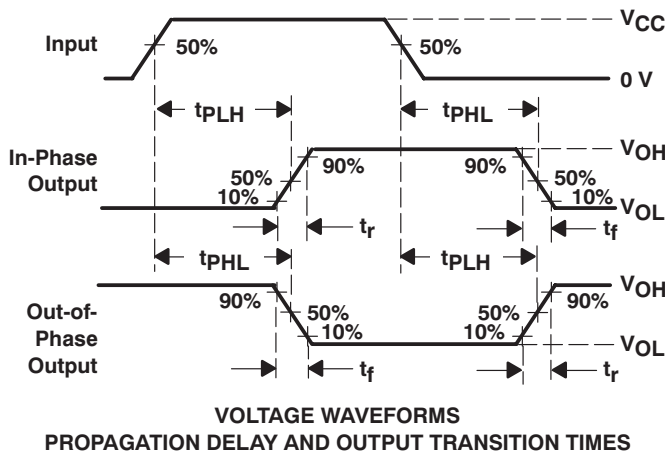
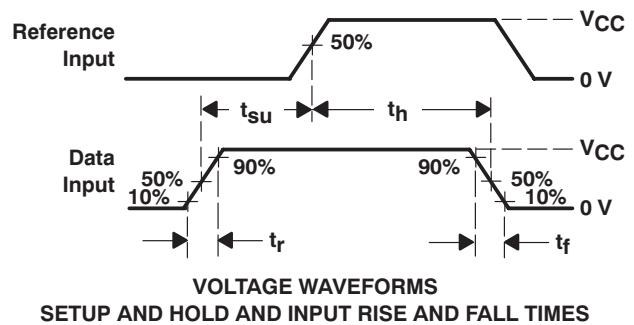
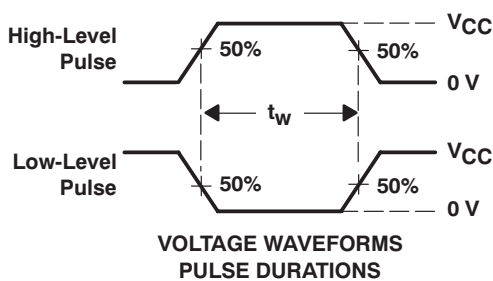
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 400 | pF |

PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | | 50 pF or 150 pF | Open | Open |



- NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 E. The outputs are measured one at a time, with one input transition per measurement.
 F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 G. t_{PZL} and t_{PZH} are the same as t_{en} .
 H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-86816012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-8681601EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-8681601VEA | ACTIVE | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| 5962-8681601VFA | ACTIVE | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | |
| SN54HC595J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74HC595D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DBR | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DRG3 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | |
| SN74HC595DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74HC595DWE4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DWRE4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC595NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74HC595NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74HC595PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SNJ54HC595FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54HC595J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54HC595W | OBSOLETE | | | 16 | | TBD | Call TI | Call TI | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC595, SN54HC595-SP, SN74HC595 :

● Catalog: [SN74HC595](#), [SN54HC595](#)

● Enhanced Product: [SN74HC595-EP](#), [SN74HC595-EP](#)

● Military: [SN54HC595](#)

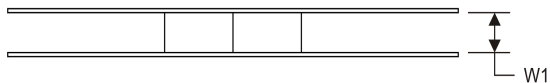
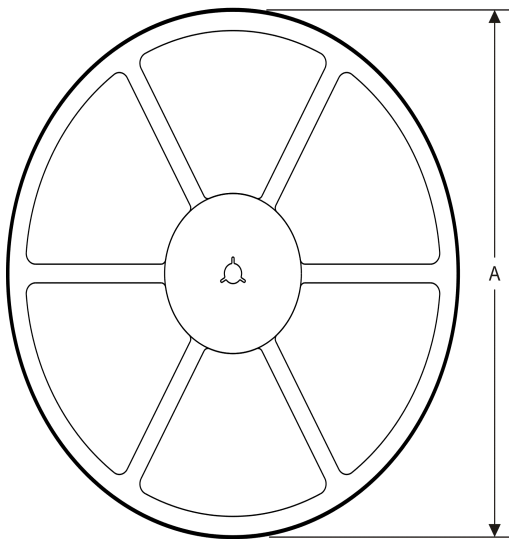
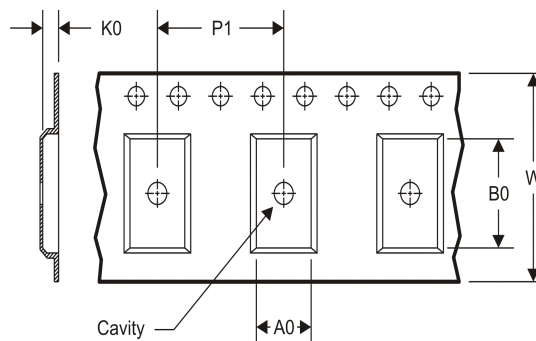
● Space: [SN54HC595-SP](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC595DBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN74HC595NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC595DBR | SSOP | DB | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74HC595DWR | SOIC | DW | 16 | 2000 | 366.0 | 364.0 | 50.0 |
| SN74HC595NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

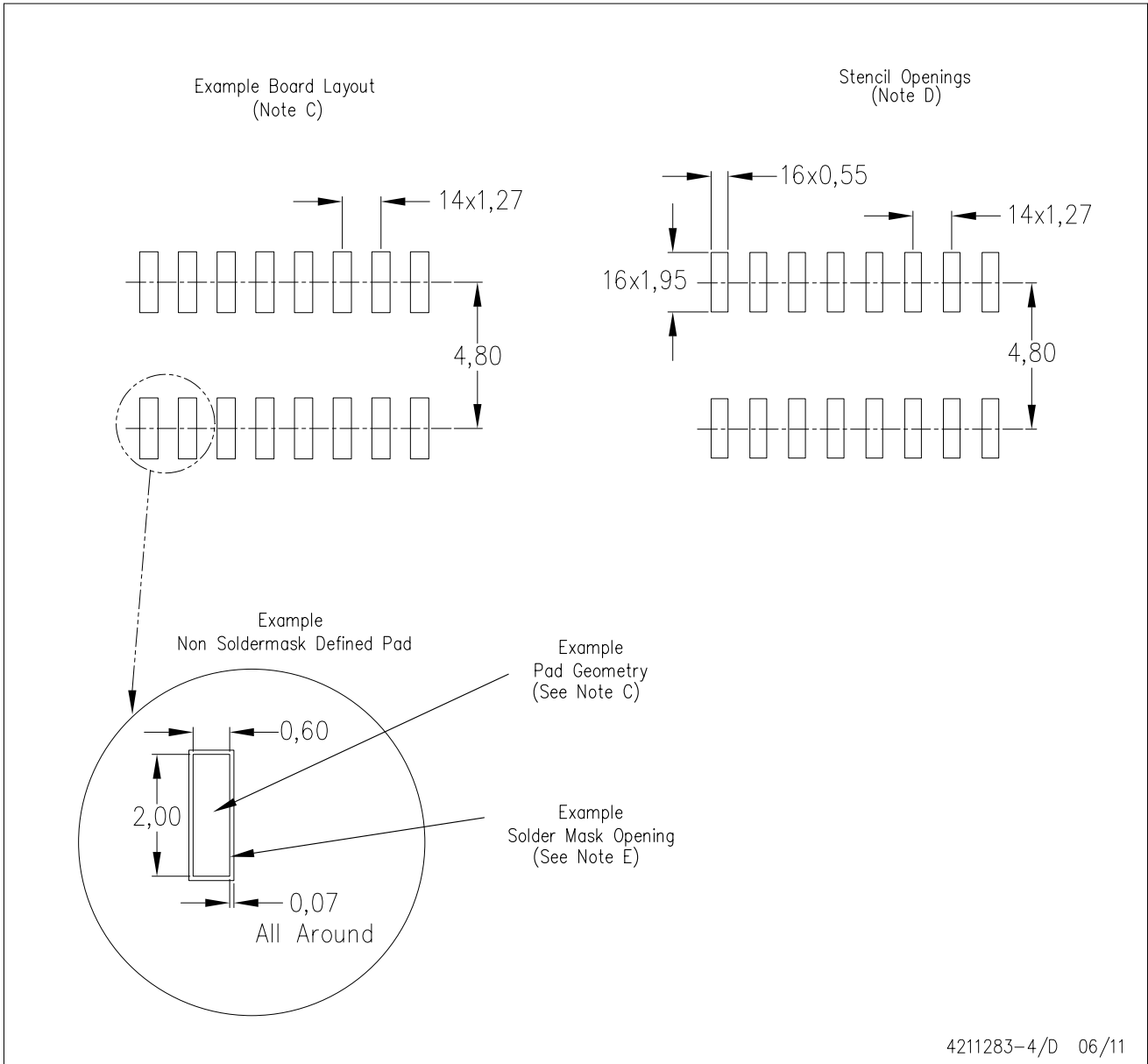
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

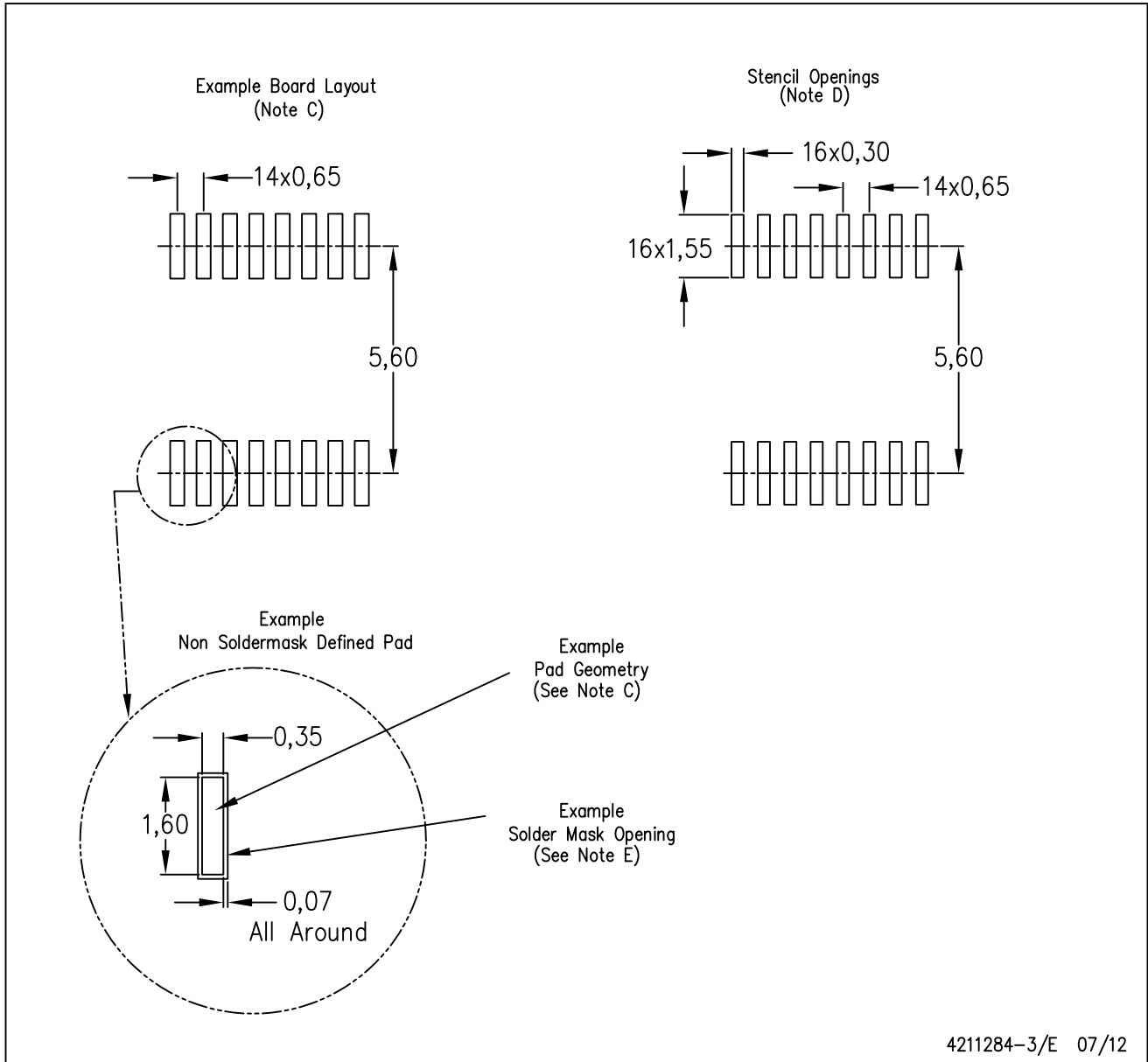


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G16)

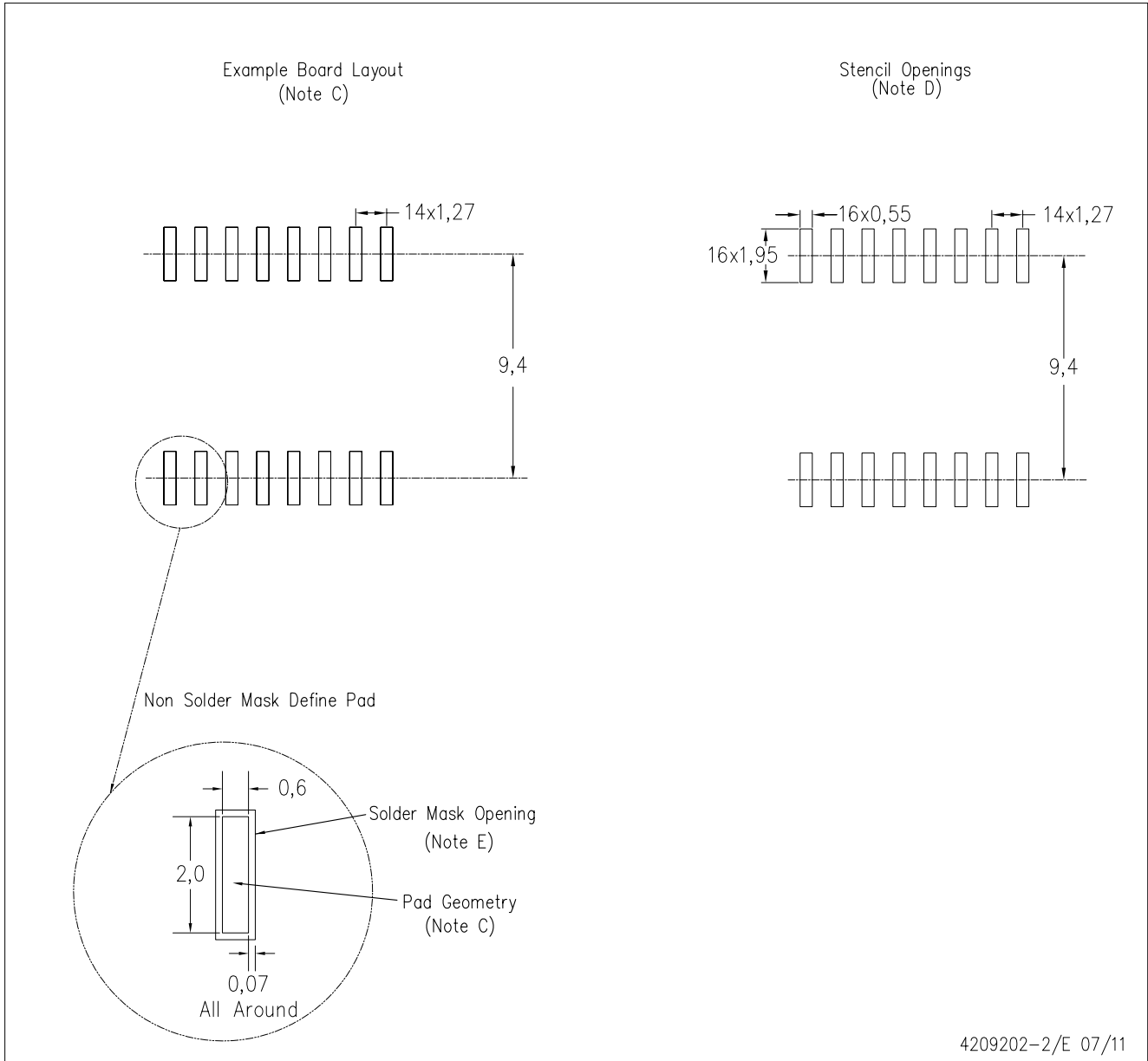
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4209202-2/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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