Industrial Analog Current/Voltage OUTPUT DRIVER

Check for Samples: XTR300

FEATURES

- **USER-SELECTABLE: Voltage or Current Output**
- **+40V SUPPLY VOLTAGE**
- **V_{OUT}: ±10V (up to ±17.5V at ±20V supply)**
- **I_{OUT}: ±20mA (linear up to ±24mA)**
- **SHORT- OR OPEN-CIRCUIT FAULT INDICATOR PIN**
- **NO CURRENT SHUNT REQUIRED**
- **OUTPUT DISABLE FOR SINGLE INPUT MODE**
- **THERMAL PROTECTION**
- **OVERCURRENT PROTECTION**
- **SEPARATE DRIVER AND RECEIVER CHANNELS**
- **DESIGNED FOR TESTABILITY**

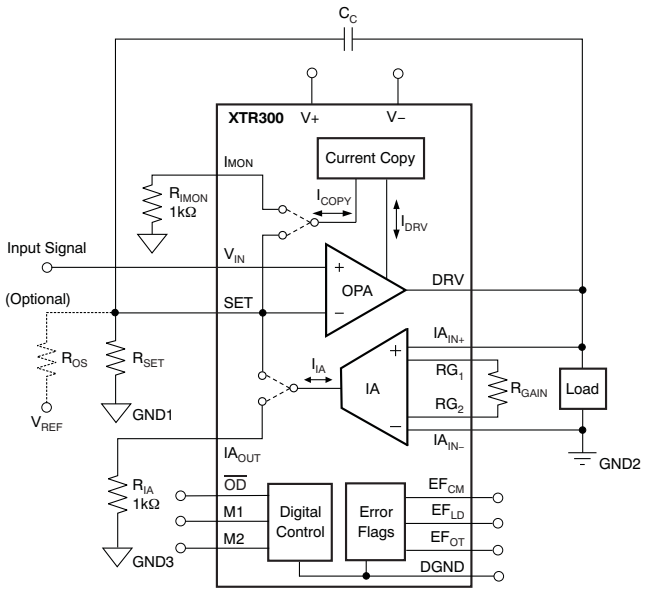


Figure 1. XTR300 Basic Diagram

APPLICATIONS

- **PLC OUTPUT PROGRAMMABLE DRIVER**
- **INDUSTRIAL CROSS-CONNECTORS**
- **INDUSTRIAL HIGH-VOLTAGE I/O**
- **3-WIRE-SENSOR CURRENT OR VOLTAGE OUTPUT**
- **±10V 2- AND 4-WIRE VOLTAGE OUTPUT**

U.S. Patent Nos. 7,427,898, 7,425,848, and 7,449,873

Other Patents Pending

DESCRIPTION

The XTR300 is a complete output driver for industrial and process control applications. The output can be configured as current or voltage by the digital I/V select pin. No external shunt resistor is required. Only external gain-setting resistors and a loop compensation capacitor are required.

The separate driver and receiver channels provide flexibility. The Instrumentation Amplifier (IA) can be used for remote voltage sense or as a high-voltage, high-impedance measurement channel. In voltage output mode, a copy of the output current is provided, allowing calculation of load resistance.

The digital output selection capability, together with the error flags and monitor pins, make remote configuration and troubleshooting possible. Fault conditions on the output and on the IA input as well as over-temperature conditions are indicated by the error flags. The monitoring pins provide continuous feedback about load power or impedance. For additional protection, the maximum output current is limited and thermal protection is provided.

The XTR300 is specified over the −40°C to +85°C industrial temperature range and for supply voltages up to 40V.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
XTR300	QFN-20 (5mm x 5mm)	RGW	XTR300

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	XTR300	UNIT
Supply Voltage, V_{VSP}	+44	V
Signal Input Terminals:		
Voltage(2)	(V−) − 0.5 to (V+) + 0.5	V
Current(2)	±25	mA
DGND	±25	mA
Output Short-Circuit(3)	Continuous	
Operating Temperature	–55 to +125	°C
Storage Temperature	–55 to +125	°C
Junction Temperature	+150	°C
Electrostatic Discharge Ratings:		
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited. DRV pin allows a peak current of 50mA. See the *Output Protection* section in Applications Information.
(3) See the *Driver Output Disable* section in Applications Information for thermal protection.

ELECTRICAL CHARACTERISTICS: VOLTAGE OUTPUT MODE

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_S = ±20V, R_{LOAD} = 800Ω, R_{SET} = 2kΩ, R_{OS} = 2kΩ, V_{REF} = 4V, R_{GAIN} = 10kΩ, Input Signal Span 0V to 4V, and C_C = 100pF, unless otherwise noted.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
OFFSET VOLTAGE						
Offset Voltage, RTI	V_{OS}			±0.4	±1.9	mV
vs Temperature	**dV_{OS}/dT**			**±1.6**	**±6**	**µV/°C**
vs Power Supply	PSRR	V_S = ±5V to ±22V		±0.2	±10	µV/V
INPUT VOLTAGE RANGE						
Nominal Setup for ±10V Output		See Figure 2				
Input Voltage for Linear Operation			(V−) + 3V		(V+) − 3V	V
NOISE						
Voltage Noise, f = 0.1Hz to 10Hz, RTI				3		μV_{PP}
Voltage Noise Density, f = 1kHz, RTI	e_n			40		$nV/\sqrt{Hz}$
OUTPUT						
Voltage Output Swing from Rail		**I_{DRV} ≤ 15mA**	**(V−) +3**		**(V+) − 3**	**V**
Gain Nonlinearity				±0.01	±0.1	%FS
vs Temperature				**±0.1**	**±1**	**ppm/°C**
Gain Error	I_B			±0.04	±0.1	%FS
vs Temperature				**±0.2**	**±1**	**ppm/°C**
Output Impedance, dV_{DRV}/dI_{DRV}				7		mΩ
Output Leakage Current While Output Disabled		**Pin $\overline{OD}$ = L**(1)		**30**		**nA**
Short-Circuit Current	**I_{SC}**		**±15**	**±20**	**±24**	**mA**
Capacitive Load Drive	C_{LOAD}	C_C = 10nF, R_C = 15(2)		1		µF
Rejection of Voltage Difference between GND1 and GND2, RTO				130		dB
FREQUENCY RESPONSE						
Bandwidth(3)	−3dB	G = 5		300		kHz
Slew Rate(2)	SR			1		V/µs
	SR	C_C = 10nF, C_L = 1µF, R_C = 15Ω		0.015		V/µs
Settling Time(2)(4), 0.1%, Small Signal		V_{DRV} = ±1V		8		µs
Overload Recovery Time		50% Overdrive		12		µs

(1) Output leakage includes input bias current of INA.
(2) Refer to *Driving Capacitive Loads* section in Applications Information.
(3) Small signal with no capacitive load.
(4) 8µs plus number of chopping periods. See Applications Information, *Internal Current Sources and Settling Time* section.

ELECTRICAL CHARACTERISTICS: CURRENT OUTPUT MODE

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_S = ±20V, R_{LOAD} = 800Ω, R_{SET} = 2kΩ, R_{OS} = 2kΩ, V_{REF} = 4V, Input Signal Span 0 to 4V, and C_C = 100pF, unless otherwise noted.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	Output Current < 1µA		±0.4	±1.8	mV
vs Temperature	**dV_{OS}/dT**			**±1.5**	**±6**	**µV/°C**
vs Power Supply	PSRR	V_S = ±5V to ±22V		±0.2	±10	µV/V
INPUT VOLTAGE RANGE						
Nominal Setup for ±20mA Output		See Figure 3				
Maximum Input Voltage for Linear Operation			(V−) + 3V		(V+) − 3V	V
NOISE						
Voltage Noise, f = 0.1Hz to 10Hz, RTI				3		μV_{PP}
Voltage Noise Density, f = 1kHz, RTI	e_n			33		$nV/\sqrt{Hz}$
OUTPUT						
Compliance Voltage Swing from Rail		**I_{DRV} = ±24mA**	**(V−) +3**		**(V+) − 3**	**V**
Output Conductance (dI_{DRV}/dV_{DRV})		dV_{DRV} = ±15V, dI_{DRV} = ±24mA		0.7		µA/V
Transconductance		See Transfer Function in Figure 3				
Gain Error		I_{DRV} = ±24mA		±0.04	±0.12	%FS
vs Temperature		**I_{DRV} = ±24mA**		**±3.6**	**±10**	**ppm/°C**
Linearity Error	I_B	I_{DRV} = ±24mA		±0.01	±0.1	%FS
vs Temperature		**I_{DRV} = ±24mA**		**±1.5**	**±6**	**ppm/°C**
Output Leakage Current While Output Disabled		**Pin $\overline{OD}$ = L**		**0.6**		**nA**
Short-Circuit Current	**I_{SC}**		**±24.5**	**±32**	**±38.5**	**mA**
Capacitive Load Drive(1)(2)	C_{LOAD}			1		µF
FREQUENCY RESPONSE						
Bandwidth	−3dB			160		kHz
Slew Rate(2)	SR			1.3		mA/µs
Settling Time(2)(3), 0.1%, Small Signal		I_{DRV} = ±2mA		8		µs
Overload Recovery Time		C_{LOAD} = 0, 50% Overdrive		1		µs

(1) Refer to *Driving Capacitive Loads* section in Applications Information.
(2) With capacitive load, the slew rate can be limited by the short circuit current and the load error flag can trigger during slewing.
(3) 8µs plus number of chopping periods. See Applications Information, *Internal Current Sources and Settling Time* section.

ELECTRICAL CHARACTERISTICS: OPERATIONAL AMPLIFIER (OPA)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_S = ±20V, and R_{LOAD} = 800Ω, unless otherwise noted.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
OFFSET VOLTAGE						
Offset Voltage, RTI	V_{OS}	I_{DRV} = 0A		±0.4	±1.8	mV
Drift	**dV_{OS}/dT**			**±1.5**		**µV/°C**
vs Power Supply	PSRR	V_S = ±5V to ±22V		±0.2	±5	µV/V
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V−) + 3		(V+) − 3	V
Common-Mode Rejection Ratio	CMRR	(V−) + 3V < V_{CM} < (V+) − 3V	100	126		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B			±20	±35	nA
Input Offset Current	I_{OS}			±0.3	±10	nA
INPUT IMPEDANCE						
Differential				10^8 || 5		Ω || pF
Common-Mode				10^8 || 5		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V−) + 3V < V_{DRV} < (V+) − 3V , I_{DRV} = ±24mA	100	126		dB
OUTPUT						
Voltage Output Swing from Rail		I_{DRV} = ±24mA	(V−) + 3		(V+) − 3	V
Short-Circuit Current	I_{LIMIT}	M2 = High	±25.5	±32	±38.5	mA
	I_{LIMIT}	M2 = Low	±16	±20	±24	mA
Output Leakage Current While Output Disabled	I_{LEAK_DRV}	Pin $\overline{OD}$ = L		10		pA
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = 1		2		MHz
Slew Rate	SR			1		V/µs

ELECTRICAL CHARACTERISTICS: INSTRUMENTATION AMPLIFIER (IA)

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C, V_S = ±20V, R_{IA} = 2kΩ, and R_{GAIN} = 2kΩ, unless otherwise noted. See Figure 4.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
OFFSET VOLTAGE						
Offset Voltage, RTI	V_{OS}	I_{DRV} = 0A		±0.7	±2.7	mV
vs Temperature	**dV_{OS}/dT**			**±2.4**	**±10**	**µV/°C**
vs Power Supply	PSRR	V_S = ±5V to ±22V		±0.8	±10	µV/V
INPUT VOLTAGE RANGE						
Input Voltage Range	V_{CM}		(V−) + 3		(V+) − 3	V
Common-Mode Rejection Ratio	CMRR	RTI	100	130		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B			±20	±35	nA
Input Offset Current	I_{OS}			±1	±10	nA
INPUT IMPEDANCE						
Differential				10^5 || 5		Ω || pF
Common-Mode				10^5 || 5		Ω || pF
TRANSCONDUCTANCE (Gain)		$IA_{OUT} = 2 (IA_{IN+} - IA_{IN-})/R_{GAIN}$				
Transconductance Error		IA_{OUT} = ±2.4mA, (V−) + 3V < V_{IAOUT} < (V+) − 3V		±0.04	±0.1	%/FS
vs Temperature				**±0.2**		**ppm/°C**
Linearity Error		(V−) + 3V < V_{IAOUT} < (V+) − 3V		±0.01	±0.1	%FS
Input Bias Current to G1, G2				±20		nA
Input Offset Current to G1, G2 (1)				±1		nA
OUTPUT						
Output Swing to the Rail		IA_{OUT} = ±2.4mA	(V−) + 3		(V+) − 3	V
Output Impedance		IA_{OUT} = ±2.4mA		600		mΩ
Short-Circuit Current	I_{LIMIT}	M2 = High		±7.2		mA
	I_{LIMIT}	M2 = Low		±4.5		mA
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = 1, R_{GAIN} = 10kΩ, R_{IA} = 5kΩ		1		MHz
Slew Rate	SR	G = 1, R_{GAIN} = 10kΩ, R_{IA} = 5kΩ		1		V/µs
Settling Time (2), 0.1%		IA_{OUT} = ±40µA, R_{GAIN} = 10kΩ, R_{IA} = 5kΩ, C_L = 100pF		6		µs
Overload Recovery Time, 50%		R_{GAIN} = 10kΩ, R_{IA} = 15kΩ, C_L = 100pF		10		µs

(1) See Typical Characteristics curve (Figure 7).
(2) 6µs plus number of chopping periods. See Applications Information, *Internal Current Sources and Settling Time section*.

ELECTRICAL CHARACTERISTICS: CURRENT MONITOR

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C and V_S = ±20V, unless otherwise noted. See Figure 4.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
OUTPUT						
Offset Current	I_{OS}	I_{DRV} = 0A		±30	±100	nA
Drift	**dI_{OS}/dT**			**±0.05**		**nA/°C**
vs Power Supply	PSRR	V_S = ±5V to ±22V		±0.1	±10	nA/V
Monitor Output Swing to the Rail		I_{MON} = ±2.4mA	(V−) + 3		(V+) − 3	V
Monitor Output Impedance		I_{MON} = ±2.4mA		200		MΩ
MONITOR CURRENT GAIN		$I_{MON} = I_{DRV}/10$				
Current Gain Error		I_{DRV} = ±24mA		±0.04	±0.12	%FS
vs Temperature		**I_{DRV} = ±24mA**		**±3.6**		**ppm/°C**
Linearity Error		I_{DRV} = ±24mA		±0.01	±0.1	%FS
vs Temperature		**I_{DRV} = ±24mA**		**±1.5**		**ppm/°C**

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range: **T_A = –40°C to +85°C.**
All specifications at T_A = +25°C and V_S = ±20V, unless otherwise noted. See Figure 4.

PARAMETER		CONDITIONS	XTR300 MIN	XTR300 TYP	XTR300 MAX	UNIT
POWER SUPPLY						
Specified Voltage Range	V_S		±5		±20	V
Operating Voltage Range			±5		±22	V
Quiescent Current	I_Q	$I_{DRV} = IA_{OUT}$ = 0A		1.8	2.3	mA
Over Temperature					**2.8**	**mA**
TEMPERATURE RANGE						
Specified Temperature Range			−40		+85	°C
Operating Temperature Range			−55		+125(1)	°C
Storage Temperature Range			−55		+125	°C
Thermal Resistance						
Junction-to-Case	θ_{JC}			15.2		°C/W
Junction-to-Ambient	θ_{JA}			38		°C/W
THERMAL FLAG (EF_{OT}) Output						
Alarm (EF_{OT} pin LOW)				140		°C
Return to Normal Operation (EF_{OT} pin HIGH)				125		°C
DIGITAL INPUTS (M1, M2, $\overline{OD}$)						
V_{IL} Low-Level Input Voltage				≤ 0.8		V
V_{IH} High-Level Input Voltage				> 1.4		V
Input Current				±1		µA
DIGITAL OUTPUTS (EF_{LD}, EF_{CM}, EF_{OT})						
I_{OH} High-Level Leakage Current (Open-Drain)				−1.2		µA
V_{OL} Low-Level Output Voltage		I_{OL} = 5mA		0.8		V
V_{OL} Low-Level Output Voltage		I_{OL} = 2.8mA		0.4		V
DIGITAL GROUND PIN		(V−) ≤ DGND ≤ (V+) − 7V				
Current Input		M1 = M2 = L, $\overline{OD}$ = H, All Digital Outputs H		−25		µA

(1) EF_{OT} not connected with $\overline{OD}$.

FUNCTIONAL BLOCK DIAGRAMS

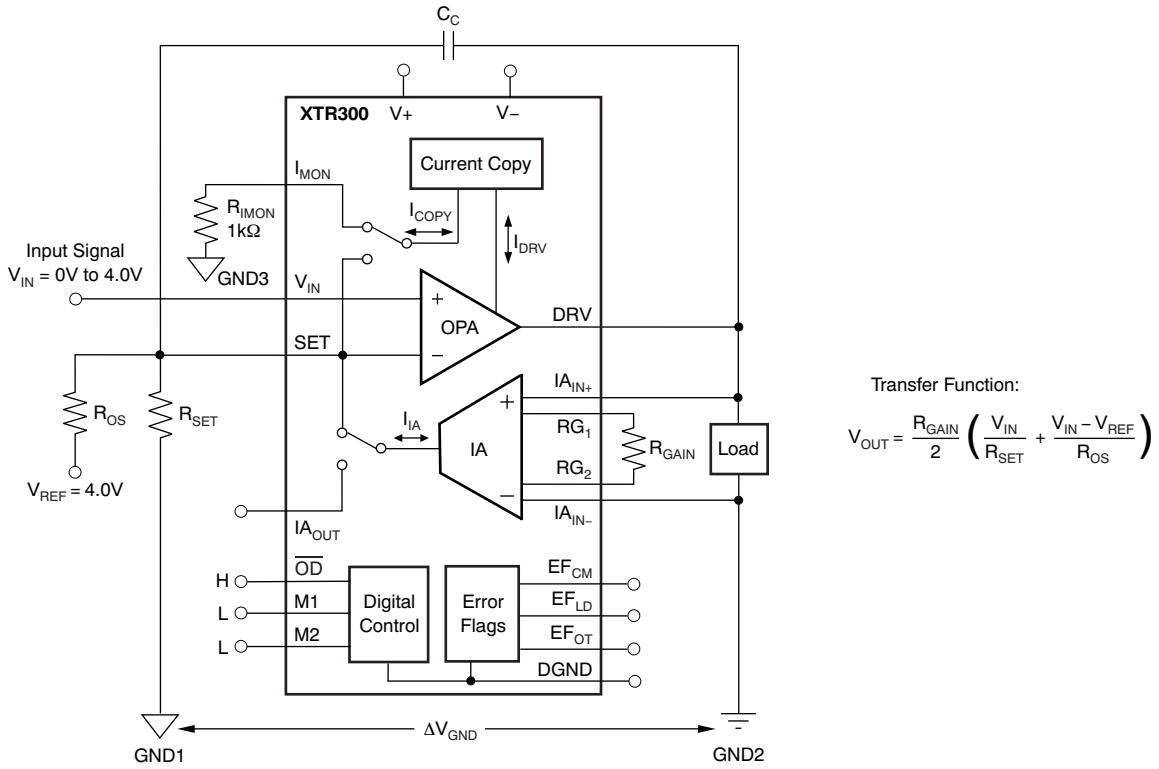


Figure 2. Standard Circuit for Voltage Output Mode

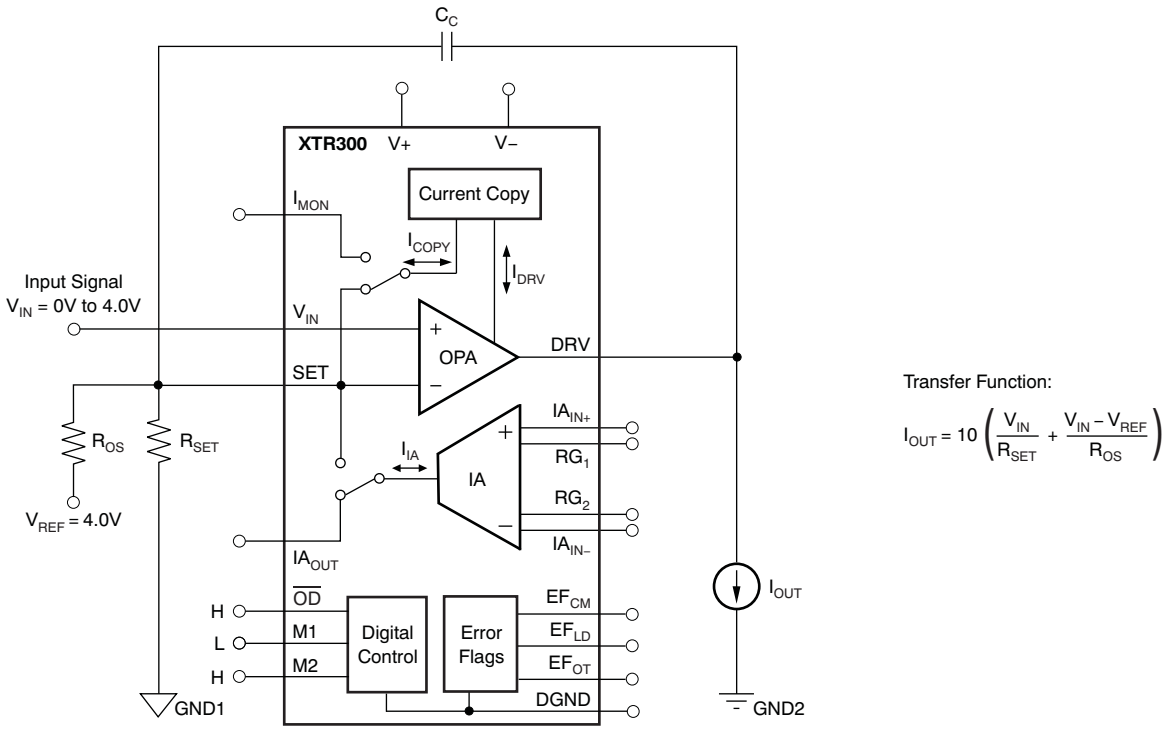


Figure 3. Standard Circuit for Current Output Mode

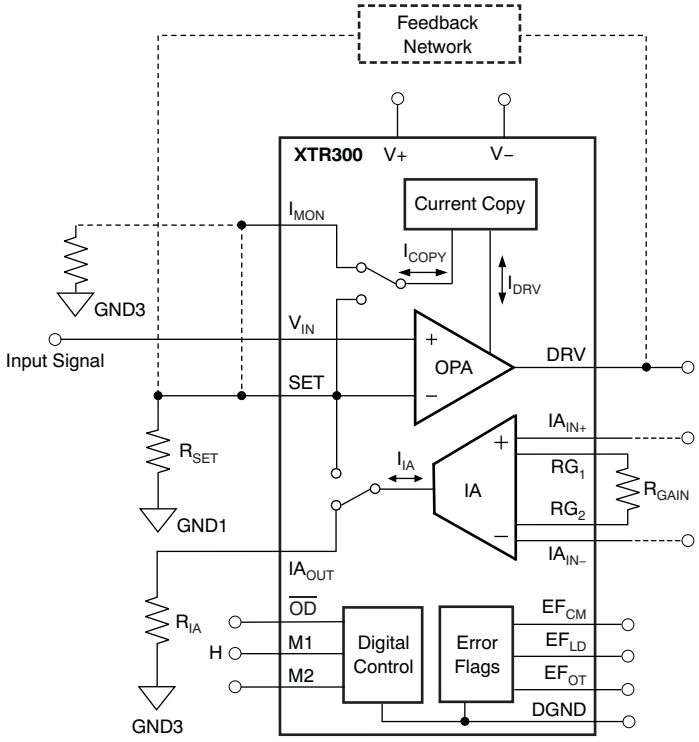
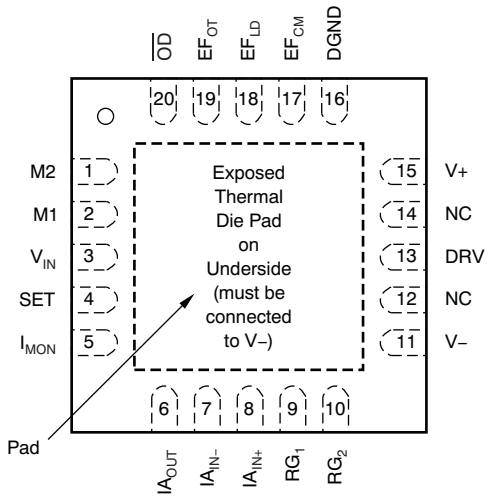


Figure 4. Standard Circuit for Externally Configured Mode

PIN CONFIGURATIONS

RGW PACKAGE
QFN-20
(TOP VIEW)



PIN ASSIGNMENTS

PIN NO.	NAME	FUNCTION
1	M2	Mode Input
2	M1	Mode Input
3	V_{IN}	Noninverting Signal Input
4	SET	Input for Gain Setting; Inverting Input
5	I_{MON}	Current Monitor Output
6	IA_{OUT}	Instrumentation Amplifier Signal Output
7	IA_{IN-}	Instrumentation Amplifier Inverting Input
8	IA_{IN+}	Instrumentation Amplifier Noninverting Input
9	RG1	Instrumentation Amplifier Gain Resistor
10	RG2	Instrumentation Amplifier Gain Resistor
11	V–	Negative Power Supply
12	NC	No Internal Connection
13	DRV	Operational Amplifier Output
14	NC	No Internal Connection
15	V+	Positive Power Supply
16	DGND	Ground for Digital I/O
17	EF_{CM}	Error Flag for Common-Mode Over-Range, Active Low
18	EF_{LD}	Error Flag for Load Error, Active Low
19	EF_{OT}	Error Flag for Over Temperature, Active Low
20	$\overline{OD}$	Output Disable, Disabled Low
Pad	Exposed Pad	Exposed thermal pad must be connected to V–

TYPICAL CHARACTERISTICS

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

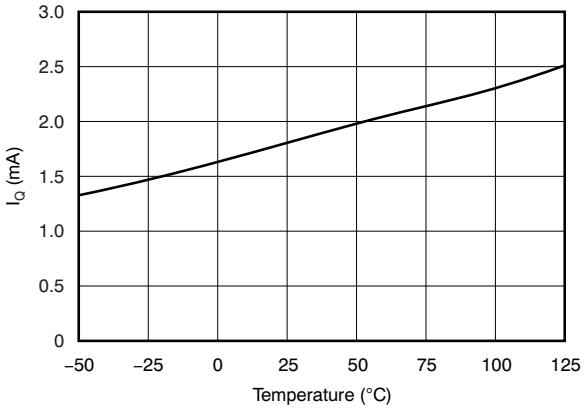


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

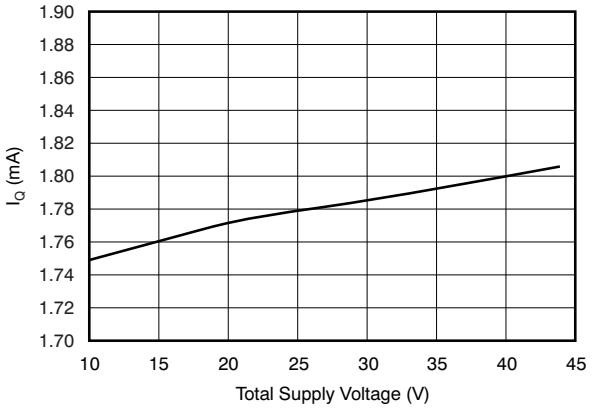


Figure 6.

INPUT BIAS CURRENT vs TEMPERATURE (V_{IN}, SET, IA_{IN+}, $IA_{IN–}$, RG1, RG2)

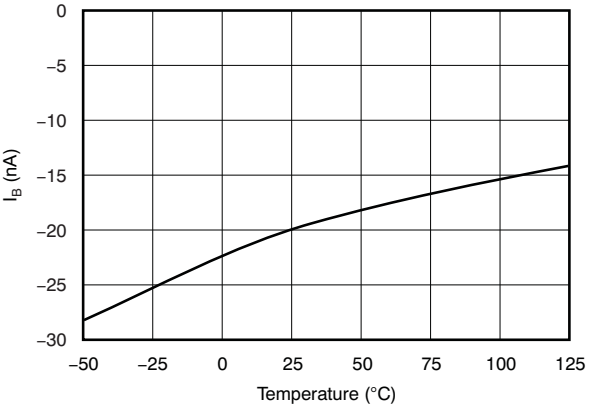


Figure 7.

OPA OUTPUT SWING TO RAIL vs TEMPERATURE

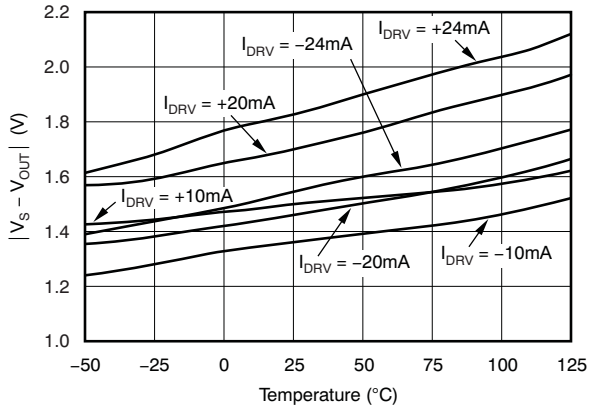


Figure 8.

OPA GAIN AND PHASE vs FREQUENCY

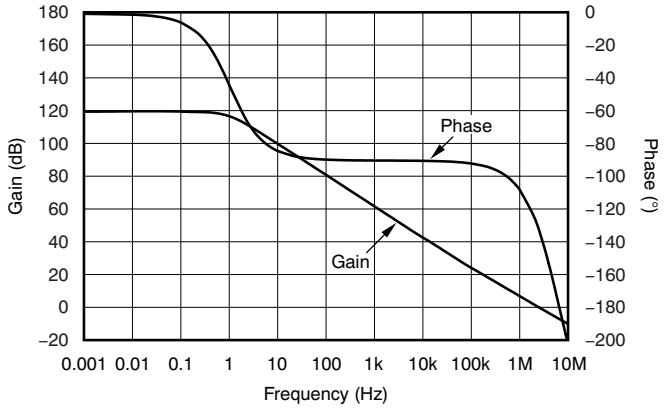


Figure 9.

IA GAIN AND PHASE vs FREQUENCY

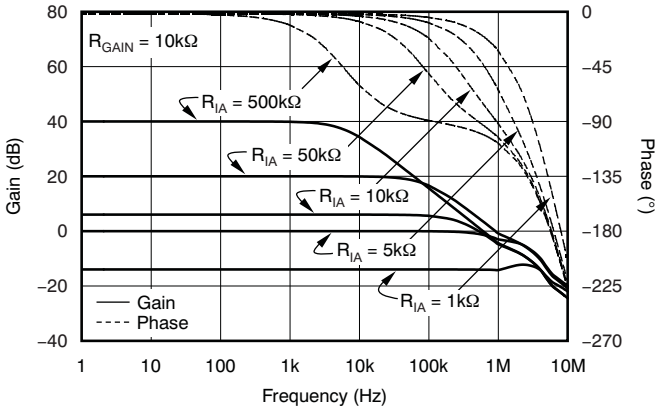


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

OPA CMRR AND PSRR vs FREQUENCY

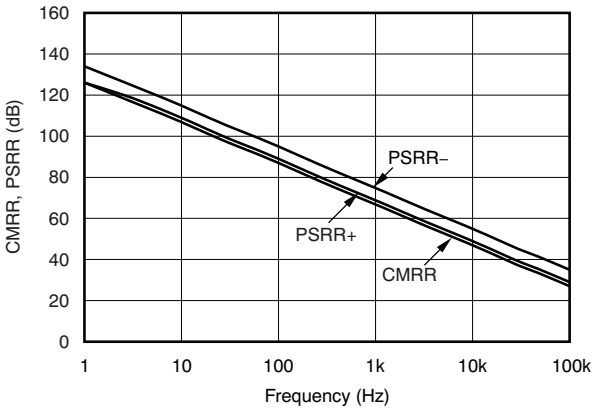


Figure 11.

IA CMRR AND PSRR vs FREQUENCY

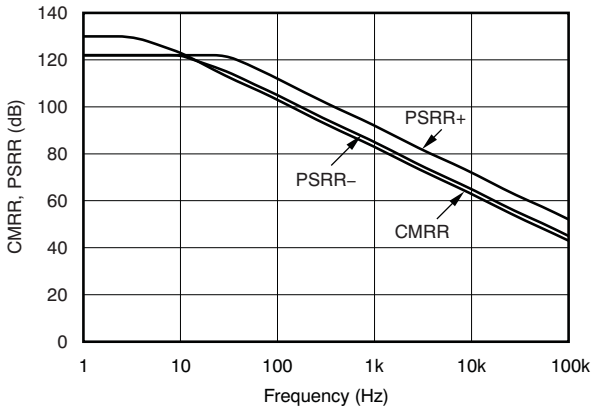


Figure 12.

SMALL−SIGNAL STEP RESPONSE CURRENT MODE

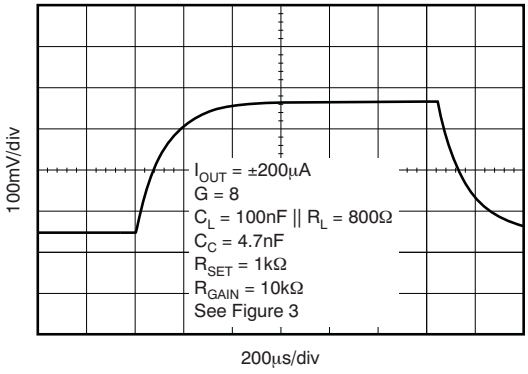


Figure 13.

LARGE−SIGNAL STEP RESPONSE CURRENT MODE

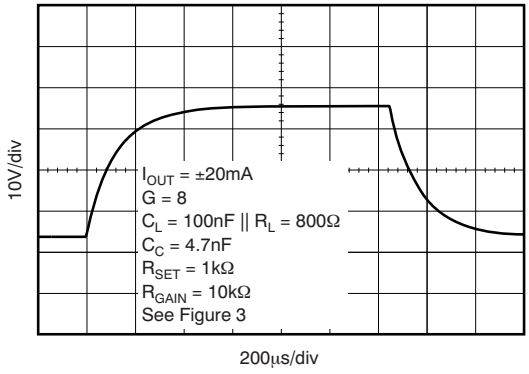


Figure 14.

SMALL−SIGNAL STEP RESPONSE VOLTAGE MODE

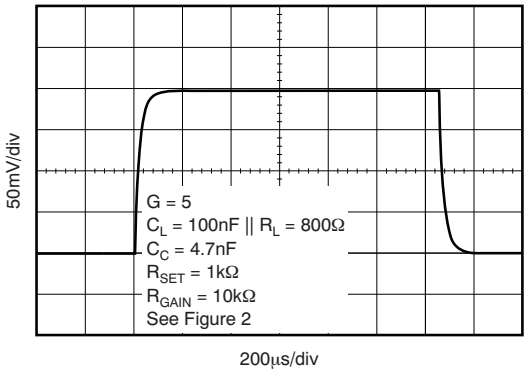


Figure 15.

LARGE−SIGNAL STEP RESPONSE VOLTAGE MODE

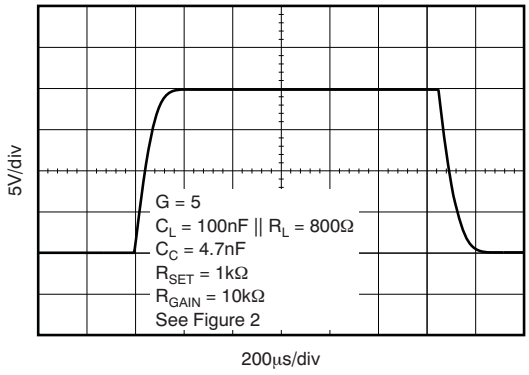


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

INPUT−REFERRED NOISE SPECTRUM VOLTAGE OUTPUT MODE

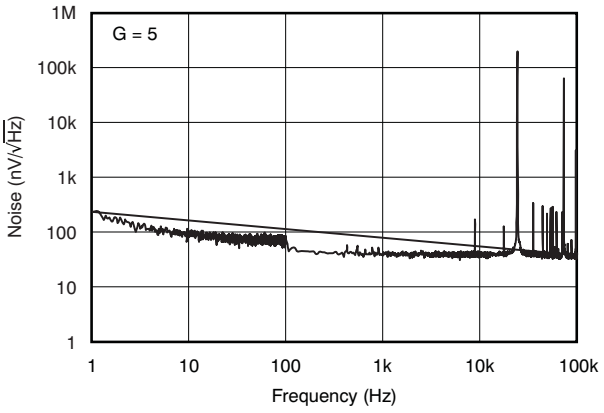


Figure 17.

INPUT−REFERRED 0.1Hz to 10Hz NOISE VOLTAGE OUTPUT MODE

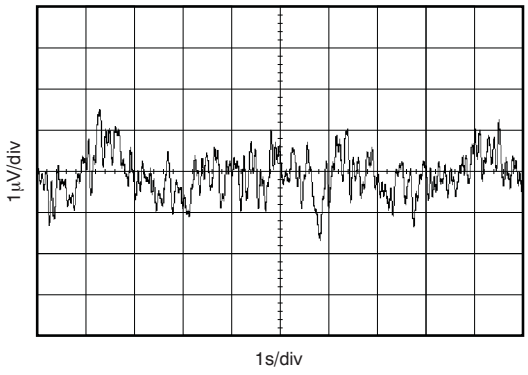


Figure 18.

INPUT−REFERRED NOISE SPECTRUM CURRENT OUTPUT MODE

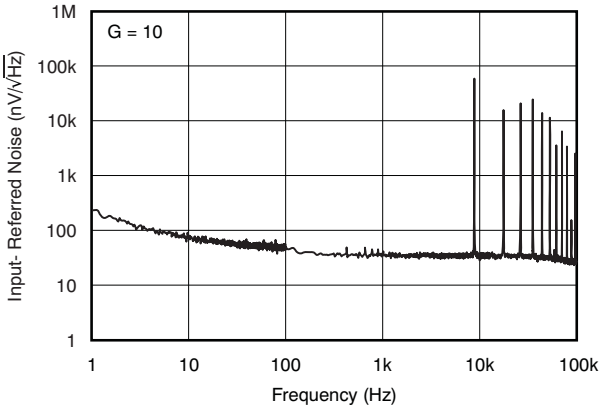


Figure 19.

INPUT−REFERRED 0.1Hz to 10Hz NOISE CURRENT OUTPUT MODE

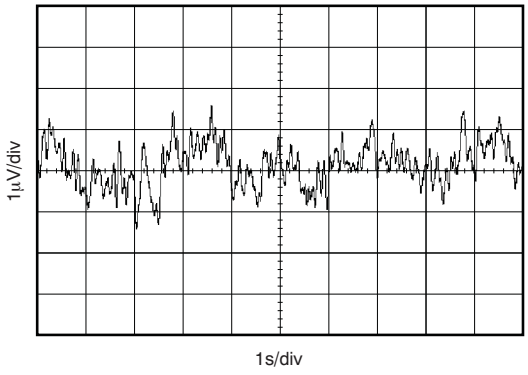


Figure 20.

IA INPUT−REFERRED NOISE SPECTRUM

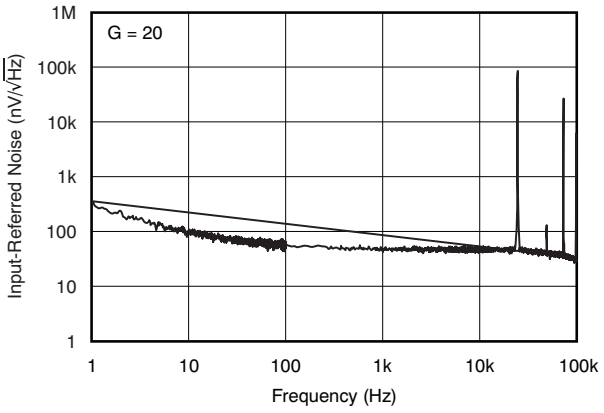


Figure 21.

IA INPUT−REFERRED 0.1Hz to 10Hz NOISE

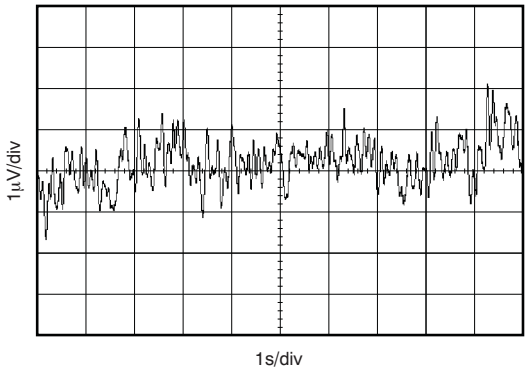


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

OPA OFFSET VOLTAGE DISTRIBUTION

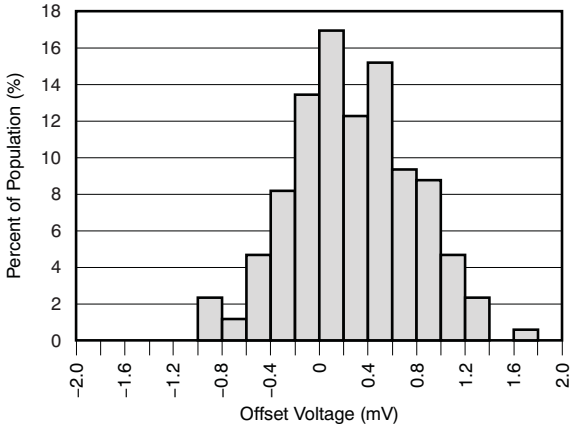


Figure 23.

IA OFFSET VOLTAGE DISTRIBUTION

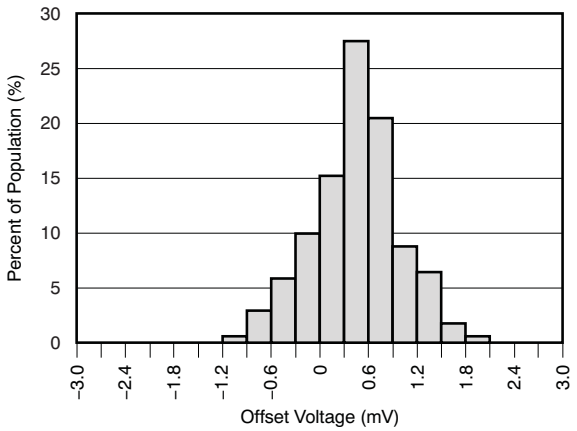


Figure 24.

OPA OFFSET VOLTAGE DRIFT DISTRIBUTION

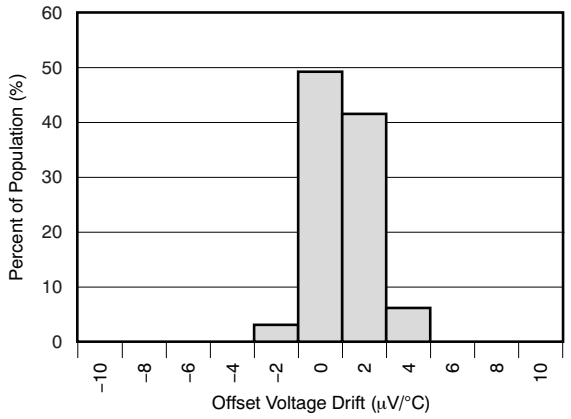


Figure 25.

IA OFFSET VOLTAGE DRIFT DISTRIBUTION

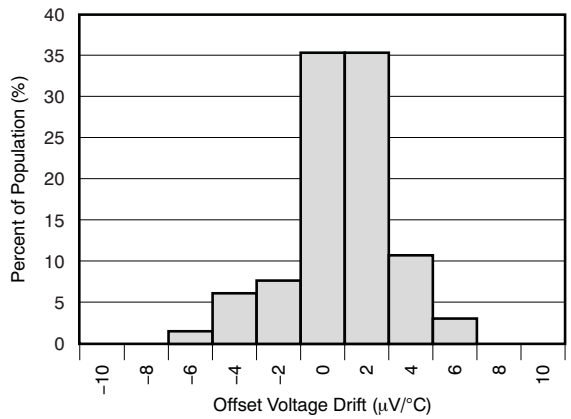


Figure 26.

VOLTAGE MODE GAIN ERROR DISTRIBUTION

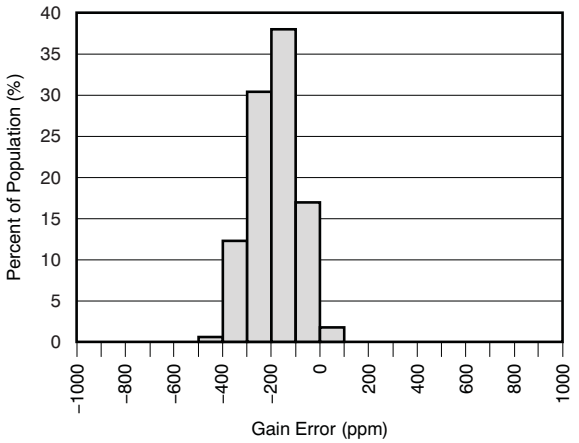


Figure 27.

CURRENT MODE GAIN ERROR DISTRIBUTION

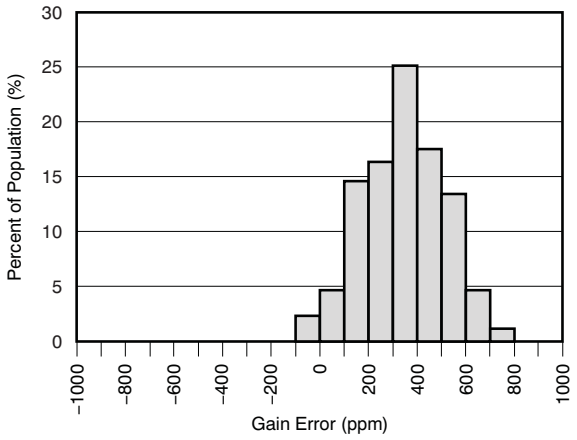


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

VOLTAGE MODE NONLINEARITY DISTRIBUTION

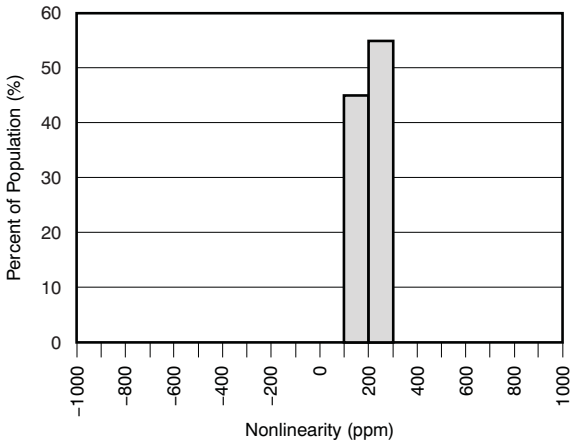


Figure 29.

CURRENT MODE NONLINEARITY DISTRIBUTION

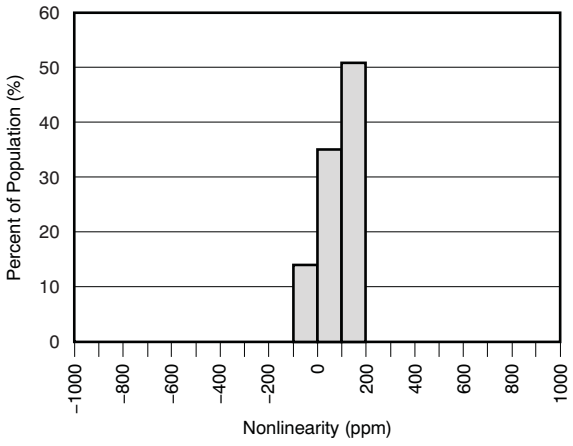


Figure 30.

VOLTAGE MODE GAIN ERROR DRIFT DISTRIBUTION

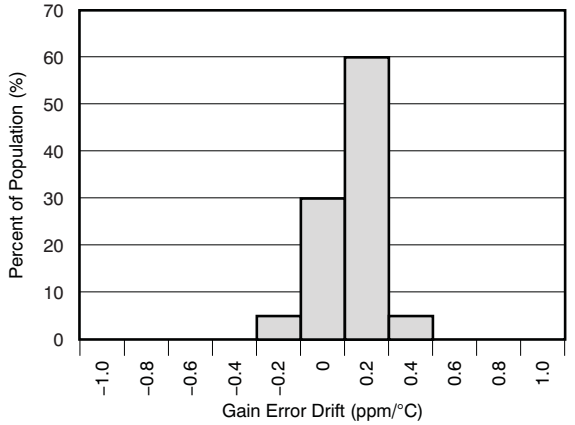


Figure 31.

CURRENT MODE GAIN ERROR DRIFT DISTRIBUTION

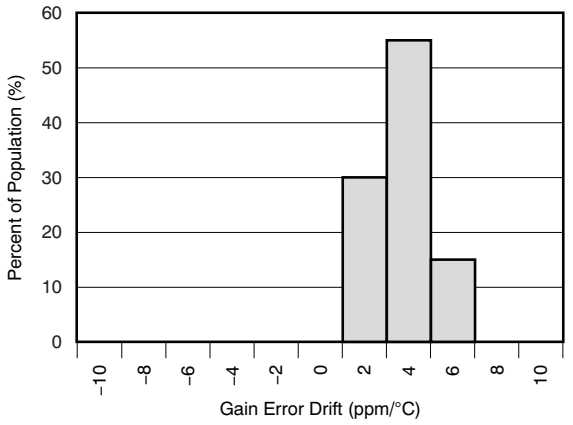


Figure 32.

VOLTAGE MODE NONLINEARITY DRIFT DISTRIBUTION

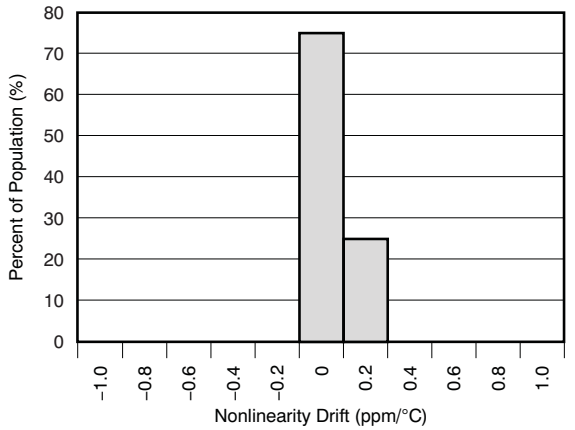


Figure 33.

CURRENT MODE NONLINEARITY DRIFT DISTRIBUTION

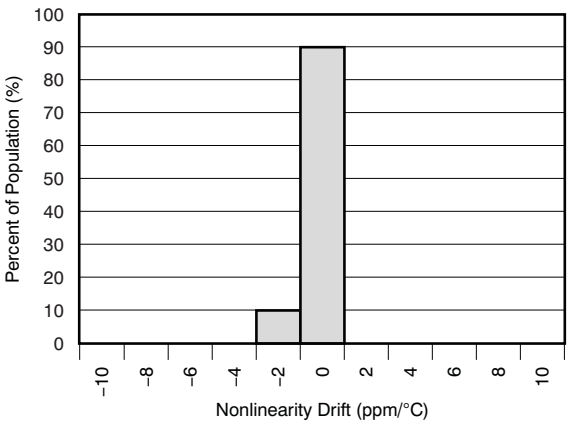


Figure 34.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V+ = ±20V, unless otherwise noted.

POSITIVE CURRENT LIMIT vs TEMPERATURE

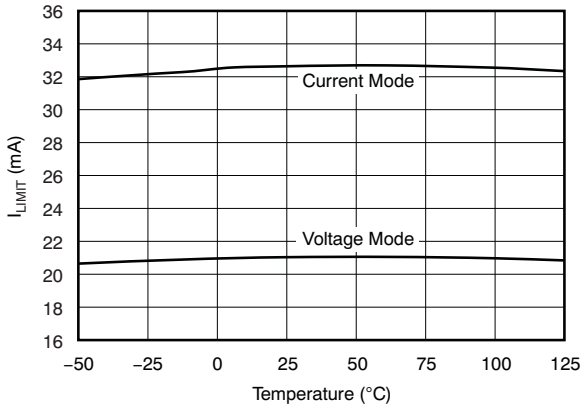


Figure 35.

NEGATIVE CURRENT LIMIT vs TEMPERATURE

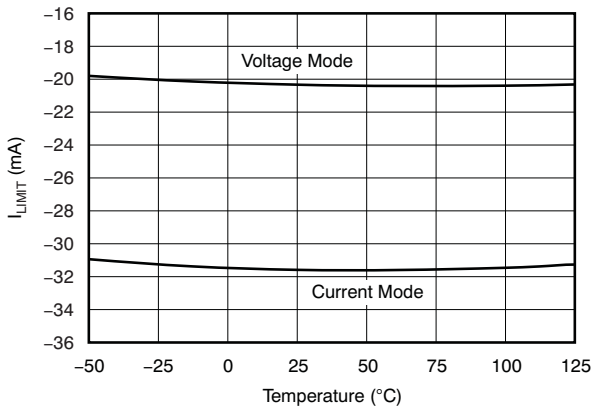


Figure 36.

NONLINEARITY vs OUTPUT CURRENT (±24mA End Point Calibration)

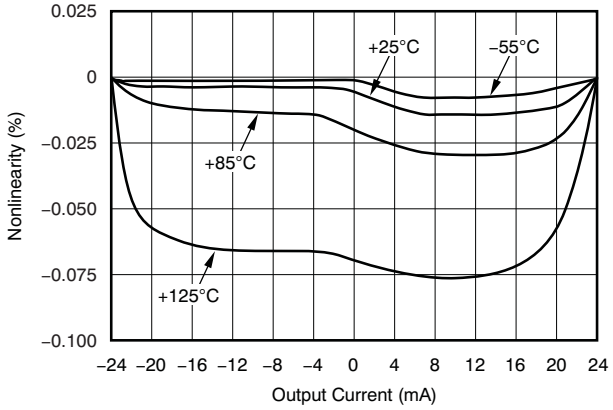


Figure 37.

NONLINEARITY vs OUTPUT CURRENT (±20mA End Point Calibration)

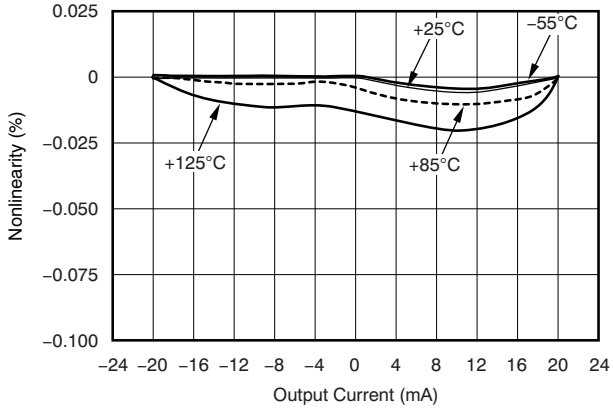
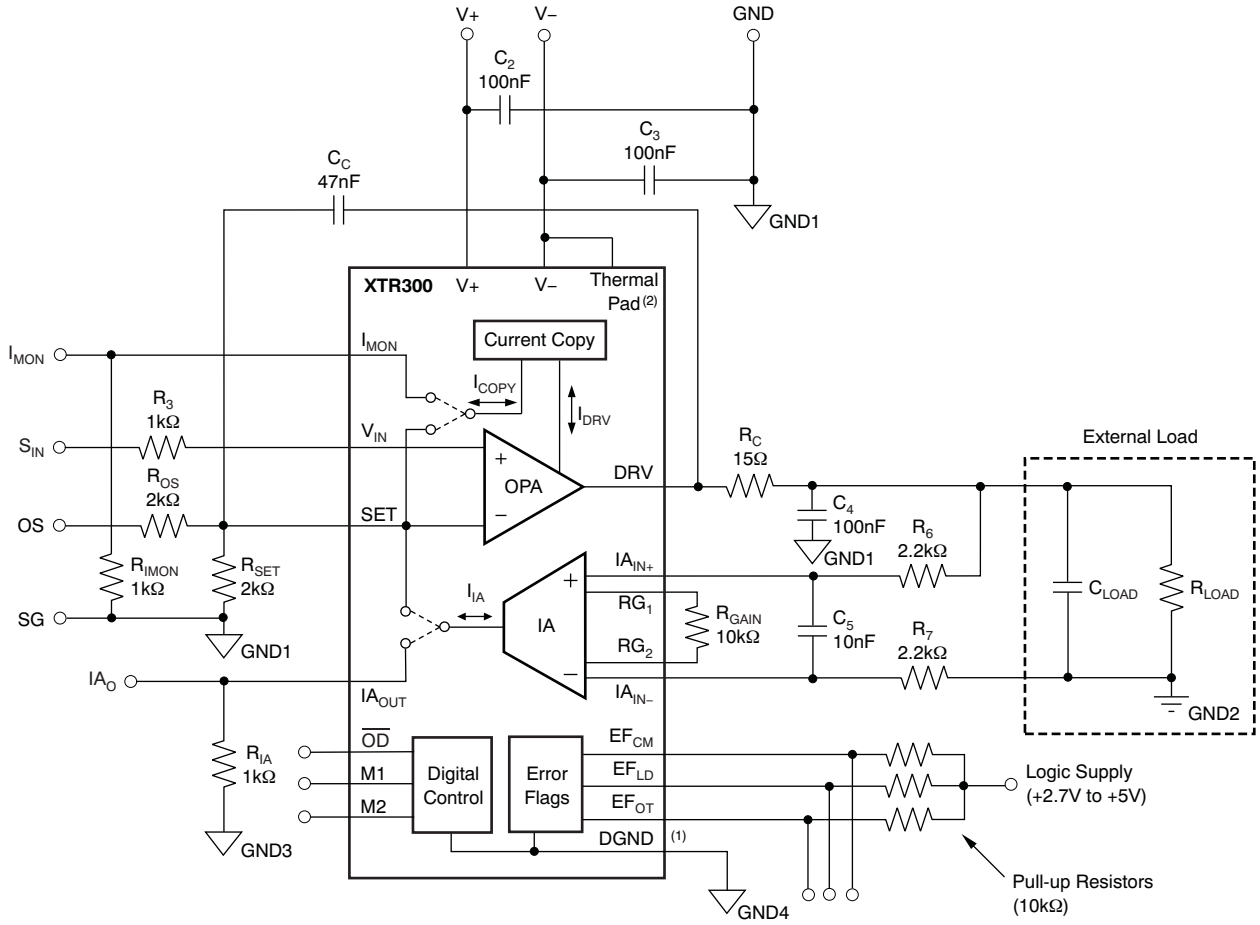


Figure 38.

APPLICATION INFORMATION



(1) See the Electrical Characteristics and *Digital Input and Output* section for operating limits of DGND.

(2) Connect thermal pad to V−.

Figure 39. Standard Circuit Configuration

The following information should be considered during XTR300 circuit configuration:

- Recommended bypassing: 100nF or more for supply bypassing at each supply.
- R_{IMON} can be in the kΩ-range or short-circuited if not used. Do not leave this current output unconnected—it would saturate the internal current source. The current at this I_{MON} output is $I_{DRV}/10$. Therefore, $V_{IMON} = R_{IMON} (I_{DRV}/10)$.
- R_3 is not required but can match R_{SET} (or $R_{SET}||R_{OS}$) to compensate for the bias current.
- R_{IA} can be short-circuited if not used. Do not leave this current output unconnected. R_{GAIN} is selected to 10kΩ to match the output of 10V with 20mA for the equal input signal.
- R_C ensures stability for unknown load conditions and limits the current into the internal protection diodes. C_4 helps protect the device. Over-voltage clamp diodes (standard 1N4002) might be necessary to protect the output.
- R_6, R_7, and C_5 protect the IA.
- R_{LOAD} and C_{LOAD} represent the load resistance and load capacitance.
- R_{SET} defines the transfer gain. It can be split to allow a signal offset and, therefore, allow a 5V single-supply digital-to-analog converter (DAC) to control a ±10V or ±20mA output signal.

The XTR300 can be used with asymmetric supply voltages; however, the minimum negative supply voltage should be equal to or more negative than −3V (typically −5V). This supply value ensures proper control of 0V and 0mA with wire resistance, ground offsets, and noise added to the output. For positive output signals, the current requirement from this negative voltage source is less than 5mA.

GND1 through GND4 must be selected to fulfill specified operating ranges. DGND must be in the range of (V−) ≤ DGND ≤ (V+) −7V.

Built on a robust high-voltage BiCMOS process, the XTR300 is designed to interface the 5V or 3V supply domain used for processors, signal converters, and amplifiers to the high-voltage and high-current industrial signal environment. It is specified for up to ±20V supply, but can also be powered asymmetrically (for example, +24V and −5V). It is designed to allow insertion of external circuit protection elements and drive large capacitive loads.

FUNCTIONAL FEATURES

The XTR300 provides two basic functional blocks: an instrumentation amplifier (IA) and a driver that is a unique operational amplifier (OPA) for current or voltage output. This combination represents an analog output stage which can be digitally configured to provide either current or voltage output to the same terminal pin. Alternatively, it can be configured for independent measurement channels.

Three open collector error signals are provided to indicate output related errors such as over-current or open-load (EF_{LD}) or exceeding the common-mode input range at the IA inputs (EF_{CM}). An over-temperature flag (EF_{OT}) can be used to control output disable to protect the circuit. The monitor outputs (I_{MON} and IA_{OUT}) and the error flags offer optimal testability during operation and configuration. The I_{MON} output represents the current flowing into the load in voltage output mode, while the IA_{OUT} represents the voltage across the connectors in current output mode. Both monitor outputs can be connected together when used in current or voltage output mode because the monitor signals are multiplexed accordingly.

VOLTAGE OUTPUT MODE

In voltage output mode (M1 and M2 are connected low or left unconnected), the feedback loop through the IA provides high impedance remote sensing of the voltage at the destination, compensating the resistance of a protection circuit, switches, wiring, and connector resistance. The output of the IA is a current that is proportional to the input voltage. This current is internally routed to the OPA summing junction through a multiplexer, as shown in Figure 40.

A 1:10 copy of the output current of the OPA can be monitored at the I_{MON} pin. This output current and the known output voltage can be used to calculate the load resistance or load power.

During an output short-circuit or an over-current condition the XTR300 output current is limited and EF_{LD} (load error, active low) flag is activated.

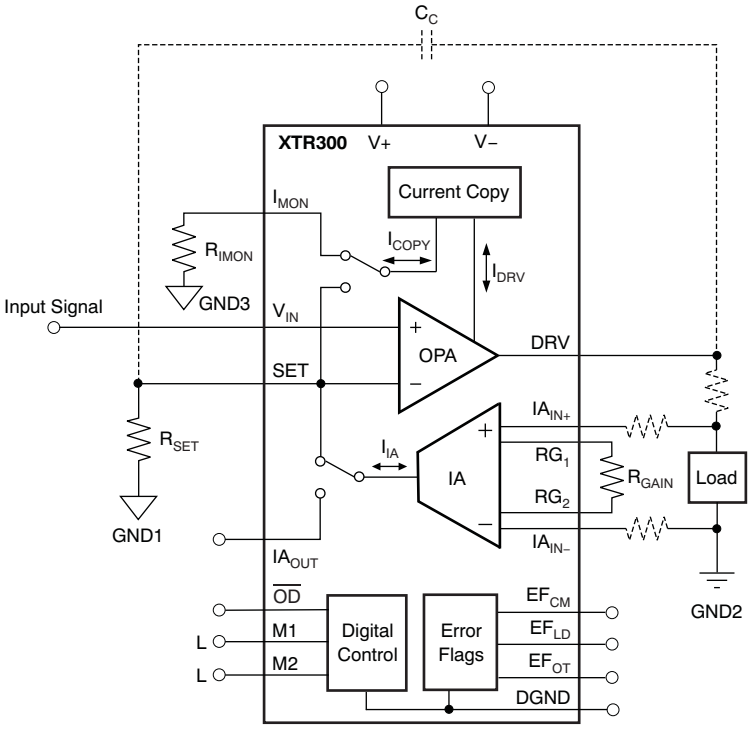


Figure 40. Simplified Voltage Output Mode Configuration

Applications not requiring the remote sense feature can use the OPA in stand-alone operation (M1 = high). In this case, the IA is available as a separate input channel.

The IA gain can be set by two resistors, R_{GAIN} and R_{SET}:

$$V_{OUT} = \frac{R_{GAIN}}{2R_{SET}} V_{IN} \quad (1)$$

or when adding an offset, V_{REF}, to get bidirectional output with a single-ended input:

$$V_{OUT} = \frac{R_{GAIN}}{2}\left(\frac{V_{IN}}{R_{SET}} + \frac{V_{IN} - V_{REF}}{R_{OS}}\right) \quad (2)$$

The R_{SET} resistor is also used in current output mode. Therefore, it is useful to define R_{SET} for the current mode, then set the ratio between current and voltage span with R_{GAIN}.

CURRENT OUTPUT MODE

The XTR300 does not require a shunt resistor for current control because it uses a precise current mirror arrangement.

In current output mode (M1 connected low, or left unconnected and M2 connected high) a precise copy of 1/10th of the output is internally routed back to the summing junction of the OPA through a multiplexer, closing the control loop for the output current.

The OPA driver can deliver more than ±24mA within a wide output voltage range. An open-output condition or high-impedance load that prevents the flow of the required current activates the EF_{LD} flag and the IA can become overloaded and draw greater than 7mA saturation current.

While in current output mode, a current (I_{IA}) that is proportional to the voltage at the IA input is routed to IA_{OUT} and can be used to monitor the load voltage. A resistor converts this current into voltage. This arrangement makes level shifting easy.

Alternatively, the IA can be used as an independent monitoring channel. If this output is not used, connect it to GND to maintain proper function of the monitor stage, as shown in Figure 41.

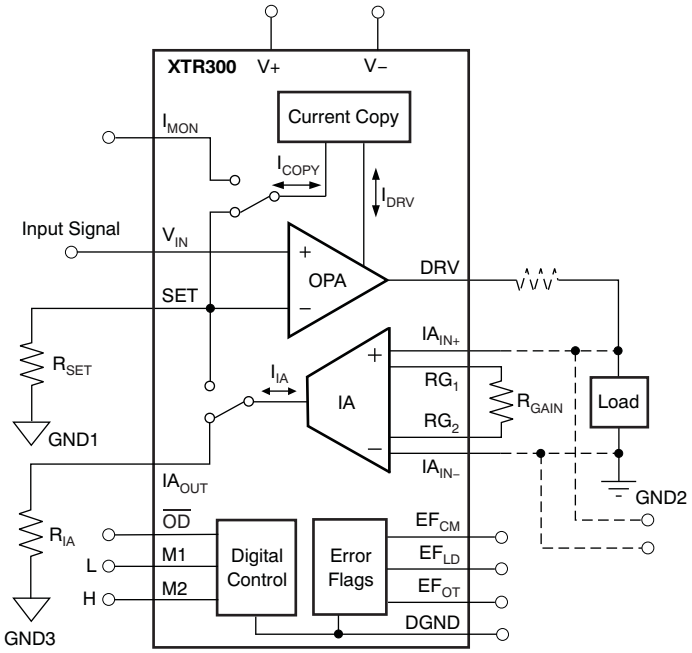


Figure 41. Simplified Current Output Mode Configuration

The transconductance (gain) can be set by the resistor, R_{SET}, according to the equation:

$$I_{OUT} = \frac{10}{R_{SET}} V_{IN} \quad (3)$$

or when adding an offset V_{REF} to get bidirectional output with a single-ended input:

$$I_{OUT} = 10\left(\frac{V_{IN}}{R_{SET}} + \frac{V_{IN} - V_{REF}}{R_{OS}}\right) \quad (4)$$

INPUT SIGNAL CONNECTION

It is possible to drive the XTR300 with a unidirectional input signal and still get a bidirectional output by adding an additional resistor, R_{OS}, and an offset voltage signal, V_{REF}. It can be a mid-point voltage or a signal to shift the output voltage to a desired value.

This design is illustrated in Figure 42a, Figure 42b, and Figure 42c. As with a normal operational amplifier, there are several options for offset-shift circuits. The input can be connected for inverting or noninverting gain. Unlike many op amp input circuits, however, this configuration uses current feedback, which removes the voltage relationship between the noninverting input and output potential because there is no feedback resistor.

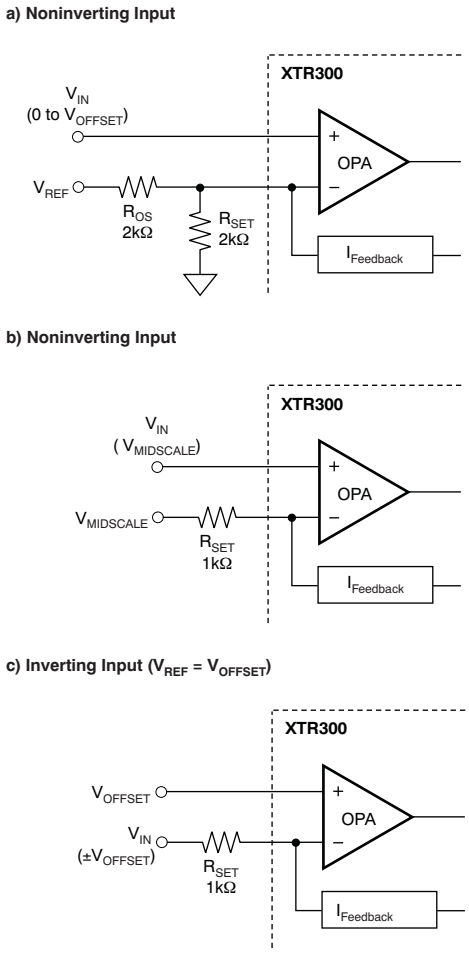


Figure 42. Circuit Options for Op Amp Output Level-Shifting

The input bias current effect on the offset voltage can be reduced by connecting a resistor in series with the positive input that matches the approximate resistance at the negative input. This resistor placed close to the input pin acts as a damping element and makes the design less sensitive to RF noise. See R_3 in Figure 39.

EXTERNALLY-CONFIGURED MODE: OPA AND IA

It is possible to use the precision of the operational amplifier (OPA) and instrumentation amplifier (IA) independently from each other by configuring the digital control pins (M1 high). In this mode, the IA output current is routed to IA_{OUT} and the copy of the OPA output current is routed to I_{MON}, as shown in Figure 4.

This mode allows external configuration of the analog signal routing and feedback loop.

The current output IA has high input impedance, low offset voltage and drift, and very high common-mode rejection ratio. An external resistor (R_{IA}) can be used to convert the output current of the IA (I_{IA}) to an output voltage. The gain is given by:

$$I_{IA} = \frac{2}{R_{GAIN}} V_{IN} \text{ or } V_{IA} = \frac{2R_{IA}}{R_{GAIN}} V_{IN} \quad (5)$$

The OPA provides low drift and high voltage output swing that can be used like a common operational amplifier by connecting a feedback network around it. In this mode, the copy of the output current is available at the I_{MON} pin (it includes the current into the feedback network). It provides an output current limit for protection, which can be set between two ranges by M2. The error flag indicates an overcurrent condition, as well as indicating driving the output into the supply rails.

Alternatively, the feedback can be closed through the I_{MON} pin to create a precise voltage-to-current converter.

DRIVER OUTPUT DISABLE

The OPA output (DRV) can be switched to a high-impedance mode by driving the $\overline{OD}$ control pin low. This input can be connected to the over-temperature flag, EF_{OT}, and a pull-up resistor to protect the IC from over-temperature by disconnecting the load.

The output disable mode can be used to sense and measure the voltage at the IA input pins without loading from the DRV output. This mode allows testing of any voltage present at the I/O connector. However, consider the bias current of the IA input pins.

The digital control inputs, M1 and M2, set the four operation modes of the XTR300 as shown in Table 1. When M1 is asserted low, M2 determines voltage or current mode and the corresponding appropriate current limit (I_{SC}) setting. When M1 is high, the internal feedback connections are opened; IA_{OUT} and I_{MON} are both connected to the output pins; and M2 only determines the current limit (I_{SC}) setting.

M1 and M2 are pulled low internally with 1µA. Terminate these two pins to avoid noise coupling. Output disable ($\overline{OD}$) is internally pulled high with approximately 1µA. When connecting $\overline{OD}$ to EF_{OT}, a 2.2kΩ pull-up resistor is recommended.

Table 1. Summary of Configuration Modes(1)

M1	M2	MODE	DESCRIPTION
L	L	V_{OUT}	Voltage Output Mode, I_{SC} = 20mA
L	H	I_{OUT}	Current Output Mode, I_{SC} = 32mA
H	L	Ext	IA and I_{MON} on ext. pins, I_{SC} = 20A
H	H	Ext	IA and I_{MON} on ext. pins, I_{SC} = 32mA

(1) $\overline{OD}$ is a control pin independent of M1 or M2.

DRIVING CAPACITIVE LOADS AND LOOP COMPENSATION

For normal operation, the driver OPA and the IA are connected in a closed loop for voltage output. In current output mode, the current copy closes the loop directly.

In current output mode, loop compensation is not critical, even for large capacitive loads. However, in voltage output mode, the capacitive load, together with the source impedance and the impedance of the protection circuit, generates additional phase lag. The IA input might also be protected by a low-pass filter that influences phase in the closed loop.

The loop compensation low-pass filter consists of C_C and the parallel resistance of R_{OS} and R_{SET}. For loop stability with large capacitive load, the external phase shift has to be added to the OPA phase. With C_C, the voltage gain of the OPA has to approach zero at the frequency where the total phase approaches 180° + 135°.

The best stability for large capacitive loads is provided by adding a small resistor, R_C (15Ω). See the *Output Protection* section.

An empirical method of evaluation is using a square wave input signal and observing the settling after transients. Use small signal amplitudes only—steep signal edges cause excessive current to flow into the capacitive load and may activate the current limit, which hides or prevents oscillation. A small-signal oscillation can be hidden from large capacitive loads, but observing the I_{MON} output on an appropriate resistor (use a similar value like $R_{SET}||R_{OS}$) would indicate stability issues. Note that noise pulses at I_{MON} during overload (EF_{LD} active) are normal and are caused by cycling of the current mirror.

The voltage output mode includes the IA in the loop. An additional low-pass filter in the input reverses the phase and therefore increases the signal bandwidth of the loop, but also increases the delay. Again, loop stability has to be observed. Overloading the IA disconnects the closed loop and the output voltage rails.

INTERNAL CURRENT SOURCES, SWITCHING NOISE, AND SETTLING TIME

The accuracy of the current output mode and the dc performance of the IA rely on dynamically-matched current mirrors.

Identical current sources are rotated to average out mismatch errors. It can take several clock cycles of the internal 100kHz oscillator (or a submultiple of that frequency) to reach full accuracy. This may dominate the settling time to the 0.1% accuracy level and can be as much as 100µs in current output mode or 40µs in voltage output mode.

A small portion of the switching glitches appear at the DRV output, and also at the I_{MON} and IA_{MON} outputs. The standard circuit configuration, with R_C, C_4, and C_C, which are required for loop compensation and output protection, also helps reduce the noise to negligible levels at the signal output. If necessary, the monitor outputs can be filtered with a shunt capacitor.

IA STRUCTURE, VOLTAGE MONITOR

The instrumentation amplifier has high-impedance NPN transistor inputs that do not load the output signal, which is especially important in current output mode. The output signal is a controlled current that is multiplexed either to the SET pin (to close the voltage output loop) or to IA_{OUT} (for external access).

The principal circuit is shown in Figure 43. The two input buffer amplifiers reproduce the input difference voltage across R_{GAIN}. The resulting current through this resistor is bidirectionally mirrored to the output. That mirroring results in the ideal transfer function of:

$$I_{IA} = IA_{OUT} = 2 \frac{(IA_{IN+} - IA_{IN-})}{R_{GAIN}} \quad (6)$$

The accuracy and drift of R_{GAIN} defines the accuracy of the voltage to current conversion. The high accuracy and stability of the current mirrors result from a cycling chopper technique.

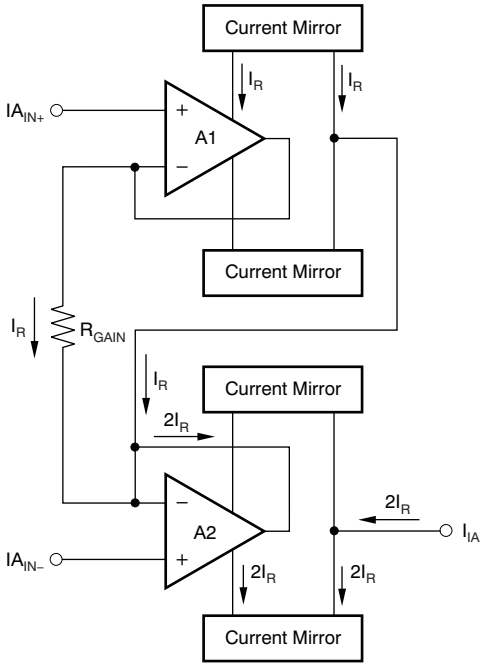


Figure 43. IA Block Diagram

The output current, IA_{OUT}, of the instrumentation amplifier is limited to protect the internal circuitry. This current limit has two settings controlled by the state of M2 (see Electrical Characteristics, Short-Circuit Current specification). Note that if R_{SET} is too small, the current output limitation of the instrumentation amplifier can disrupt the closed loop of the XTR300 in voltage output mode. With M2 = low, the nominal R_{GAIN} of 10kΩ allows an input voltage of $20V_{PP}$, which produces an output current of $4mA_{PP}$. When using lower resistors for R_{GAIN} that can allow higher currents, the IA output current limitation must be taken into account.

CURRENT MONITOR

In current output mode (M2 = high), the XTR300 provides high output impedance. A precision current mirror generates an exact 1/10th copy of the output current and this current is either routed to the summing junction of the OPA to close the feedback loop (in the current output mode) or to the I_{MON} pin for output current monitoring in other operating modes.

The high accuracy and stability of this current split results from a cycling chopper technique. This design eliminates the need for a precise shunt resistor or a precise shunt voltage measurement, which would require high common-mode rejection performance.

During a saturation condition of the DRV output (the error flag is active), the monitor output (I_{MON}) shows a current peak because the loop opens. Glitches from the current mirror chopper appear during this time in the monitor signal. This part of the signal cannot be used for measurement.

ERROR FLAGS

The XTR300 is designed for testability of its proper function and allows observation of the conditions at the load connection without disrupting service.

If the output signal is not in accordance to the transfer function, an error flag is activated (limited by the dynamic response capabilities). These error flags are in addition to the monitor outputs, I_{MON} and IA_{OUT}, which allow the momentary output current (in voltage mode) or output voltage (in current mode) to be read back.

This combination of error flag and monitor signal allows easy observation of the XTR300 for function and working condition, providing the basis for not only remote control, but also for remote diagnosis.

All error flags of the XTR300 have open collector outputs with a weak pull-up of approximately 1µA to an internal 5V. External pull-up resistors to the logic voltage are required when driving 3V or 5V logic.

The output sink current should not exceed 5mA. This is just enough to directly drive optical-couplers, but a current-limiting resistor is required.

There are three error flags:

- **IA Common-Mode Over-Range (EF_{CM})**—goes low as soon as the inputs of the IA reach the limits of the linear operation for the input voltage. This flag shows noise from the saturated current mirrors which can be filtered with a capacitor to GND.
- **Load Error (EF_{LD})**—indicates fault conditions driving voltage or current into the load. In voltage output mode it monitors the voltage limits of the output swing and the current limit condition caused from short or low load resistance. In current output mode it indicates a saturation into the supply rails from a high load resistance or open load.
- **Over-Temperature Flag (EF_{OT})**—is a digital output that goes low if the chip temperature reaches a temperature of +140°C and resets as soon as it cools down to +125°C. It does not automatically shut down the output; it allows the user system to take action on the situation. If desired, this output can be connected to output disable ($\overline{OD}$) which disables the output and therefore removes the source of power. This connection acts like an automatic shut down, but requires a 2.2kΩ external pull-up resistor to safely override the internal current sources. The IA channel is not affected, which allows continuous observation of the voltage at the output.

DIGITAL I/O AND GROUND CONSIDERATIONS

The XTR300 offers voltage output mode, current output mode, external configuration, and instrumentation mode (voltage input). In addition, the internal feedback mode can be disconnected and external loop connections can be made. These modes are controlled by M1 and M2 (see the function table). The $\overline{OD}$ input pin controls enable or disable of the output stage ($\overline{OD}$ is active low).

The digital I/O is referenced to DGND and signals on this pin should remain within 5V of the DGND potential. This DGND pin carries the output low-current (sink current) of the logic outputs. DGND can be connected to a potential within the supply voltage but needs to be 8V below the positive supply. Proper connection avoids current from the digital outputs flowing into the analog ground.

CAUTION

It is important to note that DGND has normally reverse-biased diodes connected to the supply. Therefore, high and destructive currents could flow if DGND is driven beyond the supply rails by more than a diode forward voltage. *Avoid this condition during power-on and power-off!*

OUTPUT PROTECTION

The XTR300 is intended to operate in a harsh industrial environment. Therefore, a robust semiconductor process was chosen for this design. However, some external protection is still required.

The instrumentation amplifier inputs can be protected by external resistors that limit current into the protection cell behind the IC-pins, as shown in Figure 44. This cell conducts to the power-supply connection through a diode as soon as the input voltage exceeds the supply voltage. The circuit configuration example shows how to arrange these two external resistors.

The bias current is best cancelled if both resistors are equal. The additional capacitor reduces RF noise in the input signal to the IA.

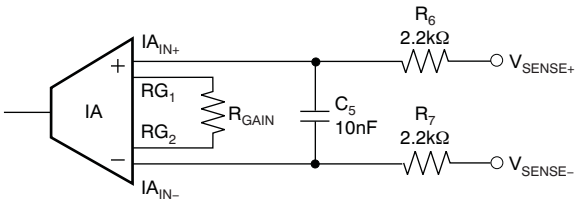


Figure 44. Current-Limiting Resistors

The load connection to the DRV output must be low impedance; therefore, external protection diodes may be necessary to handle excessive currents, as shown in Figure 45. The internal protection diodes start to conduct earlier than a normal external PN-type diode because they are affected by the higher die temperature. Therefore, either Schottky diodes are required, or an additional resistor (R_C) can be placed in series with the input. An example of this protection is shown in Figure 45. Assuming the standard diodes limit the voltage to 1.4V and the internal diodes clamp at 0.7V, this resistor can limit the current into the internal protection diodes to 50mA:

$$\frac{(1.4V - 0.7V)}{15\Omega} = 47mA \quad (7)$$

R_C is also part of the recommended loop compensation. C_4 helps protect the output against RFI and high-voltage spikes.

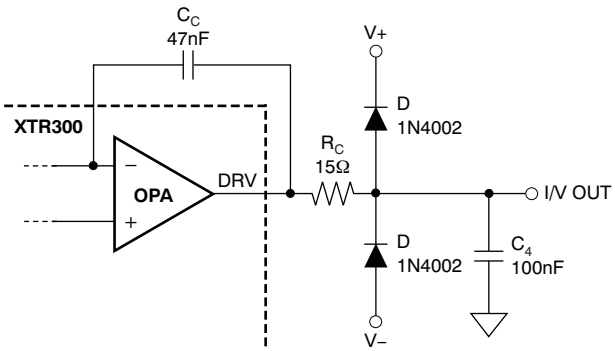


Figure 45. Example for DRV Output Protection

POWER ON/OFF GLITCH

When power is turned on or off, most analog amplifiers generate some glitching of the output because of internal circuit thresholds and capacitive charges. Characteristics of the supply voltage, as well as its rise and fall time, directly influence output glitches. Load resistance and capacitive load also affect the amplitude.

The output disable control ($\overline{OD}$) cannot fully suppress glitches during power-on and power-off, but reduces the energy significantly. The glitch consists of a small amount of current and capacitive charge (voltage) that reacts with the resistive and capacitive load. The bias current of the IA inputs that are normally connected to the output also generate a voltage across the load.

Figure 46 indicates no glitches when transitioning between disable and enable. This measurement is made with a load resistance of 1kΩ and tested in the circuit configuration of Figure 39.

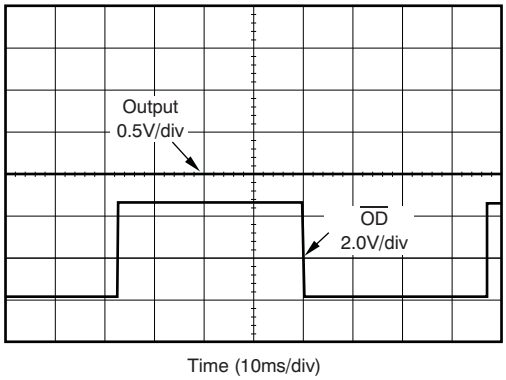


Figure 46. Output Signal During Toggle of $\overline{OD}$

When power is off or with low supply, the output is diode clamped to the momentary supply voltage, but can float while output disabled within those limits unless terminated. Only an external switch (relays or opto-relays) can isolate the output under such conditions. Refer to Figure 47 for an illustration of this configuration. The same consideration applies if low impedance zero output is required, even during power-off.

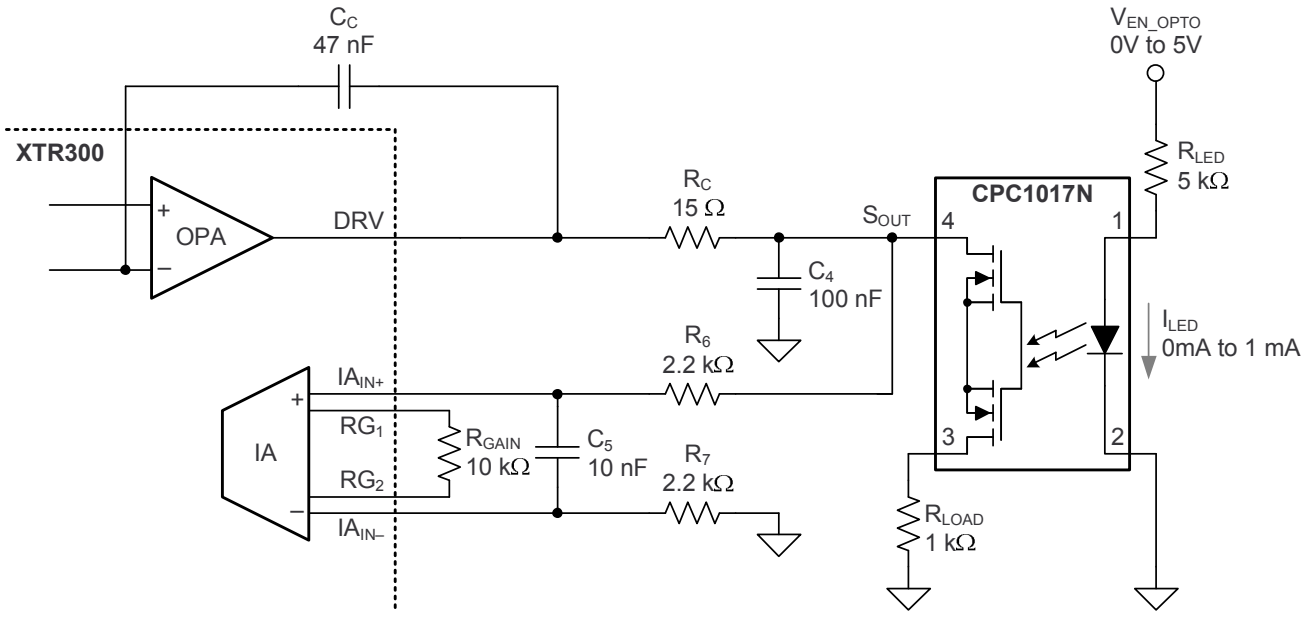


Figure 47. Example for Opto-Relay Output Isolation

LAYOUT CONSIDERATIONS

Supply bypass capacitors should be close to the package and connected with low-impedance conductors. Avoid noise coupled into R_{GAIN}, and observe wiring resistance. For thermal management, see the *Package and Heat Sinking* section.

Layout for the XTR300 is not critical; however, its internal current chopping works best with good (low dynamic impedance) supply decoupling. Therefore, avoid throughhole contacts in the connection to the bypass capacitors or use multiple through-hole contacts. Switching noise from chopper-type power supplies should be filtered enough to reduce influence on the circuit. Small resistors (2Ω, for example) or damping inductors in series with the supply connection (between the dc/dc converter and the XTR circuit) act as a decoupling filter together with the bypass capacitor, as shown in Figure 48.

Resistors connected close to the input pins help dampen environmental noise coupled into conductor traces. Therefore, place the OPA input- and IA input-related resistors close to the package. Also, avoid additional wire resistance in series to R_{SET}, R_{OS}, and R_{GAIN} (observe the reliability of the through-hole contacts), because this resistance could produce gain and offset error as well as drift; 1Ω is already 0.1% of the 1kΩ resistor.

The exposed lead-frame die pad on the bottom of the package must be connected to V−, pin 11 (see the *QFN Package and Heat Sinking* section for more details).

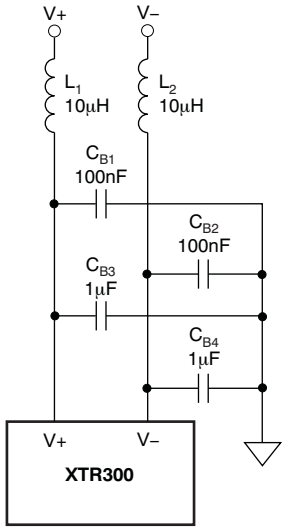


Figure 48. Suggested Supply Decoupling for Noisy Chopper-Type Supplies

QFN PACKAGE AND HEAT SINKING

The XTR300 is available in a QFN package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics of the device through an exposed thermal pad.

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but printed circuit board (PCB) layout greatly influences overall heat dissipation. The thermal resistance from junction-to-ambient (θ_{JA}) is specified for the packages with the exposed thermal pad soldered to a normalized PCB, as described in Technical Brief SLMA002, *PowerPAD™ Thermally-Enhanced Package*. See also *EIA/JEDEC Specifications JESD51-0 to 7, QFN/SON PCB Attachment* (SLUA271), and *Quad Flatpack No-Lead Logic Packages* (SCBA017). These documents are available for download at www.ti.com.

NOTE: All thermal models have an accuracy variation of ±20%.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.

The exposed lead-frame die pad on the bottom of the package must be connected to the V− pin.

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. It is dominated by the power dissipation of the output transistors of the OPA. For dc signals, power dissipation is equal to the product of output current, I_{OUT} and the output voltage across the conducting output transistor ($V_S - V_{OUT}$).

It is very important to note that the temperature protection does not shut the part down in overtemperature conditions, unless the EF_{OT} pin is connected to the output enable pin $\overline{OD}$; see the *Driver Output Disable* section.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design and conditions. The QFN package with an exposed thermal pad is specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation.

To appropriately determine the required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize overheat conditions and allow for reliable long-term operation.

The heat sinking efficiency can be tested using the EF_{OT} output signal. This output goes low at nominally +140°C junction temperature (assume 6% tolerance). With full power dissipation (for example, maximum current into a 0Ω load), the ambient temperature can be slowly raised until the OT flag goes low. This flag would indicate the minimum heat-sinking for the usable operation condition.

The recommended landing pattern for the QFN package is shown at the end of this data sheet.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March, 2006) to Revision C **Page**

- Updated document format to current standards 1
- Deleted information regarding HART digital communication throughout document 1
- Added footnote regarding small-signal measurement with no capacitive load in Electrical Characteristics (Voltage Output Mode) 3
- Corrected *Nominal setup for ±20mA Output* parameter from *±20V Output* in Electrical Characteristics (Current Output Mode) 4
- Changed *Common-Mode Voltage Range* parameter to *Input Voltage Range* in Electrical Characteristics (Instrumentation Amplifier) 6
- Added conditions to *Short Circuit Current* parameter in Electrical Characteristics (Instrumentation Amplifier) 6
- Changed last paragraph of *Driver Output Disable* section 22
- Corrected footnote to Table 1 22
- Revised *Over-Temperature Flag* description in *Error Flags* section to indicate the need for a 2.2kΩ resistor 25
- Revised *Power On/Off Glitch* section and added Figure 47 27
- Updated and combined *QFN Package and Heat Sinking* sections 28
- Added *Power Dissipation* section 29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
XTR300AIRGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	XTR 300	Samples
XTR300AIRGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	XTR 300	Samples
XTR300AIRGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	XTR 300	Samples
XTR300AIRGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	XTR 300	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

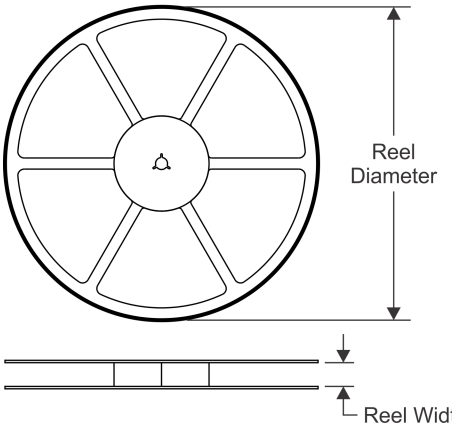
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

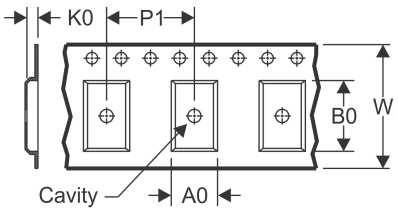
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

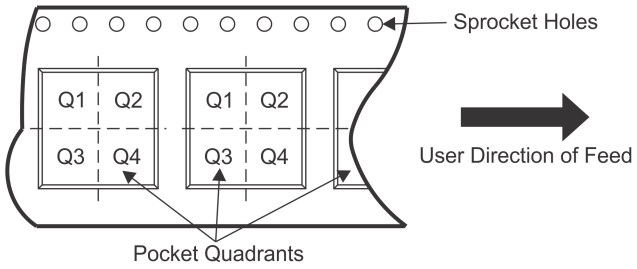


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

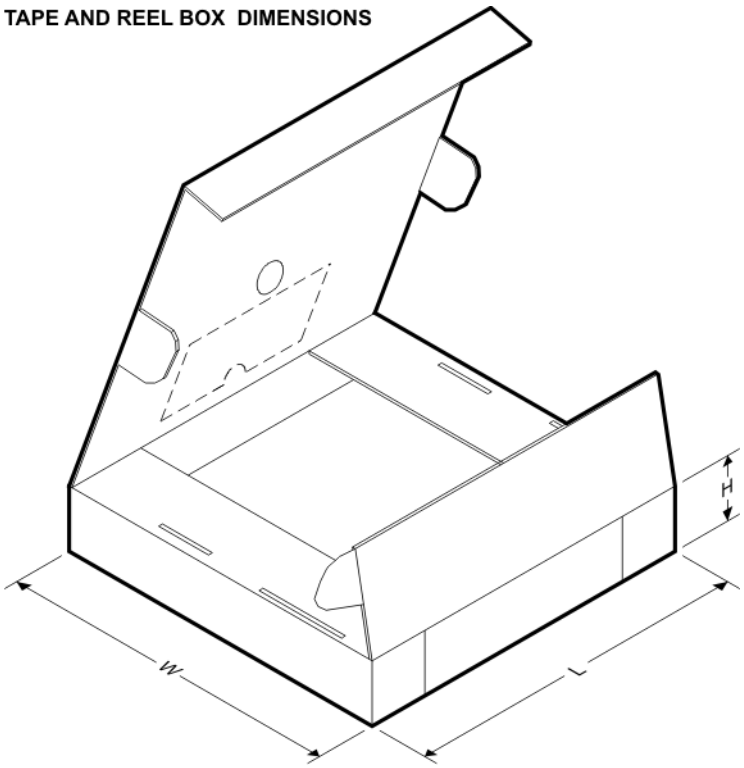
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XTR300AIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
XTR300AIRGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

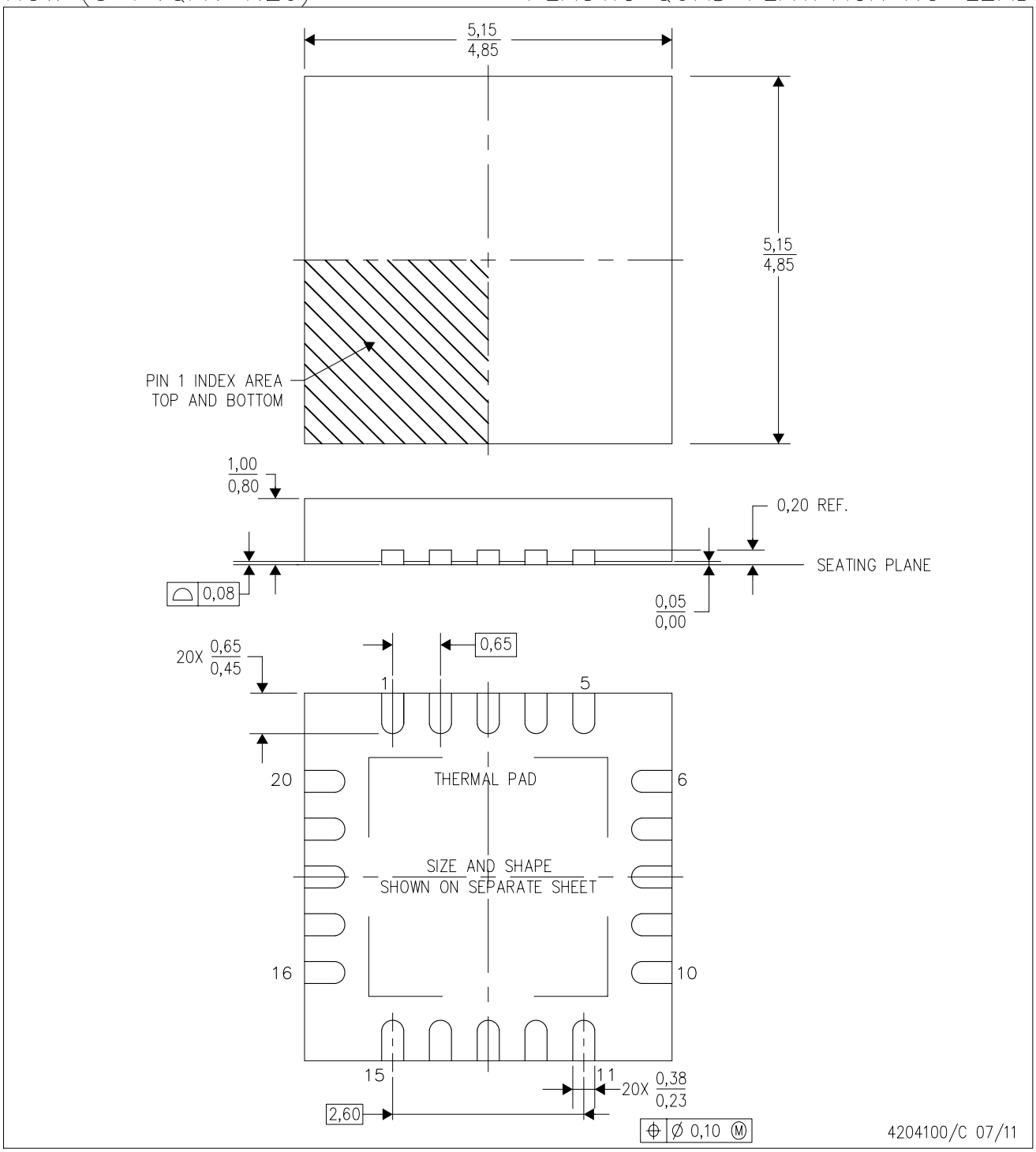
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XTR300AIRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
XTR300AIRGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

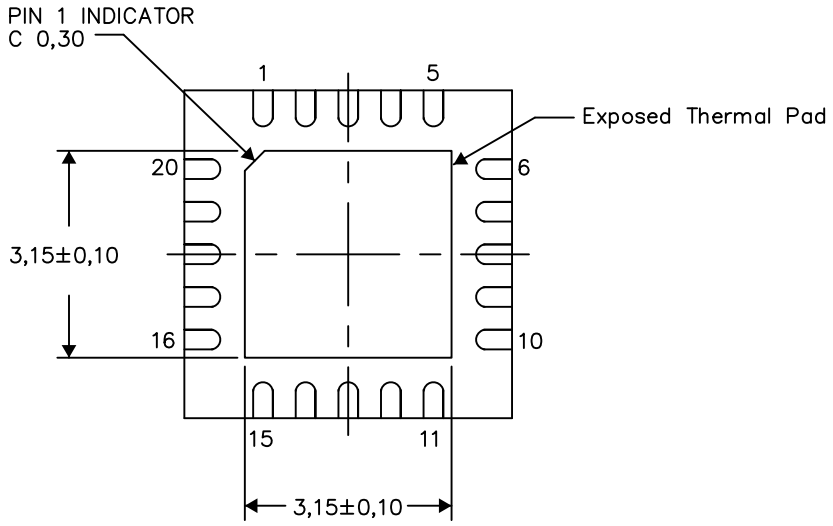
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



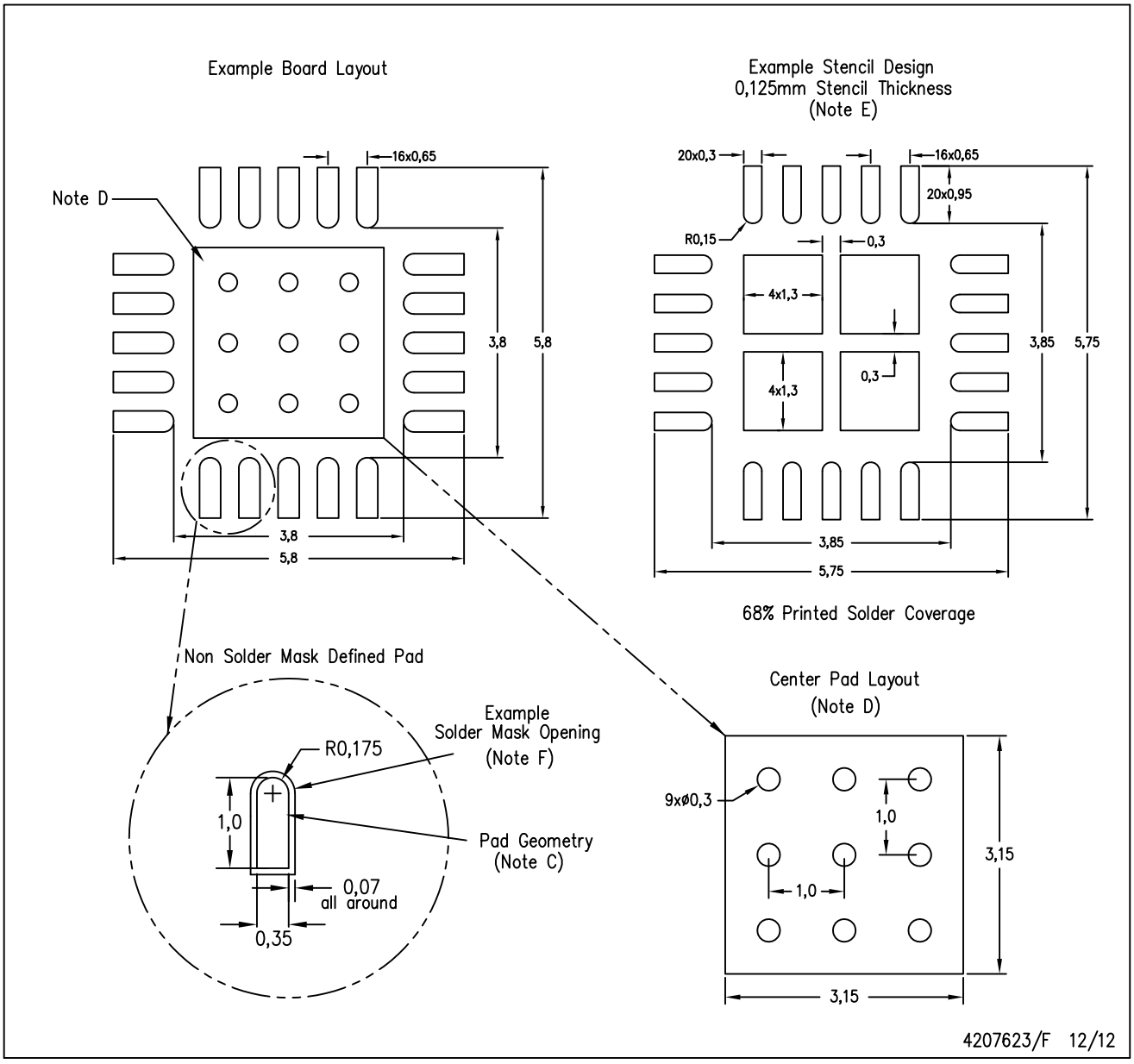
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/K 12/12

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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Logic	logic.ti.com	Security	www.ti.com/security
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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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