SanDisk®

(JEDEC Package)

Data Sheet
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Revision History

- *February 2007 Revision 1.0—Preliminary draft of initial release*
- *March 2007Revsision 1.1—Preliminary datasheet release*
- *July 2007 Revision 1.2—iNAND ball array, mechanical and electrical specifications and ordering info updated. Ball and signal names changed (FCAP changed to CREG, VDD_H changed to VDDH, VDD_F changed to VDDF) ball address grids revised (to conform to JEDEC format)*

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1. INTRODUCTION

1.1. General Description

SanDisk iNAND combines SanDisk's advanced MLC NAND flash with SanDisk's controller and flash management technology, providing a highly reliable, high performance on-board mass storage device.

Designed specifically for mobile multimedia applications, iNAND is the most mature on board SD/MMC device since 2005, providing mass storage of up to 8GB in JEDEC compatible form factors, with low power consumption and high performance that are an ideal solution for multimedia handsets of 2.5G and up.

MLC NAND Flash is the ideal storage medium for portable, battery-powered devices. It features low power consumption and is non-volatile, requiring no power to maintain the stored data. It also has a wide operating range for temperature, shock and vibration.

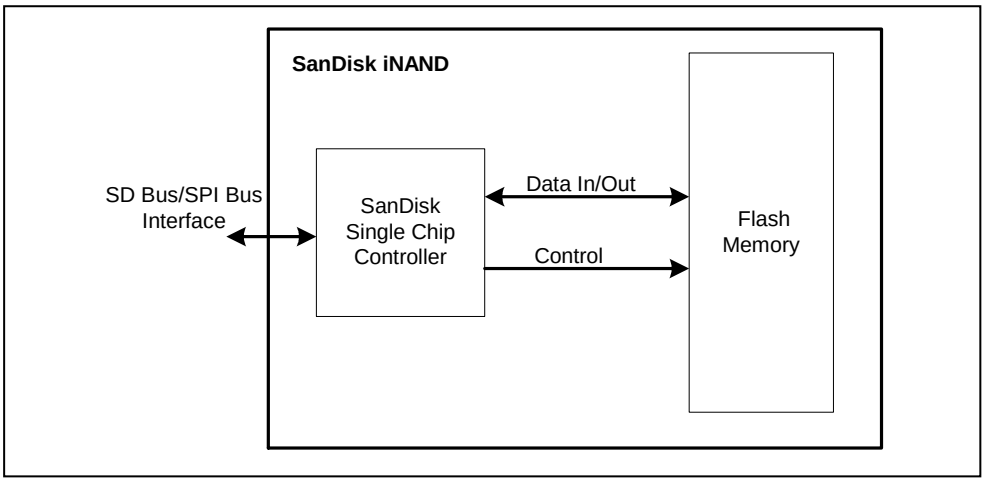
SanDisk iNAND is well-suited to meet the needs of small, low power, electronic devices. With form factors measuring 11.5mm x 13mm, 12mm x 16mm and 12mm x 18mm, JEDEC compatible and 169, 0.5mm ball pitch, iNAND is fit for a wide variety of portable devices like multi-media mobile handsets, personal media players, GPS devices and more.

To support this wide range of applications, iNAND is offered with an SD Interface. The SD interface is widely adopted by all leading industry chipsets, and provides a 4-bit high-speed data bus for maximum performance. For compatibility with existing controllers, the iNAND offers, in addition to these interfaces, an alternate communication-protocol based on the SPI standard.

These interfaces allow for easy integration into any design, regardless of which type of microprocessor is used. All device and interface configuration data (such as maximum frequency and card identification) are stored on the device.

The SanDisk iNAND provides up to 8 GB of memory for use in mass storage applications. In addition to the mass-storage-specific flash memory chip, iNAND includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management, wear leveling, and clock control. Figure 1 is a block diagram of the SanDisk iNAND with SD Interface.

Figure 1 - SanDisk iNAND Block Diagram



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1.2. Features

SanDisk iNAND product features include the following:

- Up to 8 GB of data storage
- SD 1.1 and 2.0 protocol compatible
- Supports SPI Mode
- Designed for portable and stationary applications that require high performance and reliable data storage
- Voltage range:
  - Core voltage (VDDF): 2.7-3.6v
  - Host voltage, either: 1.7-1.9v or 2.7-3.6v
- Variable clock rate 0-25 MHz (default), 0-50 MHz (high-speed)
- Up to 25 MB/sec bus transfer rate (using 4 parallel data lines)
- Correction of memory-field errors
- Built-in write protection features (permanent and temporary)
- Application-specific commands
- Standard footprint across all capacities

1.3. Document Scope

This document describes the key features and specifications of the SanDisk iNAND as well as the information required to interface it to a host system. Chapter 2 describes the physical and mechanical properties of iNAND, Chapter 3 contains the pins and register overview, and Chapter 4 gives a general overview of the SD protocol. Information about SPI Protocol can be referenced in Section 7 of the *SDA Physical Layer Specification, Version 2.00.*

1.4. iNAND Standard

SanDisk iNAND devices are fully compatible with the SDA *Physical Layer Specification*, *Version 2.00*. This specification is available from the SD Card Association (SDA).

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1.5. Functional Description

The SanDisk iNAND contains a high-level, intelligent subsystem as shown in Figure 1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of storage devices. These capabilities include:

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- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives)
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.6. Technology Independence

The 512-byte sector size of the SanDisk iNAND is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host software simply issues a read or write command to the card. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important since flash devices are getting increasingly complex with current advanced NAND MLC processes. Because iNAND uses an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support iNAND technology today will be able to access future SanDisk devices built with new flash technology without having to update or change the host software.

1.7. Defect and Error Management

The SanDisk iNAND contains a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary, iNAND will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. The soft error rate specification for iNAND is much better than the magnetic disk drive specification. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk iNAND unparalleled reliability.

1.8. Wear Leveling

Wear-leveling is an intrinsic part of the erase pooling functionality of iNAND.

1.9. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received in less than 5 milliseconds (ms). The host does not have to take any action for this to occur. However, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep, and respond.

1.10. iNAND — SD Bus Mode

The following sections provide valuable information on SanDisk iNAND in SD Bus mode.

SanDisk iNAND devices are fully compliant with the SDA *Physical Layer Specification*, *Version 2.00*. Card Specific Data (CSD) Register structures are compliant with CSD Structure 1.0 and 2.0.

This section covers Negotiating Operating Conditions, Card Acquisition and Identification, Card Status, Memory Array Partitioning, Read/Write Operations, Data Transfer Rate, Data Protection in Flash Cards, Write Protection, Copy Bit, and CSD Register.

Additional practical card detection methods can be found in application notes pertaining to the SDA *Physical Layer Specification*, *Version 2.00*.

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Figure 2 - Memory Array Partitioning

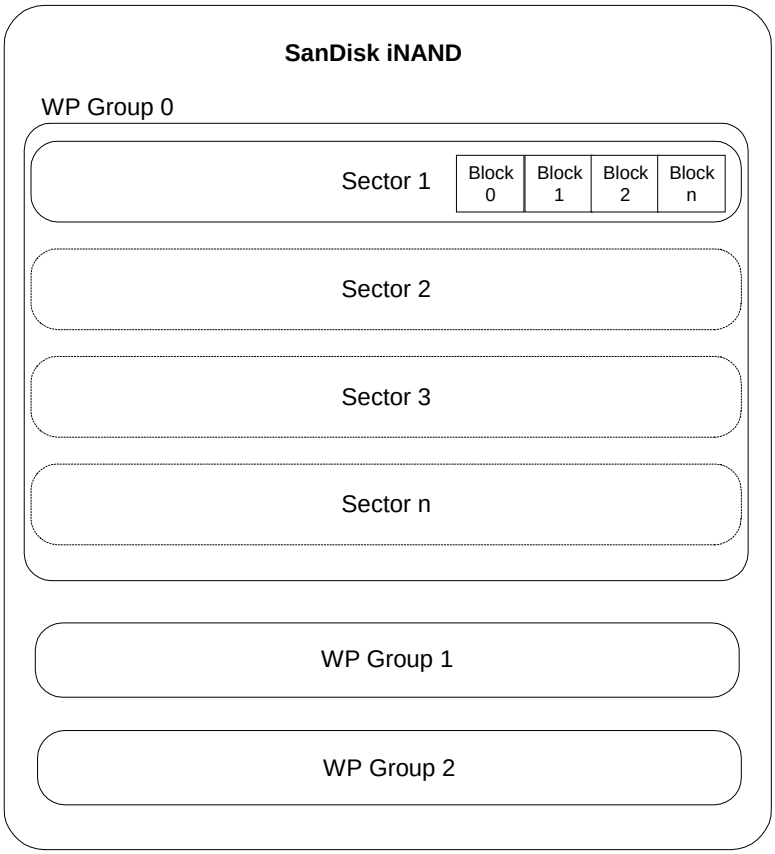

Figure 3 - Data Transfer Formats

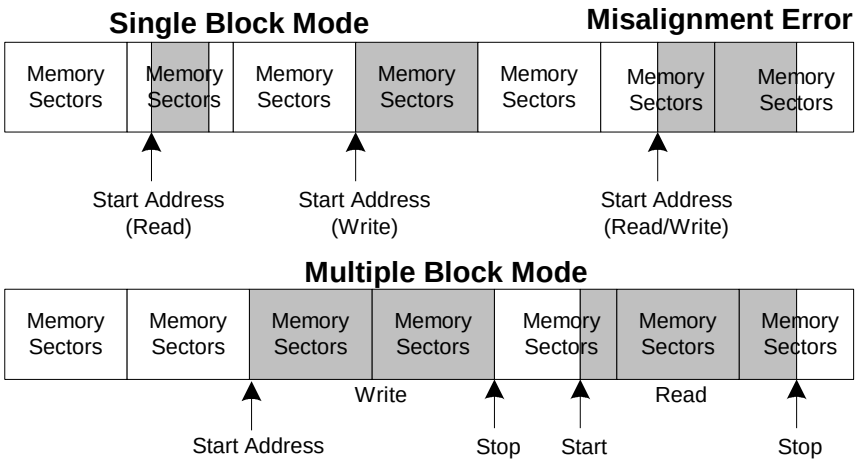

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Table 1 - Mode Definitions

Mode	Description
Single Block	In this mode the host reads or writes one data block in a pre-specified length. The data block transmission is protected with 16-bit CRC that is generated by the sending unit and checked by the receiving unit. The block length for read operations is limited by the device sector size (512 bytes) but can be as small as a single byte. Misalignment is not allowed. Every data block must be contained in a single physical sector. The block length for write operations must be identical to the sector size and the start address aligned to a sector boundary.
Multiple Block	This mode is similar to the single block mode, except for the host can read/write multiple data blocks (all have the same length) that are stored or retrieved from contiguous memory addresses starting at the address specified in the command. The operation is terminated with a stop transmission command. Misalignment and block length restrictions apply to multiple blocks and are identical to the single block read/write operations.

1.11. SPI Mode

The SPI Mode is a secondary communication protocol for iNAND devices. This mode is a subset of the SD Protocol, designed to communicate with an SPI channel, commonly found in Motorola and other vendors' microcontrollers.

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2. PRODUCT SPECIFICATIONS

2.1. Overview

For details about the environmental, reliability and durability specifications, refer to *Section 8.1* of the SDA *Physical Layer Specification*, *Version 2.00*.

2.2. Typical Power Requirements

Table 2 - iNAND Power Requirements (Ta=25°C@3.3V)

		Value	Measurement	Average
Sleep		250	uA	Max.
Read	Default Speed	100	mA	Max.
	High-Speed	200	mA	Max.
Write	Default Speed	100	mA	Max.
	High-Speed	200	mA	Max.
VDD (ripple: max, 60mV peak-to-peak) 2.7 V – 3.6 V				

Note: Current measurement numbers are average over 1 second.

2.3. Operating Conditions

2.3.1. Operating and Storage Temperature Specifications

Table 3 - Operating and Storage Temperatures

Temperature	Operating	-25° C to 85° C
	Non-Operating: After soldered onto PC Board	-40° C to 85° C

2.3.2. Moisture Sensitivity

The moisture sensitivity level for iNAND is MSL = 3.

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2.4. System Performance

All performance values for iNAND in Table 4 were measured using the following conditions:

- Voltage range:
  - Core voltage (VDDF): 2.7-3.6v
  - Host voltage, either: 1.7-1.9v or 2.7-3.6v
- Temperature -25° C to 85° C

Table 4 - System Performance

Timing	Value
Sustained Read	15 MB/s
Sustained Write	9 MB/s
Block Read Access Time (MAX)	100 ms
Block Write Access Time (MAX)	250 ms
CMD1 to Ready after Power-up (MAX)	1000 ms

2.5. System Reliability and Maintenance

Table 5 - Reliability and Maintenance Specifications

MTBF	>1,000,000 hours
Preventative Maintenance	None
Data Reliability	<1 non-recoverable error in 10^{14} bits read

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2.6. Physical Specifications

The SanDisk iNAND is a 169-pin, thin fine-pitched ball grid array (BGA). See Figure 4 and Figure 5 (169-pin) for physical specifications and dimensions.

Figure 4 - iNAND Specifications Top and Side View (Detail A)

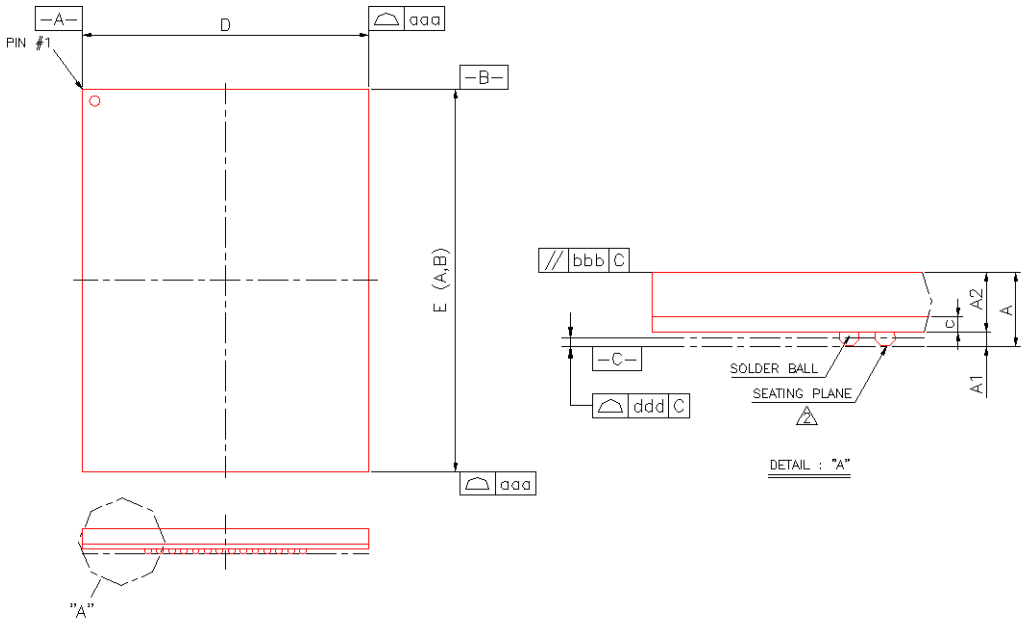

Figure 5 - iNAND Specifications Bottom View and Ball Data (Detail B)

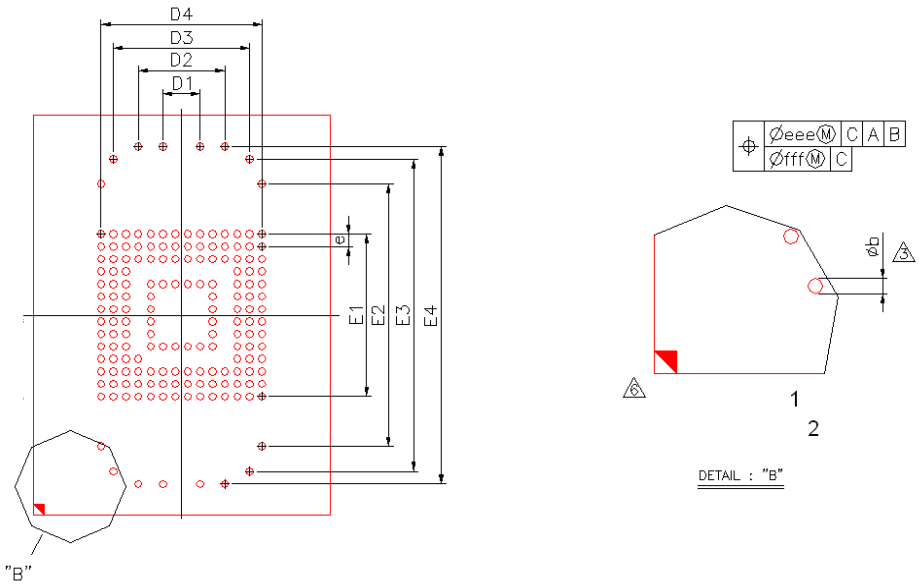

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Table 6 - iNAND Package Specifications

	Dimension in millimeters			**Dimension in inches**		
Symbol	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	---	---	1.20	---	---	0.047
A1	0.17	0.22	0.27	0.007	0.009	0.011
A2	0.785	0.835	0.885	0.031	0.033	0.035
C	0.17	0.21	0.25	0.007	0.008	0.010
D	11.93	12.00	12.07	0.470	0.472	0.475
E (A)[1]	15.93	16.00	16.07	0.627	0.630	0.633
E (B)[2]	17.93	18.00	18.07	0.706	0.709	0.711
D1	---	1.50	---	---	0.059	---
D2	---	3.50	---	---	0.138	---
D3	---	5.50	---	---	0.217	---
D4	---	6.50	---	---	0.256	---
E1	---	6.50	---	---	0.256	---
E2	---	10.50	---	---	0.413	---
E3	---	12.50	---	---	0.492	---
E4	---	13.50	---	---	0.531	---
e	---	.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	14/14			14/14		

[1] These measurements are for the 16 x 12mm package.

[2] These measurements are for the 18 x 12mm package.

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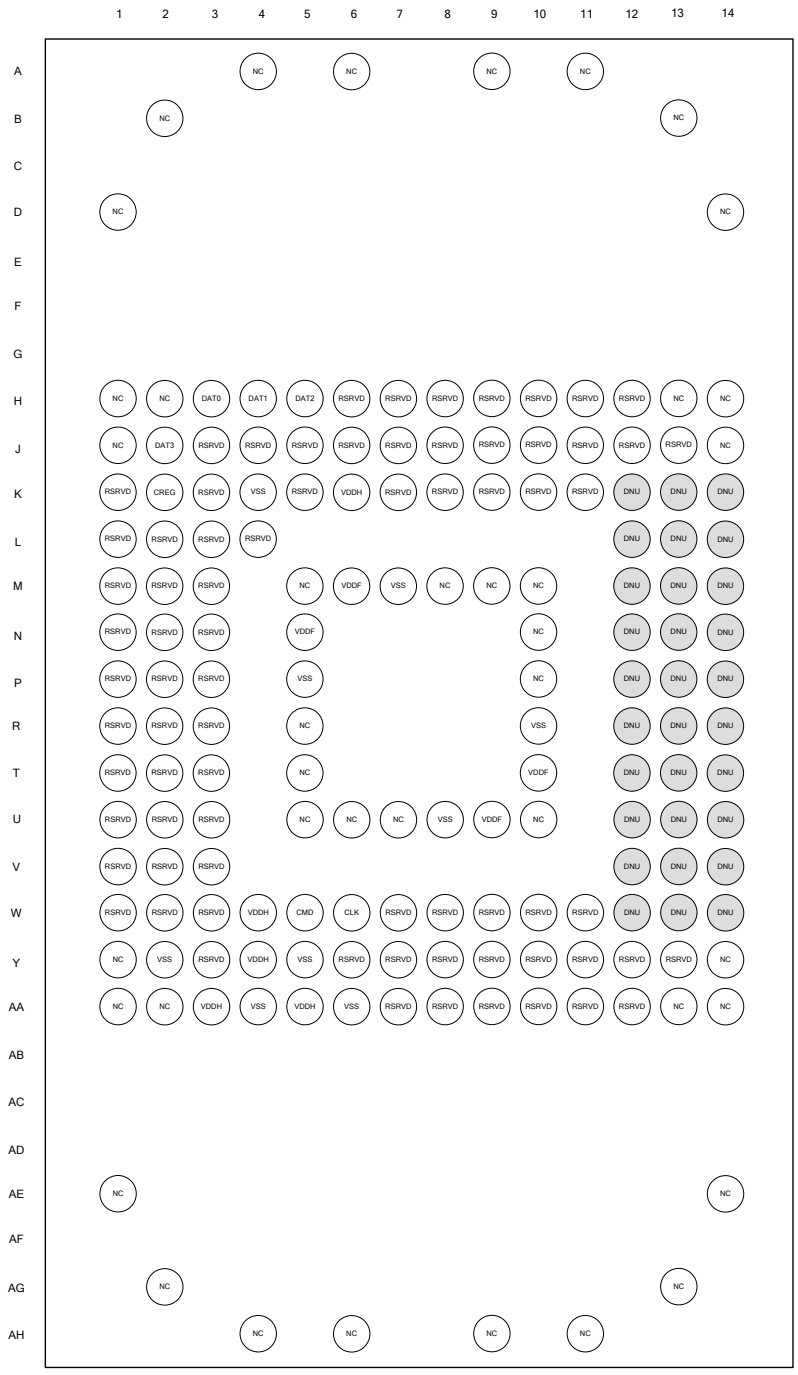
3. iNAND Interface Description

3.1. iNAND Ball Array

Figure 6 illustrates the SanDisk iNAND ball array.

Figure 6 - iNAND Ball Array (Top View)



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3.2. Pins and Signal Description

Table 7 contains the SanDisk iNAND functional pin assignment.

Table 7 - iNAND Pin Assignment

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A4	NC	**K8**	RSRVD	**R2**	RSRVD	**W11**	RSRVD
A6	NC	**K9**	RSRVD	**R3**	RSRVD	**W12**	DNU
A9	NC	**K10**	RSRVD	**R5**	RSRVD	**W13**	DNU
A11	NC	**K11**	RSRVD	**R10**	VSS	**W14**	DNU
B2	NC	**K12**	DNU	**R12**	DNU	**Y1**	NC
B13	NC	**K13**	DNU	**R13**	DNU	**Y2**	VSS
D1	NC	**K14**	DNU	**R14**	DNU	**Y3**	RSRVD
D14	NC	**L1**	RSRVD	**T1**	RSRVD	**Y4**	VDDH
H1	NC	**L2**	RSRVD	**T2**	RSRVD	**Y5**	VSS
H2	NC	**L3**	RSRVD	**T3**	RSRVD	**Y6**	RSRVD
H3	DAT0	**L4**	RSRVD	**T5**	RSRVD	**Y7**	RSRVD
H4	DAT1	**L12**	DNU	**T10**	VDDF	**Y8**	RSRVD
H5	DAT2	**L13**	DNU	**T12**	DNU	**Y9**	RSRVD
H6	NC	**L14**	DNU	**T13**	DNU	**Y10**	RSRVD
H7	RSRVD	**M1**	RSRVD	**T14**	DNU	**Y11**	RSRVD
H8	RSRVD	**M2**	RSRVD	**U1**	RSRVD	**Y12**	RSRVD
H9	RSRVD	**M3**	RSRVD	**U2**	RSRVD	**Y13**	RSRVD
H10	RSRVD	**M5**	RSRVD	**U3**	RSRVD	**Y14**	NC
H11	RSRVD	**M6**	VDDF	**U5**	RSRVD	**AA1**	NC
H12	RSRVD	**M7**	VSS	**U6**	RSRVD	**AA2**	NC
H13	NC	**M8**	RSRVD	**U7**	RSRVD	**AA3**	VDDH
H14	NC	**M9**	RSRVD	**U8**	VSS	**AA4**	VSS
J1	NC	**M10**	RSRVD	**U9**	VDDF	**AA5**	VDDH
J2	DAT3	**M12**	DNU	**U10**	RSRVD	**AA6**	VSS
J3	RSRVD	**M13**	DNU	**U12**	DNU	**AA7**	RSRVD
J4	RSRVD	**M14**	DNU	**U13**	DNU	**AA8**	RSRVD
J5	RSRVD	**N1**	RSRVD	**U14**	DNU	**AA9**	RSRVD
J6	RSRVD	**N2**	RSRVD	**V1**	RSRVD	**AA10**	RSRVD
J7	RSRVD	**N3**	RSRVD	**V2**	RSRVD	**AA11**	RSRVD
J8	RSRVD	**N5**	VDDF	**V3**	RSRVD	**AA12**	RSRVD
J9	RSRVD	**N10**	RSRVD	**V12**	DNU	**AA13**	NC
J10	RSRVD	**N12**	DNU	**V13**	DNU	**AA14**	NC
J11	RSRVD	**N13**	DNU	**V14**	DNU	**AE1**	NC
J12	RSRVD	**N14**	DNU	**W1**	RSRVD	**AE14**	NC
J13	RSRVD	**P1**	RSRVD	**W2**	RSRVD	**AG2**	NC
J14	NC	**P2**	RSRVD	**W3**	RSRVD	**AG13**	NC
K1	RSRVD	**P3**	RSRVD	**W4**	VDDH	**AH4**	NC
K2	CREG	**P5**	VSS	**W5**	CYD	**AH6**	NC
K3	RSRVD	**P10**	RSRVD	**W6**	CLK	**AH9**	NC
K4	VSS	**P12**	DNU	**W7**	RSRVD	**AH11**	NC
K5	RSRVD	**P13**	DNU	**W8**	RSRVD		
K6	VDDH	**P14**	DNU	**W9**	RSRVD		
K7	RSRVD	**R1**	RSRVD	**W10**	RSRVD		

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Note: Balls marked as NC are Not Connected inside the device. Balls marked DNU are connected to internal signals and must be left floating. Balls marked as RSRVD are reserved for future use and recommended to be left floating for future compatibility.

3.3. Bus Topologies

SanDisk iNAND products support two communication protocols: SD and SPI. For more details, refer to *Section 3.5* of the SDA *Physical Layer Specification*, *Version 2.00*. Section 6 of the specification contains a bus circuitry diagram for reference.

3.4. Electrical Interface

Refer to *Section 6.4* of the SDA *Physical Layer Specification*, *Version 2.00*.

3.4.1. Power Up

Refer to *Section 6.4.1* of the SDA *Physical Layer Specification, Version 2.00*.

3.4.2. Bus Operating Conditions

SPI Mode bus operating conditions are identical to SD Bus Mode operating conditions. For details, see *Section 6.6* of the SDA *Physical Layer Specification*, *Version 2.00*.

3.4.3. Bus Timing (Default)

See *Section 6.7* of the SDA *Physical Layer Specification, Version 2.00.*

3.4.4. Bus Timing (High-Speed Mode)

See *Section 6.8* of the SDA *Physical Layer Specification, Version 2.00*.

3.5. iNAND Registers

There is a set of registers within the iNAND interface. For specific information about each register, refer to *Section 5* of the SDA *Physical Layer Specification, Version 2.00*.

SanDisk iNAND contains a set of information registers. Register descriptions and SDA references are provided in *Section 5.0* of the SDA *Physical Layer Specification*, *Version 2.00*.

Table 8 - iNAND Register Overview

Register Abbreviation	Width (bits)	Register Name
CID	128	Card Identification Number
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration
OCR	32	Operation Conditions
SSR	512	SD Status
CSR	32	Card status; information about the card status.

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3.5.1. Operating Conditions Register

The **Operation Conditions Register (OCR)** stores the VDD voltage profile for iNAND. Refer to *Section 5.1* of the SDA *Physical Layer Specification*, *Version 2.00*.

3.5.2. Card Identification Register

The **Card Identification (CID) Register** is 16 bytes long and contains the unique card identification number. It is programmed during manufacturing and cannot be changed by iNAND hosts. See Table 9.

Table 9 - CID Register Definitions

Name	Type	Width (bits)	CID Value	Comments
Manufacturer ID (MID)	Binary	8	0x03	Manufacturer IDs are controlled and assigned by the SD-3C, LLC
OEM/Application ID (OID)	ASCII	16	SD ASCII Code 0x53, 0x44	Identifies the card OEM and/or the card contents. The OID is controlled and assigned by the SD-3C, LLC
Product Name (PNM)	ASCII	40	ST08 ST04 ST02 ST01 ST512	Five ASCII characters long
Product Revision (PRV)	BCD	8	Product Revision xx	See Section 5.2 in the SDA *Physical Layer Specification*, *Version 2.00*
Serial Number (PSN)	Binary	32	Product Serial Number	32-bit unsigned integer
Reserved	---	4	---	---
Manufacture Date Code (MDT)	BCD	12	Manufacture date (for ex. April 2001= 0x014)	Manufacturing date—yym (offset from 2000)
CRC7 checksum	Binary	7	CRC7*	Calculated
Not used,always	---	1	---	---

Note: SD-3C, LLC is a limited liability company established by Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation.

*The CRC checksum is computed by using the following formula: CRC Calculation: $G(x) = x^7+x^3+1$

$M(x)=(MID\text{-}MSB)*x^{119}+\ldots+(CIN\text{-}LSB)*x^0$

$CRC[6\ldots0]=Remainder[(M(x)*x^7)/G(x)]$

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3.5.3. Card Specific Data Register

The **Card Specific Data (CSD) Register** configuration information is required to access iNAND data. The CSD defines the data format, error correction type, maximum data access time, etc. The field structures of the CSD Register vary depending on the physical specifications and card capacity. The *CSD_STRUCTURE* field in the CSD Register indicates which structure version is used. Table 10 shows the version number as it relates to the CSD structure. Refer to *Section 5.3.1* of the SDA *Physical Layer Specification, Version 2.00* for more information.

Table 10 - CSD Register Structures

CSD_STRUCTURE	CSD Structure Version	Valid for SD Memory Card Physical Specification Version / Card Capacity
0	CSD Version 1.0	Version 1.01 to 1.10
		Version 2.00 / Standard Capacity
1	CSD Version 2.0	Version 2.00 / High Capacity
2-3	Reserved	---

Table 11 provides an overview of the CSD Register. More field-specific information can be found in *Section 5.3.2, Table 5-4* of the SDA *Physical Layer Specification, Version 2.00*.

Table 11 - CSD Register (CSD Version 1.0)

Field	CSD Value	Description
CSD_ STRUCTURE	1.0	CSD structure
---	---	Reserved
TAAC	1.5 msec	Data read access time-1
NSAC	0	Data read access time-2 in CLK cycles (NSAC*100)
TRANS_ SPEED	Default 25MHz	Max. data transfer rate
	High-speed 50MHz	
CCC	All (inc. WP, lock/unlock)	Card command classes
READ_BL_ LEN	2G Up to 1G	Max. read data block length
READ_BL_ PARTIAL	Yes	Partial blocks for read allowed
WRITE_BLK_ MISALIGN	No	Write block misalignment
READ_BLK_ MISALIGN	No	Read block misalignment
DSR_IMP	No	DSR implemented
---	---	Reserved
C_SIZE	2 GB 1 GB 512 MB	Device size
VDD_R_ CURR_MIN	According to card performance	Max. read current @VDD min.
VDD_R_ CURR_MAX	According to card	Max. read current @VDD max.

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Field	CSD Value	Description
	performance	
VDD_W_ CURR_MIN	According to card performance	Max. write current @VDD min.
VDD_W_ CURR_MAX	According to card performance	Max. write current @VDD max.
C_SIZE_ MULT	2G=2048 1G=1024 512=512	Device size multiplier
ERASE_BLK_EN	Yes	Erase single block enable
SECTOR_ SIZE	32 blocks	Erase sector size
WP_GRP_ SIZE	128 sectors	Write protect group size
WP_GRP_ ENABLE	Yes	Write protect group enable
Reserved	---	Reserved for MMC compatibility
R2W_ FACTOR	x16	Write speed factor
WRITE_BL_ LEN	2G Up to 1G	Max. write data block length
WRITE_BL PARTIAL	No	Partial blocks for write allowed
---	---	Reserved
FILE_ FORMAT_ GRP	0	File format group
COPY	Has been copied	Copy flag (OTP)
PERM_ WRITE_ PROTECT	Not protected	Permanent write protection
TMP_WRITE_PROTECT	Not protected	Temporary write protection
FILE_ FORMAT	HD w/partition	File format
Reserved	---	Reserved
CRC	CRC7	CRC
---	---	Not used, always “1”

Refer to *Section 5.3.3, Table 5-16* of the SDA *Physical Layer Specification, Version 2.00* for more detailed information.

Table 12 - CSD Register (CSD Version 2.0)

Field	CSD Value	Description
CSD_ STRUCTURE	2.0	CSD structure
---	---	Reserved
TAAC	1.5 ms	Data read access time-1
NSAC	0	Data read access time-2 in CLK cycles (NSAC*100)
TRANS_ SPEED	Default 25MHz	Max. data transfer rate
	High-speed 50MHz	
CCC	010110110101b	Card command classes

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Field	CSD Value	Description
READ_BL_ LEN	---	Max. read data block length
READ_BL_ PARTIAL	Yes	Partial blocks for read allowed
WRITE_BLK_ MISALIGN	No	Write block misalignment
READ_BLK_ MISALIGN	No	Read block misalignment
DSR_IMP	No	DSR implemented
---	0	Reserved
C_SIZE	8 GB	Device size
	4 GB	
---	0	Reserved
ERASE_BLK_EN	1	Erase single block enable
SECTOR_ SIZE	32 blocks	Erase sector size
WP_GRP_ SIZE	128 sectors	Write protect group size
WP_GRP_ ENABLE	Yes	Write protect group enable
Reserved	---	Reserved for MMC compatibility
R2W_ FACTOR	x16	Write speed factor
WRITE_BL_ LEN	---	Max. write data block length
WRITE_BL PARTIAL	No	Partial blocks for write allowed
---	---	Reserved
FILE_ FORMAT_ GRP	0	File format group
COPY	Has been copied	Copy flag (OTP)
PERM_ WRITE_ PROTECT	Not protected	Permanent write protection
TMP_WRITE_PROTECT	No protected	Temporary write protection
FILE_ FORMAT	HD w/partition	File format
Reserved	---	Reserved
CRC	CRC7	CRC
---	---	Not used, always “1”

3.5.4. Card Status Register

The **Card Status Register (CSR)** transmits the iNAND’s status information (which may be stored in a local status register) to the host. The CSR is defined in Section *4.10.1* in the SDA *Physical Layer Specification, Version 2.00*.

3.5.5. SD Status Register

The **SD Status Register (SSR)** contains status bits that are related to iNAND proprietary features and may be used for future applications. The SD Status structure is described in *Section 4.10.2* in the SDA *Physical Layer Specification, Version 2.00*.

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3.5.6. Relative Card Address Register

The 16-bit **Relative Card Address (RCA)** Register carries the iNAND address published by the card during the card identification. Refer to Section 5.4 in the SDA *Physical Layer Specification, Version 2.00* for more information.

3.5.7. SD Card Configuration Register

The **SD Card Configuration Register (SCR)** is in addition to the CSD Register. The SCR provides information about special features in SanDisk iNAND. For more information, refer to *Section 5.6* in the SDA *Physical Layer Specification, Version 2.00*.

3.5.8. SD Card Registers in SPI Mode

All registers are accessible in SPI Mode. Their format is identical to the format in the SD Bus Mode, however a few fields are irrelevant in SPI Mode. In SPI Mode, the Card Status Register has a different, shorter, format as well. Refer to *Section 7.4* in the SDA *Physical Layer Specification, Version 2.00*. for more details.

3.6. Data Interchange Format and Card Sizes

In general, a file system provides structure for iNAND data. The SD Card File System Specification, published by the SD Association, describes the file format system implemented in the SanDisk iNAND.

Table 13 - User Area DOS Image Parameters

Capacity*	Total LBAs	Number of Partition System Area Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
8 GB	16,055,296	8192	16,047,104	16,038,912	3,073,376,256
4 GB	8,026,112	8192	8,017,920	8,009,728	4,100,980,736
2 GB	4,013,056	523	4,011,595	4,011,072	2,053,668,864
1 GB	2,006,528	523	2,005,675	2,005,152	1,026,637,824
512 MB	1,003,264	279	1,002,727	1,002,448	513,253,376

*1 megabyte (MB) = 1 million bytes; 1 gigabyte (GB) = 1 billion bytes. Some of the listed capacity is used for formatting and other functions, and thus is not available for data storage.

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4. iNAND PROTOCOL DESCRIPTION

4.1. General Description

iNAND protocol information is contained in this chapter; information includes bus protocol, card identification, and a functional description.

4.2. SD Bus Protocol

Communication over the SD bus is based on command and data-bit streams initiated by a start bit and terminated by a stop bit. See *Section 3.6.1* of the SDA *Physical Layer Specification, Version 2.00* for details.

4.3. Functional Description

The host controls all communication between itself and iNAND. To demonstrate how this communication works, this section provides a general overview of the identification and data transfer modes; commands; dependencies; various operation modes and restrictions for controlling the clock signal. All iNAND commands, together with corresponding responses, state transitions, error conditions, and timings are also provided. For detailed information, refer to *Section 4* of the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.1. Identification Mode

In Card Identification Mode the host resets all SD devices, validates operation voltage range, identifies and requests to publish a relative address. For more information see *Section 4.2* in the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.2. Data Transfer Mode

In Data Transfer Mode, the host may operate iNAND in the f_{PP} frequency range. This section contains information about data read and write, erase, write protect management, lock/unlock operations, application-specific commands, the switch function command, high-speed mode, the command system, the Send Interface Condition command (CMD8). CMD8 is part of identification mode and command functional differences in high capacity iNAND. For more detailed information, refer to *Section 4.3* of the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.3. Clock Control

The host can use the bus clock signal in iNAND to switch them to energy saving mode or to control data flow on the bus. See *Section 4.4* of the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.4. Cyclic Redundancy Codes

The Cyclic Redundancy Check (CRC) protects against transmission errors that may occur on the iNAND bus. Detailed information and examples for CRC7 and CRC16 are provided in *Section 4.5* of the SDA *Physical Layer Specification, Version 2.00*.

4.3.5. Error Conditions

See *Section 4.6* of the SDA *Physical Layer Specification, Version 2.00.*

4.3.6. Commands

See *Section 4.7* of the SDA *Physical Layer Specification*, *Version 2.00* for detailed information about iNAND commands.

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4.3.7. State Transition

The state transition is dependent on the received command. The transition is defined in *Section 4.8* of the SDA *Physical Layer Specification, Version 2.00* along with responses sent on the command line.

4.3.8. Timing Diagrams and Values

See *Section 4.12* of the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.9. Speed Class Specification

The speed class specification classifies performance by speed class number and offers the method to calculate performance. For more information, refer to *Section 4.13* of the SDA *Physical Layer Specification*, *Version 2.00*.

4.3.10. Erase Timeout Calculation

See *Section 4.14* of the SDA *Physical Layer Specification*, *Version 2.00*.

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5. APPENDIX - POWER DELIVERY AND CAPACITOR SPECIFICATIONS

5.1. SanDisk iNAND Power Domains

SanDisk iNAND has three power domains assigned to VDDH, VDDF, and CREG as shown in Table 14.

Table 14 - Power Domains

Pin	Power Domain	Comments
VDDH[3]	Host Interface	Supported voltage ranges:
		High Voltage Region: 3.3V (nominal)
		Low Voltage Region: 1.8V (nominal)
VDDF	Memory	Supported voltage range:
		High Voltage Region: 3.3V (nominal)
CREG	Internal	CREG is the internal regulator connection to an external decoupling capacitor.

5.2. Capacitor Connection Guidelines

5.2.1. CREG Connections

The CREG (K2) ball must only be connected to an external capacitor that is connected to VSS. This signal may not be left floating. The capacitor's specifications and its placement instructions are detailed below.

The capacitor is part of an internal voltage regulator that provides power to the controller.

Caution: Failure to follow the guidelines below or connecting the CREG ball to any external signal or power supply may cause the device to malfunction.

The trace requirements from the CREG (K2) ball to the capacitor are as follows:

- Resistance: <2 ohm
- Inductance: <5 nH

The capacitor requirements are as follows:

- Capacitance: >=2.2 uF
- Voltage Rating: >=6.3 V
- Dielectric: X7R or X5R

Currently both power domains can be connected to the same 3.3V (nom) power supply. However, in order to provide maximum flexibility and support low power operation in future iNAND devices, the PCB should be designed as follows:

- All VDDF balls should be connected to a 3.3V supply
- All VDDH balls should have the option of being connected either to a 3.3V or 1.8V supply

[3] Fully supported in MP devices, starting Q4 2007; in ES samples one of the following conditions must be applied: VDDF must be stable before VDDH rises OR VDDF and VDDH must rise together.

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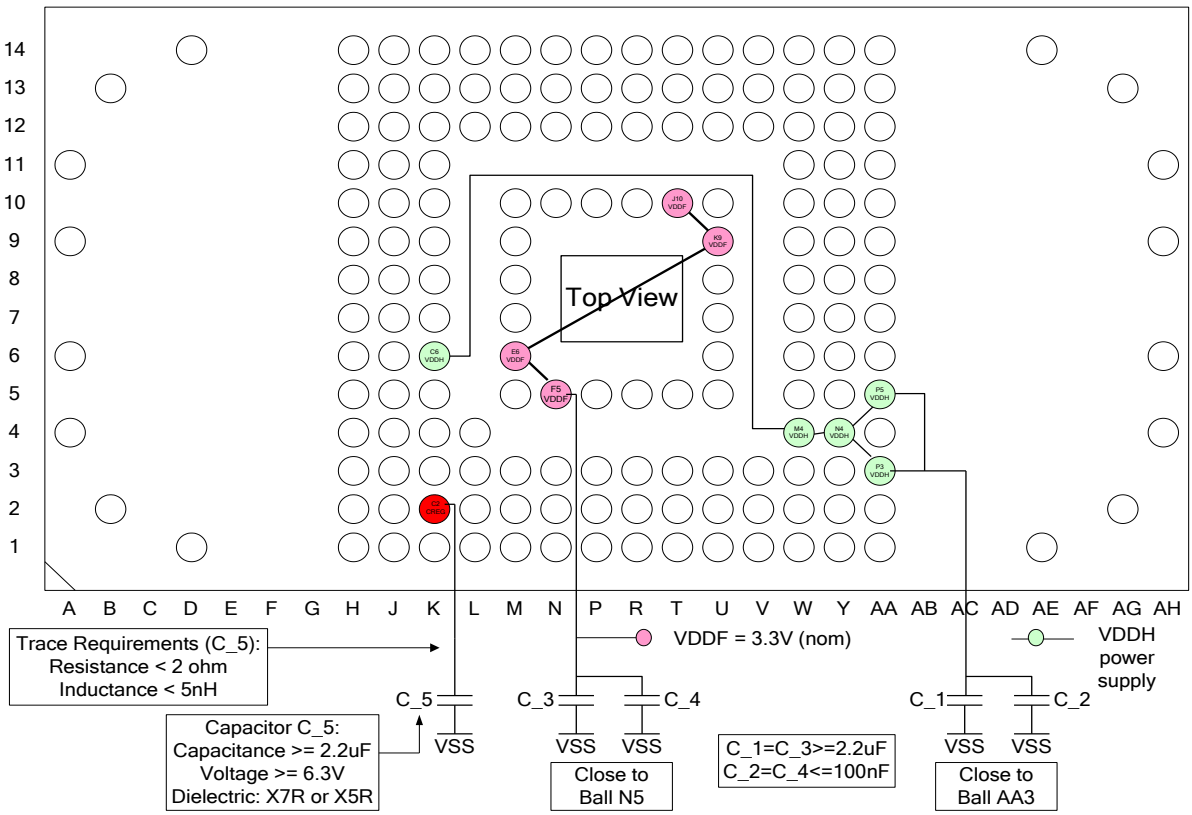
SanDisk recommends providing separate bypass capacitors for each power domain as shown in Figure 7.

Note: *Signal routing in the diagram is for illustration purposes only and the final routing depends on your PCB layout. Also, for clarity, the diagram does not show the VSS connection. All balls marked VSS should be connected to a ground (GND) plane.*

Figure 7 - Recommended Power Domain Connections



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6. APPENDIX - ORDERING INFORMATION

6.1. iNAND (JEDEC Package)

To order SanDisk products directly from SanDisk, call (408) 801-1000.

Table 15 – Ordering Information

Part Number	Capacity[4]
12 mm x 16 mm x 1.2 mm Package	
SDIN2C1-512M	512 MB
SDIN2C2-1G	1 GB
SDIN2C2-2G	2 GB
SDIN2C2-4G	4 GB
12 mm x 18 mm x 1.2 mm Package	
SDIN2B2-4G	4 GB
SDIN2B2-8G	8 GB

Note: If parts will be shipped by tape/reel, add "T" to the end of the part number. For example, SDIN2B2-8G would become SDIN2B2-8G-T.

[4] 1 megabyte (MB) = 1 million bytes; 1 gigabyte (GB) = 1 billion bytes. Some of the listed capacity is used for formatting and other functions, and thus is not available for data storage.

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7. DISCLAIMER OF LIABILITY

7.1. SanDisk Corporation Policy

SanDisk Corporation general policy does not recommend the use of its products in life support applications wherein a failure or malfunction of the product may directly threaten life or injury. Accordingly, in any use of products in life support systems or other applications where failure could cause damage, injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

SanDisk shall not be liable for any loss, injury or damage caused by use of the Products in any of the following applications:

- Special applications such as military related equipment, nuclear reactor control, and aerospace
- Control devices for automotive vehicles, train, ship and traffic equipment
- Safety system for disaster prevention and crime prevention
- Medical-related equipment including medical measurement device

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