具有可配置电压转换和三态输出的 SN74AXC8T245-Q1 汽车 8 位双电源总线收发器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
- 采用可湿侧面 QFN (WRGY) 封装
- 通过认证且完全可配置的双电源轨设计可允许各个端口在 0.65V 至 3.6V 的电源电压范围内运行
- 工作温度范围为 –40°C 至 +125°C
- 多向控制引脚，支持同步升降转换
- 从 1.8V 转换到 3.3V 时，支持高达 380Mbps 的转换速率
- V_{CC} 隔离功能可在断电情况下有效隔离两条总线
- 局部断电模式可在断电情况下限制回流电流
- 兼容 SN74AVC8T245-Q1 电平转换器
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- 信息娱乐系统音响主机
- ADAS 融合
- ADAS 前置摄像头
- HEV 电池管理系统

3 说明

通过 AEC-Q100 认证的 SN74AXC8T245-Q1 器件是一款 8 位同相总线收发器，可用于解决在最新电压节点（0.7V、0.8V 和 0.9V）上运行的器件与在业界通用电压节点（1.8V、2.5V 和 3.3V）上运行的器件之间的电压电平不匹配问题。

器件通过两条独立电源轨（V_{CCA} 和 V_{CCB}）运行，运行电压可低至 0.65V。数据引脚 A1 至 A8 均用于跟踪 V_{CCA}，可承受 0.65V-3.6V 的电源电压。数据引脚 B1 至 B8 均用于跟踪 V_{CCB}，可承受 0.65V-3.6V 的电源电压。

SN74AXC8T245-Q1 器件旨在实现数据总线间的异步通信。根据方向控制输入（DIR1 和 DIR2）的逻辑电平，此器件将数据从 A 总线传输至 B 总线，或者将数据从 B 总线传输至 A 总线。输出使能 ($\overline{OE}$) 输入可用于禁用输出，从而有效隔离总线。

SN74AXC8T245-Q1 器件旨在使控制引脚（DIR 和 $\overline{OE}$）以 V_{CCA} 为基准。

该器件专用于使用 I_{off} 的局部断电应用。当器件断电时，I_{off} 电路将会禁用输出。这会抑制电流反流到器件中，从而防止损坏器件。

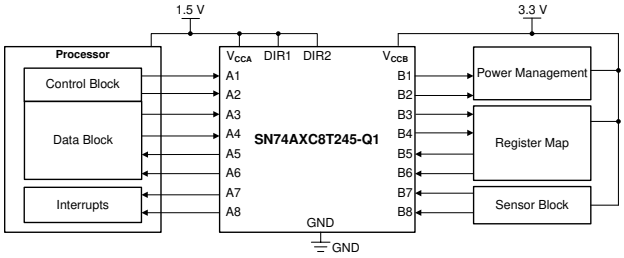
V_{CC} 隔离功能可确保当任一 V_{CC} 输入电源低于 100mV 时，所有电平转换器输出都将禁用并处于高阻抗状态。

为了确保电平转换器 I/O 在上电或断电期间处于高阻抗状态，应将 $\overline{OE}$ 通过上拉电阻器接到 V_{CCA}；此电阻器的最小值由驱动器的灌电流能力决定。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
SN74AXC8T245PW-Q1	TSSOP (24)	4.40mm × 7.80mm
SN74AXC8T245RHL-Q1	VQFN (24)	3.50mm × 5.50mm
SN74AXC8T245WRGY-Q1	VQFN (24)	3.50mm × 5.50mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



典型应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (May 2021) to Revision C (October 2021) — **Page**

- 重新编排了*器件信息*表 ... 1
- 在*特性*中添加了可湿性侧面信息 ... 1
- Added wettable flank information in *Feature Description* ... 21

Changes from Revision A (July 2019) to Revision B (May 2021) — **Page**

- 向*器件信息*表添加了 SN74AXC8T245QRGYQ1 器件型号 ... 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 ... 1
- Added the *RGY Package* to the *Pin Configuration and Functions* section ... 3
- Added the *RGY Package* to the *Thermal Information* section ... 5

Changes from Revision * (November 2018) to Revision A (July 2019) — **Page**

- 将状态更改为量产数据 ... 1
- Added Typical Characteristics graphs for Production Data release. ... 17

5 Pin Configuration and Functions

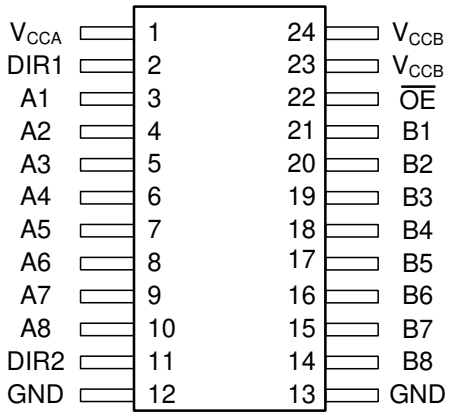
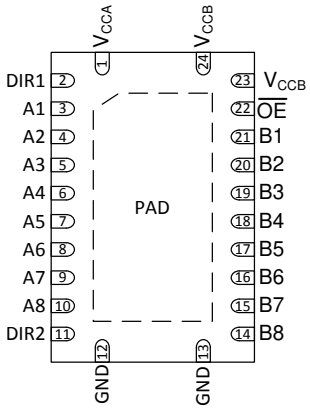


图 5-1. PW Package 24-Pin TSSOP Top View



PAD — may be grounded (recommended) or left floating.

图 5-2. RHL and WRGY Package 24-Pin VQFN Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	PW, RHL, WRGY		
A1	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR1	2	I	Direction-control signal 1. Referenced to V_{CCA}. Refer to 表 8-1.
DIR2	11	I	Direction-control signal 2. Refer to 表 8-1. Referenced to V_{CCA}. Tie to GND to maintain backward compatibility with SN74AVC8T245-Q1 device.
GND	12	—	Ground
	13	—	Ground
$\overline{OE}$	22	I	Output Enable. Pull to GND to enable all outputs. Pull to V_{CCA} to place all outputs in high-impedance mode. Referenced to V_{CCA}. Refer to 表 8-1.
V_{CCA}	1	—	A-port supply voltage. 0.65 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V
	24	—	B-port supply voltage. 0.65 V ≤ V_{CCB} ≤ 3.6 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		– 0.5	4.2	V
Supply voltage, V_{CCB}		– 0.5	4.2	V
Input voltage, V_I (2)	I/O ports (A port)	– 0.5	4.2	V
	I/O ports (B port)	– 0.5	4.2	
	Control inputs	– 0.5	4.2	
Voltage applied to any output in the high-impedance or power-off state, V_O (2)	A port	– 0.5	4.2	V
	B port	– 0.5	4.2	
Voltage applied to any output in the high or low state, V_O (2) (3)	A port	– 0.5	V_{CCA} + 0.2	V
	B port	– 0.5	V_{CCB} + 0.2	
Input clamp current, I_{IK}	V_I < 0	– 50		mA
Output clamp current, I_{OK}	V_O < 0	– 50		mA
Continuous output current, I_O		– 50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		– 100	100	mA
Junction Temperature, T_J			150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under 节 6.3. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±8000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			0.65	3.6	V
V_{CCB}	Supply voltage			0.65	3.6	V
V_{IH}	High-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V	V_{CCI} × 0.70		V
			V_{CCI} = 0.76 V - 1 V	V_{CCI} × 0.70		
			V_{CCI} = 1.1 V - 1.95 V	V_{CCI} × 0.65		
			V_{CCI} = 2.3 V - 2.7 V	1.6		
			V_{CCI} = 3 V - 3.6 V	2		
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V	V_{CCA} × 0.70		
			V_{CCA} = 0.76 V - 1 V	V_{CCA} × 0.70		
			V_{CCA} = 1.1 V - 1.95 V	V_{CCA} × 0.65		
			V_{CCA} = 2.3 V - 2.7 V	1.6		
			V_{CCA} = 3 V - 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs	V_{CCI} = 0.65 V - 0.75 V		V_{CCI} × 0.30	V
			V_{CCI} = 0.76 V - 1 V		V_{CCI} × 0.30	
			V_{CCI} = 1.1 V - 1.95 V		V_{CCI} × 0.35	
			V_{CCI} = 2.3 V - 2.7 V		0.7	
			V_{CCI} = 3 V - 3.6 V		0.8	
		Control inputs (DIR, $\overline{OE}$) Referenced to V_{CCA}	V_{CCA} = 0.65 V - 0.75 V		V_{CCA} × 0.30	
			V_{CCA} = 0.76 V - 1 V		V_{CCA} × 0.30	
			V_{CCA} = 1.1 V - 1.95 V		V_{CCA} × 0.35	
			V_{CCA} = 2.3 V - 2.7 V		0.7	
			V_{CCA} = 3 V - 3.6 V		0.8	
V_I	Input voltage(3)			0	3.6	V
V_O	Output voltage	Active state		0	V_{CCO} (2)	V
		Tri-state		0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature			– 40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AXC8T245-Q1			UNIT
		PW (TSSOP)	RHL (VQFN)	WRGY (VQFN)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	35.0	48.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.3	39.9	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	13.8	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	0.3	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.2	13.8	26.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1.4	15.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	– 40°C to 85°C			– 40°C to 125°C			UNIT
						MIN	TYP(4)	MAX	MIN	TYP(4)	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = – 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = – 50 µA	0.65 V	0.65 V	0.55			0.55			
			I_{OH} = – 200 µA	0.76 V	0.76 V	0.58			0.58			
			I_{OH} = – 500 µA	0.85 V	0.85 V	0.65			0.65			
			I_{OH} = -3 mA	1.1 V	1.1 V	0.85			0.85			
			I_{OH} = -6 mA	1.4 V	1.4 V	1.05			1.05			
			I_{OH} = -8 mA	1.65 V	1.65 V	1.2			1.2			
			I_{OH} = -9 mA	2.3 V	2.3 V	1.75			1.75			
			I_{OH} = -12 mA	3 V	3 V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100 µA	0.7 V - 3.6 V	0.7 V - 3.6 V			0.1			0.1	V
			I_{OL} = 50 µA	0.65 V	0.65 V			0.1			0.1	
			I_{OL} = 200 µA	0.76 V	0.76 V			0.18			0.18	
			I_{OL} = 500 µA	0.85 V	0.85 V			0.2			0.2	
			I_{OL} = 3 mA	1.1 V	1.1 V			0.25			0.25	
			I_{OL} = 6 mA	1.4 V	1.4 V			0.35			0.35	
			I_{OL} = 8 mA	1.65 V	1.65 V			0.45			0.45	
			I_{OL} = 9 mA	2.3 V	2.3 V			0.55			0.55	
			I_{OL} = 12 mA	3 V	3 V			0.7			0.7	
I_I	Input leakage current	Control Inputs (DIR, $\overline{OE}$): $V_I = V_{CCA}$ or GND		0.65 V - 3.6 V	0.65 V - 3.6 V	-0.5		0.5	-1		1	µA
I_{off}	Partial power down current	A Port: V_I or V_O = 0 V - 3.6 V		0 V	0 V - 3.6 V	-8		8	-12		12	µA
		B Port: V_I or V_O = 0 V - 3.6 V		0 V - 3.6 V	0 V	-8		8	-12		12	
I_{OZ} (3)	High-impedance state output current	A Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	-8		8	-12		12	µA
		B Port: $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	-8		8	-12		12	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			20			40	µA
				0 V	3.6 V	-2			-12			
				3.6 V	0 V			12			25	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			20			40	µA
				0 V	3.6 V			12			25	
				3.6 V	0 V	-2			-12			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0 mA		0.65 V - 3.6 V	0.65 V - 3.6 V			30			60	µA
C_i	Input capacitance	Control Inputs (DIR, $\overline{OE}$): V_I = 3.3 V or GND		3.3 V	3.3 V		4.5			4.5		pF
C_{io}	Data I/O capacitance	Ports A and B: $\overline{OE} = V_{CCA}$, V_O = 1.65V DC + 1 MHz -16 dBm sine wave		3.3 V	3.3 V		5.7			5.7		pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) All typical values are for T_A = 25°C

6.6 Switching Characteristics, V_{CCA} = 0.7 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	172	0.5	114	0.5	82	0.5	49	ns
			–40°C to 125°C	0.5	172	0.5	114	0.5	82	0.5	49	
		From input B to output A	–40°C to 85°C	0.5	172	0.5	153	0.5	126	0.5	88	
			–40°C to 125°C	0.5	172	0.5	153	0.5	126	0.5	88	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
			–40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	156	0.5	129	0.5	118	0.5	120	
			–40°C to 125°C	0.5	157	0.5	129	0.5	120	0.5	122	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	ns
			–40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	223	0.5	145	0.5	106	0.5	74	
			–40°C to 125°C	0.5	223	0.5	145	0.5	106	0.5	74	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	46	0.5	49	0.5	61	0.5	142	ns
			–40°C to 125°C	0.5	46	0.5	49	0.5	61	0.5	142	
		From input B to output A	–40°C to 85°C	0.5	83	0.5	82	0.5	81	0.5	81	
			–40°C to 125°C	0.5	83	0.5	82	0.5	81	0.5	81	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	192	0.5	192	0.5	192	0.5	192	ns
			–40°C to 125°C	0.5	195	0.5	195	0.5	195	0.5	195	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	69	0.5	66	0.5	67	0.5	150	
			–40°C to 125°C	0.5	70	0.5	67	0.5	67	0.5	150	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	237	0.5	237	0.5	237	0.5	237	ns
			–40°C to 125°C	0.5	237	0.5	237	0.5	237	0.5	237	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	68	0.5	69	0.5	84	0.5	552	
			–40°C to 125°C	0.5	68	0.5	69	0.5	84	0.5	552	

6.7 Switching Characteristics, V_{CCA} = 0.8 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	153	0.5	95	0.5	62	0.5	32	ns
			–40°C to 125°C	0.5	153	0.5	95	0.5	62	0.5	32	
		From input B to output A	–40°C to 85°C	0.5	114	0.5	95	0.5	78	0.5	52	
			–40°C to 125°C	0.5	114	0.5	95	0.5	78	0.5	52	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	ns
			–40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	141	0.5	114	0.5	104	0.5	106	
			–40°C to 125°C	0.5	142	0.5	115	0.5	106	0.5	109	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	ns
			–40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	202	0.5	124	0.5	86	0.5	52	
			–40°C to 125°C	0.5	202	0.5	124	0.5	86	0.5	52	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	26	0.5	25	0.5	25	0.5	35	ns
			–40°C to 125°C	0.5	26	0.5	25	0.5	25	0.5	35	
		From input B to output A	–40°C to 85°C	0.5	42	0.5	41	0.5	40	0.5	40	
			–40°C to 125°C	0.5	42	0.5	41	0.5	40	0.5	40	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	101	0.5	101	0.5	101	0.5	101	ns
			–40°C to 125°C	0.5	103	0.5	103	0.5	103	0.5	103	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	55	0.5	51	0.5	49	0.5	51	
			–40°C to 125°C	0.5	57	0.5	53	0.5	50	0.5	52	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	102	0.5	102	0.5	102	0.5	102	ns
			–40°C to 125°C	0.5	102	0.5	102	0.5	102	0.5	102	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	44	0.5	43	0.5	45	0.5	58	
			–40°C to 125°C	0.5	44	0.5	43	0.5	45	0.5	58	

6.8 Switching Characteristics, V_{CCA} = 0.9 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	127	0.5	78	0.5	52	0.5	23	ns
			–40°C to 125°C	0.5	127	0.5	78	0.5	52	0.5	23	
		From input B to output A	–40°C to 85°C	0.5	82	0.5	63	0.5	52	0.5	39	
			–40°C to 125°C	0.5	82	0.5	63	0.5	52	0.5	39	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	131	0.5	105	0.5	96	0.5	99	
			–40°C to 125°C	0.5	133	0.5	107	0.5	98	0.5	101	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	191	0.5	113	0.5	75	0.5	41	
			–40°C to 125°C	0.5	191	0.5	113	0.5	75	0.5	41	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	17	0.5	15	0.5	14	0.5	17	ns
			–40°C to 125°C	0.5	17	0.5	15	0.5	14	0.5	17	
		From input B to output A	–40°C to 85°C	0.5	28	0.5	24	0.5	22	0.5	22	
			–40°C to 125°C	0.5	28	0.5	24	0.5	22	0.5	22	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	125	0.5	125	0.5	125	0.5	125	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	47	0.5	44	0.5	40	0.5	73	
			–40°C to 125°C	0.5	50	0.5	46	0.5	42	0.5	73	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	124	0.5	124	0.5	124	0.5	124	ns
			–40°C to 125°C	0.5	128	0.5	128	0.5	128	0.5	128	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	34	0.5	32	0.5	31	0.5	35	
			–40°C to 125°C	0.5	34	0.5	32	0.5	31	0.5	35	

6.9 Switching Characteristics, V_{CCA} = 1.2 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	88	0.5	52	0.5	39	0.5	15	ns
			–40°C to 125°C	0.5	88	0.5	52	0.5	39	0.5	15	
		From input B to output A	–40°C to 85°C	0.5	49	0.5	32	0.5	23	0.5	15	
			–40°C to 125°C	0.5	49	0.5	32	0.5	23	0.5	15	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	ns
			–40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	119	0.5	94	0.5	85	0.5	89	
			–40°C to 125°C	0.5	121	0.5	96	0.5	88	0.5	93	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	168	0.5	98	0.5	61	0.5	29	
			–40°C to 125°C	0.5	168	0.5	98	0.5	61	0.5	30	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	10	0.5	9	0.5	7	0.5	7	ns
			–40°C to 125°C	0.5	10	0.5	9	0.5	7	0.5	8	
		From input B to output A	–40°C to 85°C	0.5	13	0.5	11	0.5	8	0.5	7	
			–40°C to 125°C	0.5	13	0.5	11	0.5	8	0.5	7	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	87	0.5	87	0.5	87	0.5	87	ns
			–40°C to 125°C	0.5	91	0.5	91	0.5	91	0.5	91	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	38	0.5	35	0.5	31	0.5	29	
			–40°C to 125°C	0.5	41	0.5	38	0.5	33	0.5	31	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	36	0.5	36	0.5	36	0.5	36	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	22	0.5	19	0.5	17	0.5	17	
			–40°C to 125°C	0.5	23	0.5	20	0.5	18	0.5	18	

6.10 Switching Characteristics, V_{CCA} = 1.5 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	84	0.5	42	0.5	28	0.5	13	ns
			–40°C to 125°C	0.5	84	0.5	42	0.5	28	0.5	13	
		From input B to output A	–40°C to 85°C	0.5	46	0.5	26	0.5	17	0.5	10	
			–40°C to 125°C	0.5	46	0.5	26	0.5	17	0.5	10	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	115	0.5	89	0.5	80	0.5	85	
			–40°C to 125°C	0.5	117	0.5	91	0.5	83	0.5	89	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	ns
			–40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	159	0.5	90	0.5	55	0.5	24	
			–40°C to 125°C	0.5	159	0.5	90	0.5	55	0.5	25	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	ns
			–40°C to 125°C	0.5	9	0.5	7	0.5	6	0.5	6	
		From input B to output A	–40°C to 85°C	0.5	9	0.5	7	0.5	6	0.5	5	
			–40°C to 125°C	0.5	9	0.5	8	0.5	6	0.5	5	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	34	0.5	34	0.5	34	0.5	34	ns
			–40°C to 125°C	0.5	37	0.5	37	0.5	37	0.5	37	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	35	0.5	31	0.5	28	0.5	25	
			–40°C to 125°C	0.5	38	0.5	34	0.5	31	0.5	27	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	21	0.5	21	0.5	21	0.5	21	ns
			–40°C to 125°C	0.5	23	0.5	23	0.5	23	0.5	23	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	17	0.5	15	0.5	12	0.5	11	
			–40°C to 125°C	0.5	18	0.5	15	0.5	13	0.5	12	

6.11 Switching Characteristics, V_{CCA} = 1.8 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	82	0.5	41	0.5	24	0.5	11	ns
			–40°C to 125°C	0.5	82	0.5	41	0.5	24	0.5	11	
		From input B to output A	–40°C to 85°C	0.5	49	0.5	25	0.5	15	0.5	9	
			–40°C to 125°C	0.5	49	0.5	25	0.5	15	0.5	9	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	113	0.5	87	0.5	78	0.5	83	
			–40°C to 125°C	0.5	115	0.5	89	0.5	81	0.5	87	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	ns
			–40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	157	0.5	88	0.5	54	0.5	23	
			–40°C to 125°C	0.5	157	0.5	88	0.5	54	0.5	23	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	8	0.5	6	0.5	5	0.5	5	ns
			–40°C to 125°C	0.5	8	0.5	7	0.5	6	0.5	5	
		From input B to output A	–40°C to 85°C	0.5	7	0.5	6	0.5	5	0.5	4	
			–40°C to 125°C	0.5	7	0.5	7	0.5	5	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	37	0.5	37	0.5	37	0.5	37	ns
			–40°C to 125°C	0.5	40	0.5	40	0.5	40	0.5	40	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	33	0.5	30	0.5	27	0.5	57	
			–40°C to 125°C	0.5	36	0.5	33	0.5	29	0.5	60	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	17	0.5	17	0.5	17	0.5	17	ns
			–40°C to 125°C	0.5	19	0.5	19	0.5	19	0.5	19	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	15	0.5	13	0.5	10	0.5	9	
			–40°C to 125°C	0.5	16	0.5	14	0.5	11	0.5	10	

6.12 Switching Characteristics, V_{CCA} = 2.5 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	8	ns
			–40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	8	
		From input B to output A	–40°C to 85°C	0.5	61	0.5	25	0.5	14	0.5	7	
			–40°C to 125°C	0.5	61	0.5	25	0.5	14	0.5	7	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	111	0.5	85	0.5	76	0.5	81	
			–40°C to 125°C	0.5	113	0.5	87	0.5	78	0.5	84	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	155	0.5	86	0.5	52	0.5	21	
			–40°C to 125°C	0.5	155	0.5	86	0.5	52	0.5	21	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	–40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	ns
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
		From input B to output A	–40°C to 85°C	0.5	6	0.5	5	0.5	4	0.5	4	
			–40°C to 125°C	0.5	6	0.5	5	0.5	5	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	25	0.5	25	0.5	25	0.5	25	ns
			–40°C to 125°C	0.5	28	0.5	28	0.5	28	0.5	28	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	31	0.5	28	0.5	25	0.5	23	
			–40°C to 125°C	0.5	34	0.5	31	0.5	28	0.5	25	
t_{en}	Enable time	From input $\overline{OE}$ to output A	–40°C to 85°C	0.5	11	0.5	11	0.5	11	0.5	11	ns
			–40°C to 125°C	0.5	12	0.5	12	0.5	12	0.5	12	
		From input $\overline{OE}$ to output B	–40°C to 85°C	0.5	14	0.5	11	0.5	9	0.5	7	
			–40°C to 125°C	0.5	14	0.5	12	0.5	9	0.5	8	

6.13 Switching Characteristics, V_{CCA} = 3.3 V

See 图 7-1 and 图 7-2 for test circuit and loading conditions. See 图 7-3 and 图 7-4 for measurement waveforms.

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				0.7 V ± 0.05 V		0.8 V ± 0.04 V		0.9 V ± 0.045 V		1.2 V ± 0.1 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	– 40°C to 85°C	0.5	81	0.5	40	0.5	22	0.5	7	ns
			– 40°C to 125°C	0.5	81	0.5	40	0.5	22	0.5	7	
		From input B to output A	– 40°C to 85°C	0.5	142	0.5	35	0.5	17	0.5	7	
			– 40°C to 125°C	0.5	142	0.5	35	0.5	17	0.5	8	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	– 40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	ns
			– 40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
		From input $\overline{OE}$ to output B	– 40°C to 85°C	0.5	111	0.5	84	0.5	75	0.5	80	
			– 40°C to 125°C	0.5	113	0.5	86	0.5	78	0.5	83	
t_{en}	Enable time	From input $\overline{OE}$ to output A	– 40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	ns
			– 40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
		From input $\overline{OE}$ to output B	– 40°C to 85°C	0.5	154	0.5	86	0.5	51	0.5	20	
			– 40°C to 125°C	0.5	154	0.5	86	0.5	51	0.5	20	

PARAMETER		TEST CONDITIONS		B-PORT SUPPLY VOLTAGE (V_{CCB})								UNIT
				1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay	From input A to output B	– 40°C to 85°C	0.5	5	0.5	4	0.5	4	0.5	4	ns
			– 40°C to 125°C	0.5	5	0.5	4	0.5	4	0.5	4	
		From input B to output A	– 40°C to 85°C	0.5	5	0.5	5	0.5	4	0.5	4	
			– 40°C to 125°C	0.5	6	0.5	5	0.5	4	0.5	4	
t_{dis}	Disable time	From input $\overline{OE}$ to output A	– 40°C to 85°C	0.5	22	0.5	22	0.5	22	0.5	22	ns
			– 40°C to 125°C	0.5	24	0.5	24	0.5	24	0.5	24	
		From input $\overline{OE}$ to output B	– 40°C to 85°C	0.5	30	0.5	27	0.5	25	0.5	23	
			– 40°C to 125°C	0.5	33	0.5	30	0.5	27	0.5	25	
t_{en}	Enable time	From input $\overline{OE}$ to output A	– 40°C to 85°C	0.5	9	0.5	9	0.5	9	0.5	9	ns
			– 40°C to 125°C	0.5	10	0.5	10	0.5	10	0.5	10	
		From input $\overline{OE}$ to output B	– 40°C to 85°C	0.5	13	0.5	10	0.5	8	0.5	7	
			– 40°C to 125°C	0.5	14	0.5	11	0.5	8	0.5	7	

6.14 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.5		
C_{pdA}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.1		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.1		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		9.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		11.8		
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		12		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		13		
			V_{CCA} = V_{CCB} = 2.5 V		16.4		
			V_{CCA} = V_{CCB} = 3.3 V		18.1		
C_{pdA}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.6		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.2		
			V_{CCA} = V_{CCB} = 0.9 V		1.1		
			V_{CCA} = V_{CCB} = 1.2 V		1.2		
			V_{CCA} = V_{CCB} = 1.5 V		1.2		
			V_{CCA} = V_{CCB} = 1.8 V		1.3		
			V_{CCA} = V_{CCB} = 2.5 V		1.6		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		

6.14 Operating Characteristics: T_A = 25°C (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		9.3		pF
			V_{CCA} = V_{CCB} = 0.8 V		11.7		
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		11.9		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		12.9		
			V_{CCA} = V_{CCB} = 2.5 V		16.3		
			V_{CCA} = V_{CCB} = 3.3 V		18		
C_{pdB}	Power dissipation capacitance per transceiver (A to B: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		2.6		
			V_{CCA} = V_{CCB} = 0.8 V		11.7		pF
			V_{CCA} = V_{CCB} = 0.9 V		11.8		
			V_{CCA} = V_{CCB} = 1.2 V		11.9		
			V_{CCA} = V_{CCB} = 1.5 V		12.2		
			V_{CCA} = V_{CCB} = 1.8 V		12.9		
			V_{CCA} = V_{CCB} = 2.5 V		16.3		
			V_{CCA} = V_{CCB} = 3.3 V		3.9		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs enabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.2		pF
			V_{CCA} = V_{CCB} = 0.8 V		1.8		
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.5		
C_{pdB}	Power dissipation capacitance per transceiver (B to A: outputs disabled)	C_L = 0, R_L = Open f = 1 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 0.7 V		1.1		
			V_{CCA} = V_{CCB} = 0.8 V		1.8		pF
			V_{CCA} = V_{CCB} = 0.9 V		1.8		
			V_{CCA} = V_{CCB} = 1.2 V		1.7		
			V_{CCA} = V_{CCB} = 1.5 V		1.7		
			V_{CCA} = V_{CCB} = 1.8 V		1.7		
			V_{CCA} = V_{CCB} = 2.5 V		2		
			V_{CCA} = V_{CCB} = 3.3 V		2.1		

6.15 Typical Characteristics

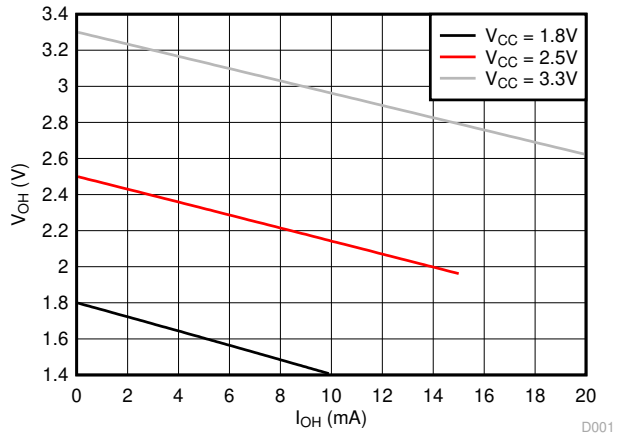


图 6-1. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

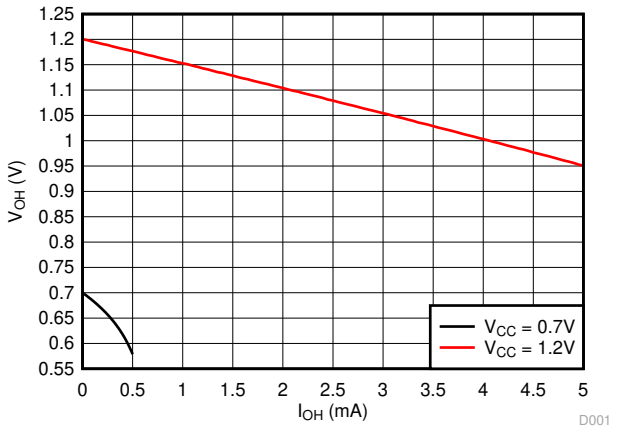


图 6-2. Typical (T_A=25°C) Output High Voltage (V_{OH}) vs Source Current (I_{OH})

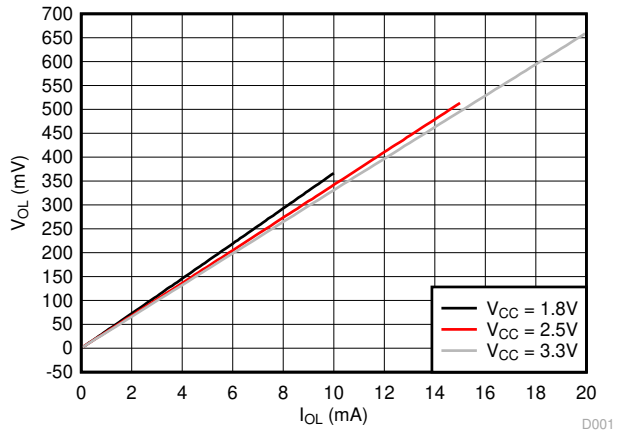


图 6-3. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

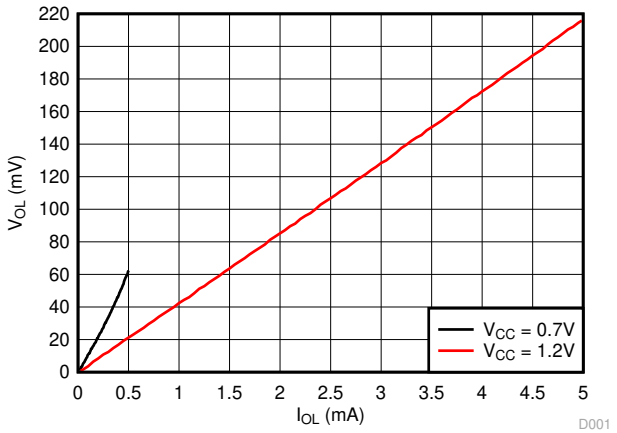
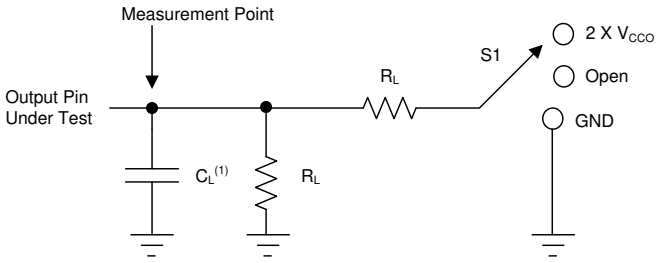


图 6-4. Typical (T_A=25°C) Output High Voltage (V_{OL}) vs Sink Current (I_{OL})

7 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f =1 MHz
- Z_0 = 50 Ω
- dv / dt ⩽ 1 ns/V



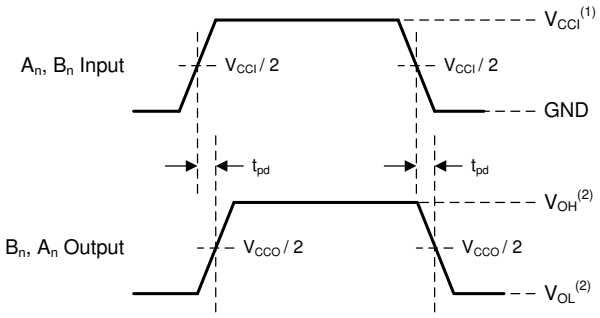
A. C_L includes probe and jig capacitance.

图 7-1. Load Circuit

Parameter	V_{CCO}	R_L	C_L	S1	V_{TP}
t_{pd}	1.1 V - 3.6 V	2 kΩ	15 pF	Open	N/A
	0.65 V - 0.95 V	20 kΩ	15 pF	Open	N/A
t_{en}(1), t_{dis}(1)	3 V - 3.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.3 V
	1.65 V - 2.7 V	2 kΩ	15 pF	2 X V_{CCO}	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	2 X V_{CCO}	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	2 X V_{CCO}	0.1 V
t_{en}(2), t_{dis}(2)	3 V - 3.6 V	2 kΩ	15 pF	GND	0.3 V
	1.65V - 2.7 V	2 kΩ	15 pF	GND	0.15 V
	1.1 V - 1.6 V	2 kΩ	15 pF	GND	0.1 V
	0.65 V - 0.95 V	20 kΩ	15 pF	GND	0.1 V

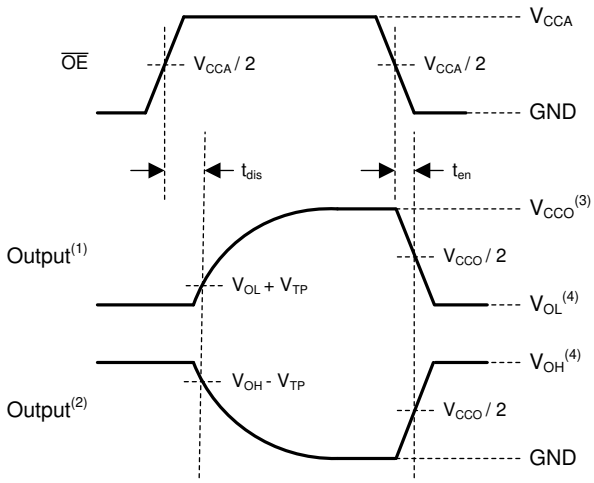
A. Output waveform on the conditions that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.

图 7-2. Load Circuit Conditions



A. V_{CCI} is the supply pin associated with the input port.
B. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

图 7-3. Propagation Delay



A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. V_{CCO} is the supply pin associated with the output port.
D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.

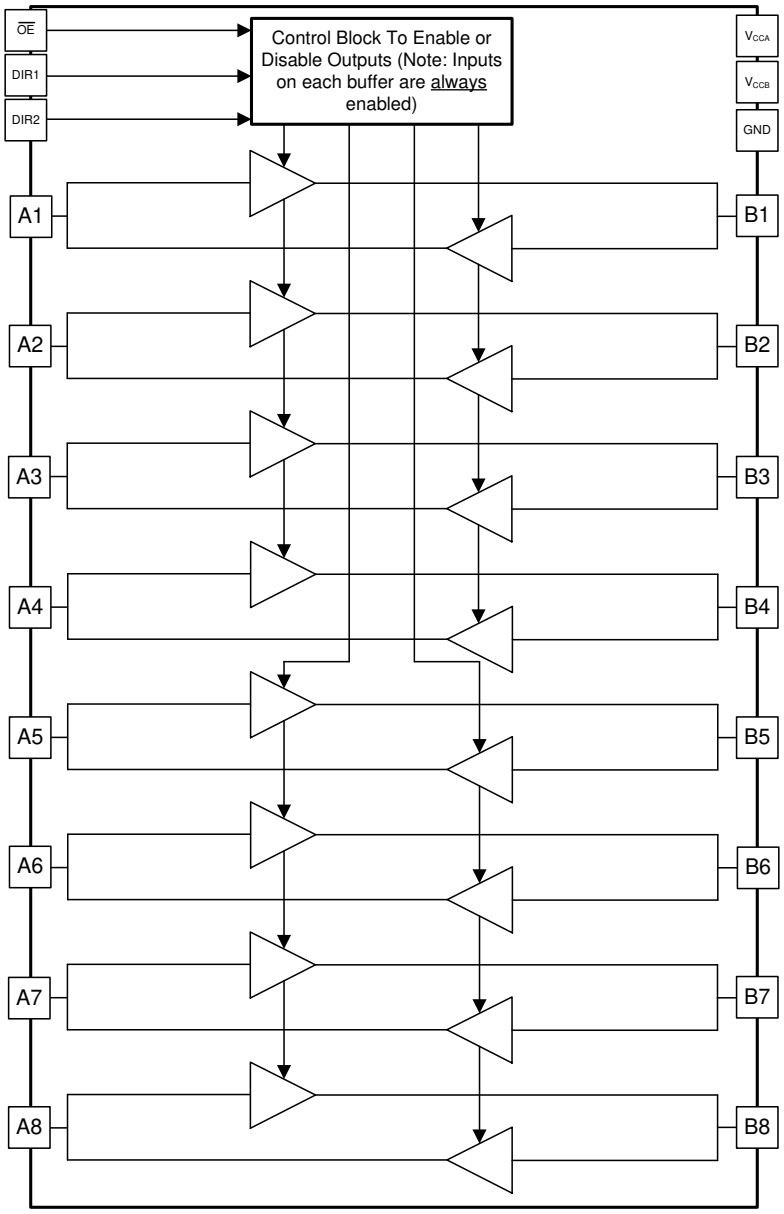
图 7-4. Enable Time And Disable Time

8 Detailed Description

8.1 Overview

The SN74AXC8T245-Q1 device is an 8-bit, dual-supply non-inverting transceiver with bidirectional voltage level translation. The I/O pins labeled with A and the control pins (DIR1, DIR2, and $\overline{OE}$) are supported by V_{CCA}, and the I/O pins labeled with B are supported by V_{CCB}. The A port and the B port are able to accept I/O voltages ranging from 0.65 V to 3.6 V.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Up-Translation and Down-Translation From 0.65 V to 3.6 V

Both supply pins are configured from 0.65 V to 3.6 V, which makes the device suitable for translating between any of the low voltage nodes (0.7 V, 0.8 V, 0.9 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V).

8.3.2 Multiple Direction Control Pins

Two control pins are used to configure the 8 data I/Os. I/O channels 1 through 4 are grouped together and I/O channels 5 through 8 are banked together. The benefit of this is to permit simultaneous up-translation and down-translation within one device. This eliminates the need for multiple devices, where each device can only provide up-translation or down-translation sequentially. Simultaneous up and down translation is supported when both V_{CCA} and V_{CCB} are at least 1.40 V.

8.3.3 I_{off} Supports Partial-Power-Down Mode Operation

This feature is to limit the leakage current of an I/O pin being driven to a voltage as large as 3.6 V while having its corresponding power supply rail powered down. This is represented by the I_{off} parameter in the *Electrical Characteristics* table.

8.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

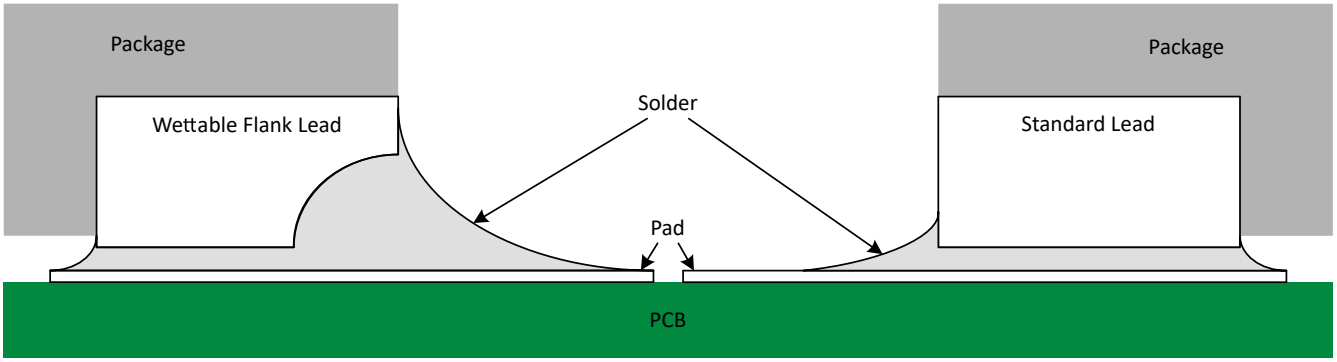


图 8-1. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in 图 8-1. Please see the mechanical drawing for additional details.

8.4 Device Functional Modes

All control inputs are referenced to V_{CCA} and must be driven to a valid Logic High or Logic Low (that is, not floating) to assure proper device operation and to prevent excessive power consumption. 表 8-1 summarizes the possible modes of device operation based on the configuration of the control inputs.

表 8-1. Function Table

CONTROL INPUTS(1)			Signal Direction	
$\overline{OE}$	DIR1	DIR2	Bits 1:4	Bits 5:8
H	X	X	Disabled (Hi-Z)	
L	L	L	B to A	
L	L	H	B to A	A to B
L	H	L	A to B	
L	H	H	A to B	B to A

(1) Input circuits of the data I/Os are always active and must be driven to a valid logic level.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The AEC-Q100 qualified SN74AXC8T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different voltage nodes. Figure 9-1 depicts an application in which the SN74AXC8T245-Q1 device is up-translating a 0.7 V input to a 3.3 V output to interface between a system controller and a peripheral device.

9.2 Typical Application

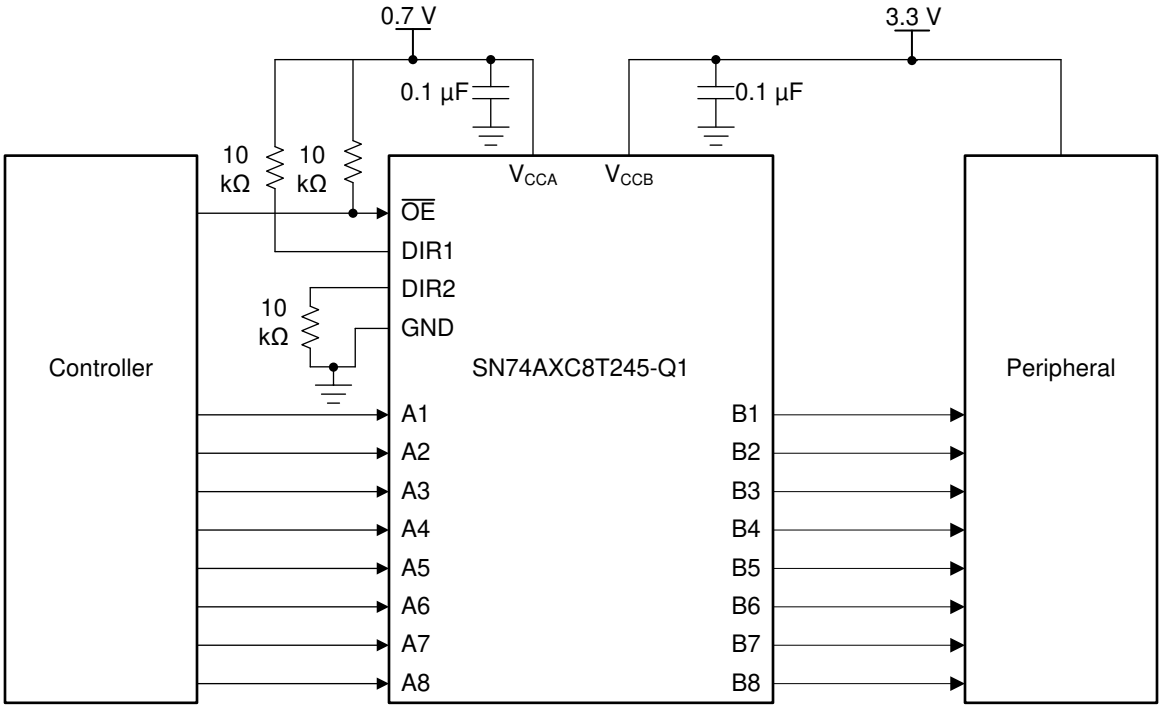


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.65 V to 3.6 V
Output voltage range	0.65 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC8T245-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC8T245-Q1 device is driving to determine the output voltage range.

9.2.3 Application Curve

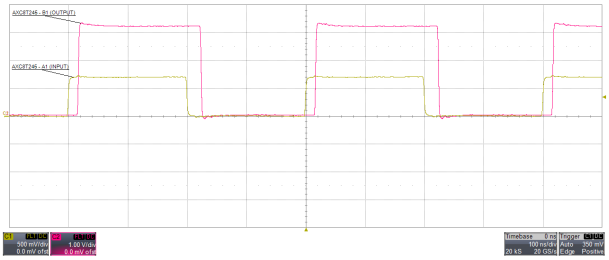


图 9-2. Translation Up (0.7 V to 3.3 V) at 2.5 MHz

10 Power Supply Recommendations

Always apply a ground reference to the GND pins first. There are no additional requirements for power supply sequencing.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report.

11 Layout

11.1 Layout Guidelines

To assure reliability of the device, follow common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

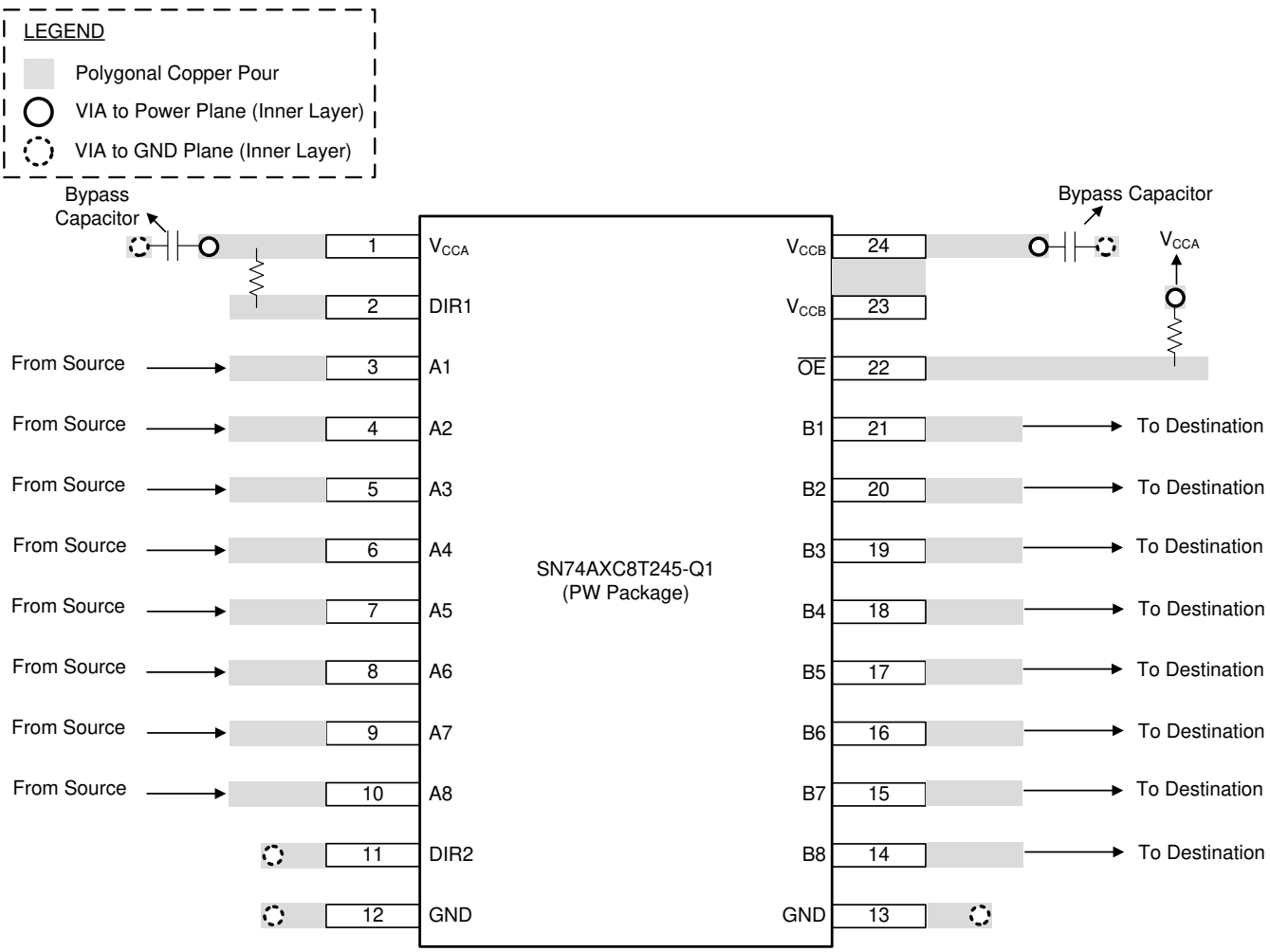


图 11-1. SN74AXC8T245-Q1 Device Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *SN74AXC8245-Q1 Evaluation Module* user's guide
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Power Sequencing for AXC Family of Devices* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAXC8T245QRHLRQ1	ACTIVE	VQFN	RHL	24	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q	Samples
CAXC8T245QWRGYRQ1	ACTIVE	VQFN	RGY	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	AX8T245Q	Samples
SN74AXC8T245QPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AX8T245Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AXC8T245-Q1 :

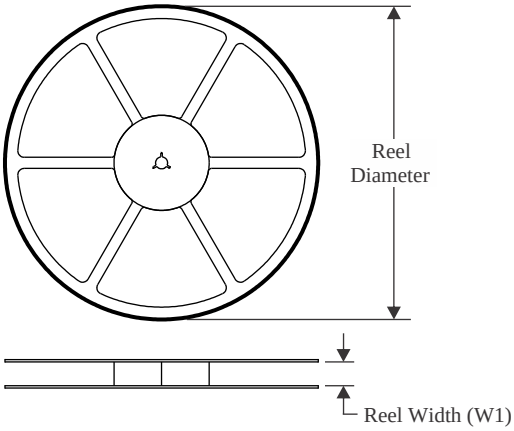
- Catalog : SN74AXC8T245

NOTE: Qualified Version Definitions:

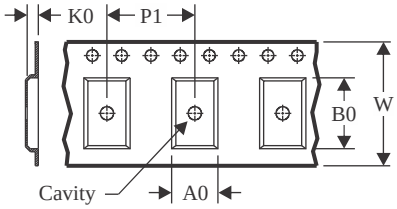
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

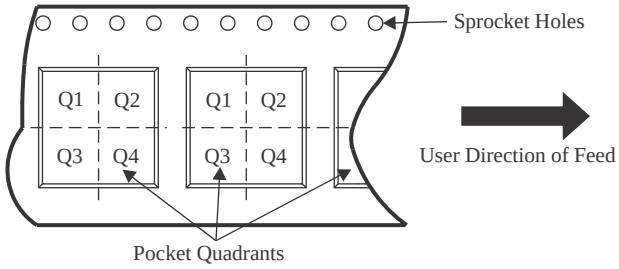


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

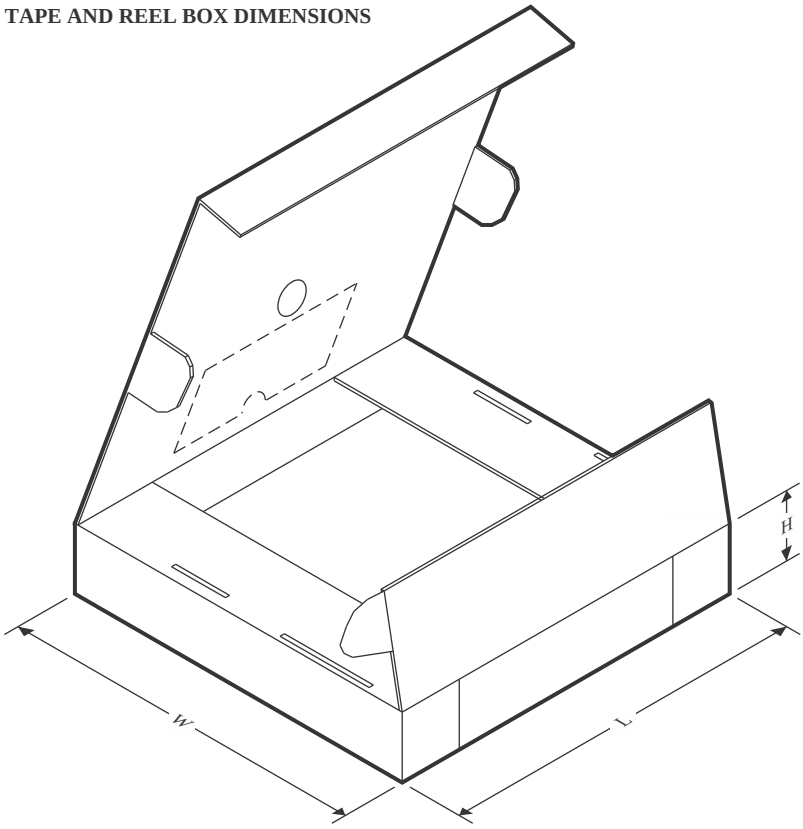
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAXC8T245QRHLRQ1	VQFN	RHL	24	1000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
CAXC8T245QWRGYRQ1	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AXC8T245QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

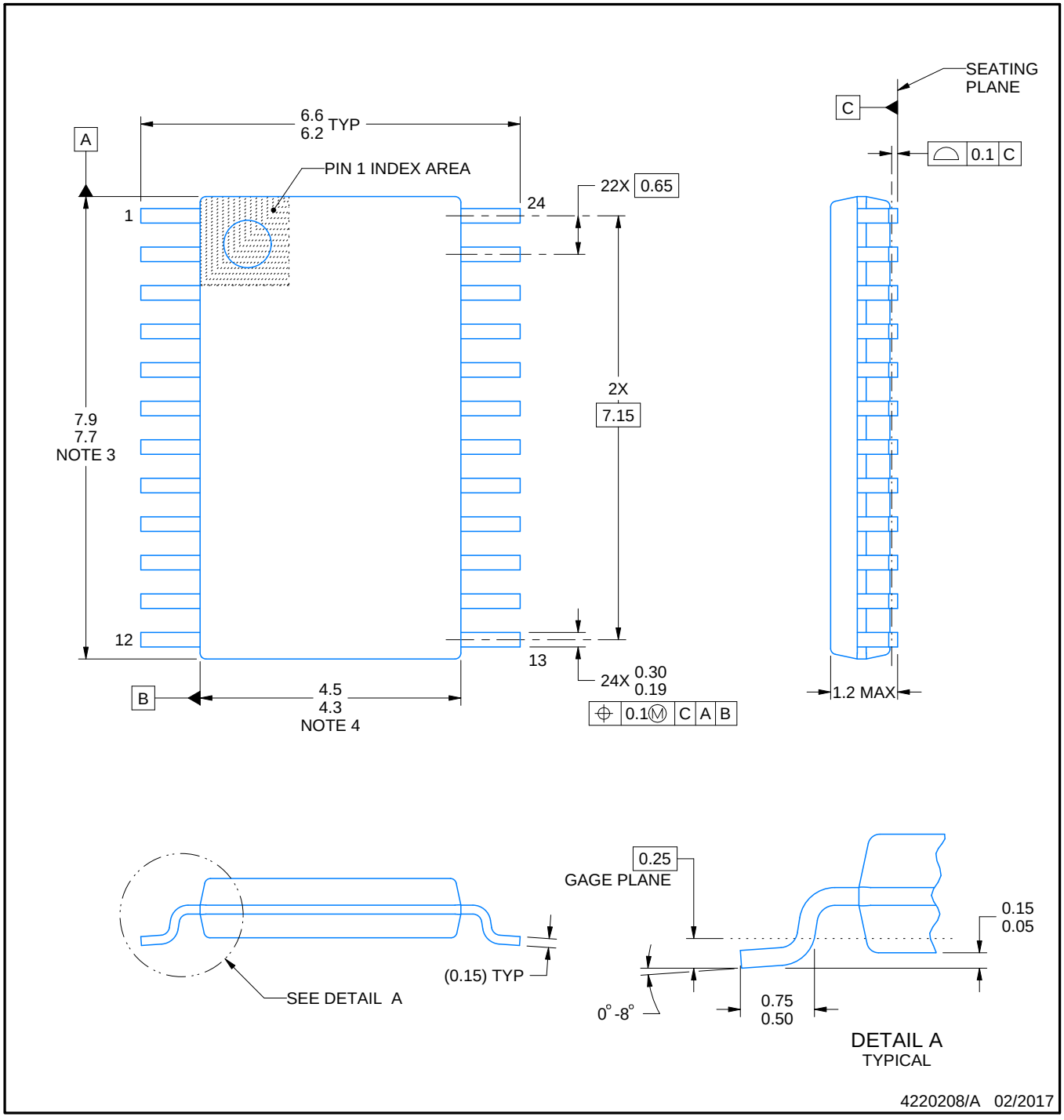
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAXC8T245QRHLRQ1	VQFN	RHL	24	1000	367.0	367.0	35.0
CAXC8T245QWRGYRQ1	VQFN	RGY	24	3000	367.0	367.0	35.0
SN74AXC8T245QPWRQ1	TSSOP	PW	24	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0024A

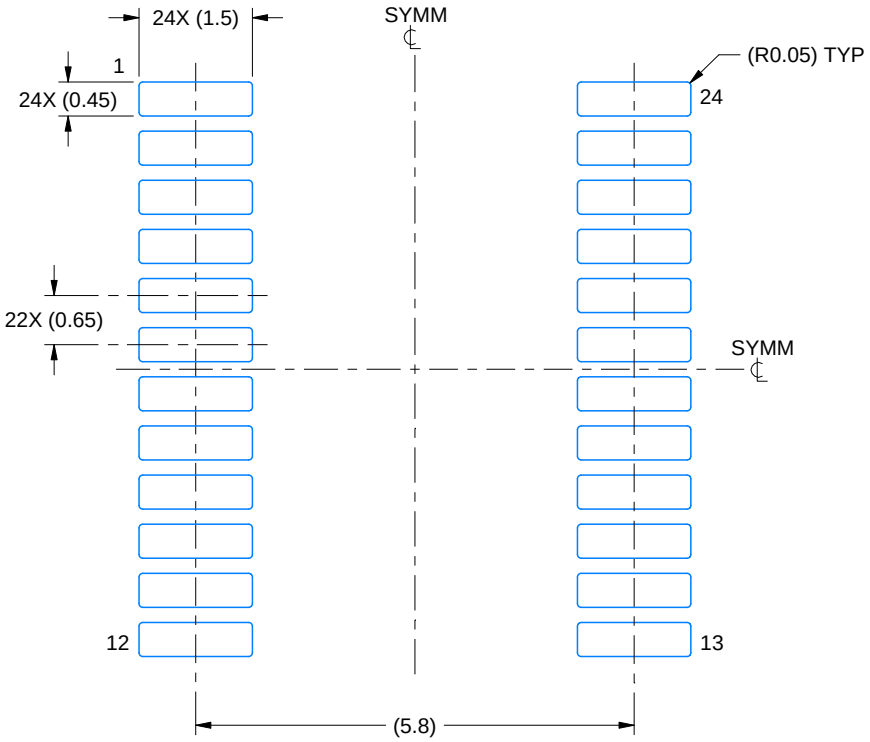
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

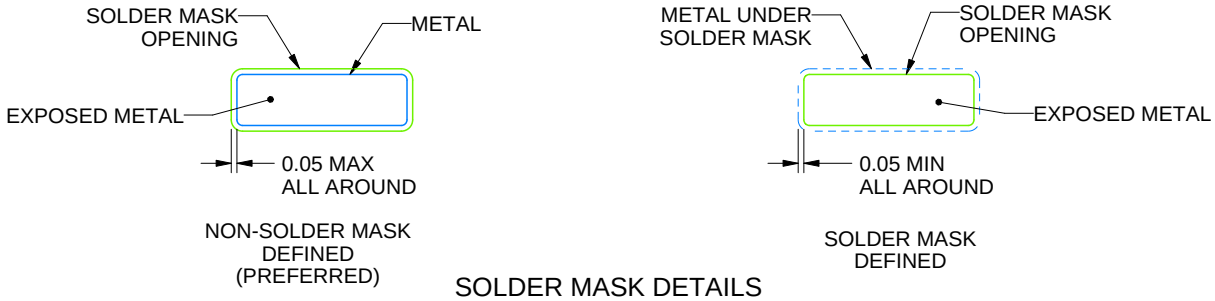


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

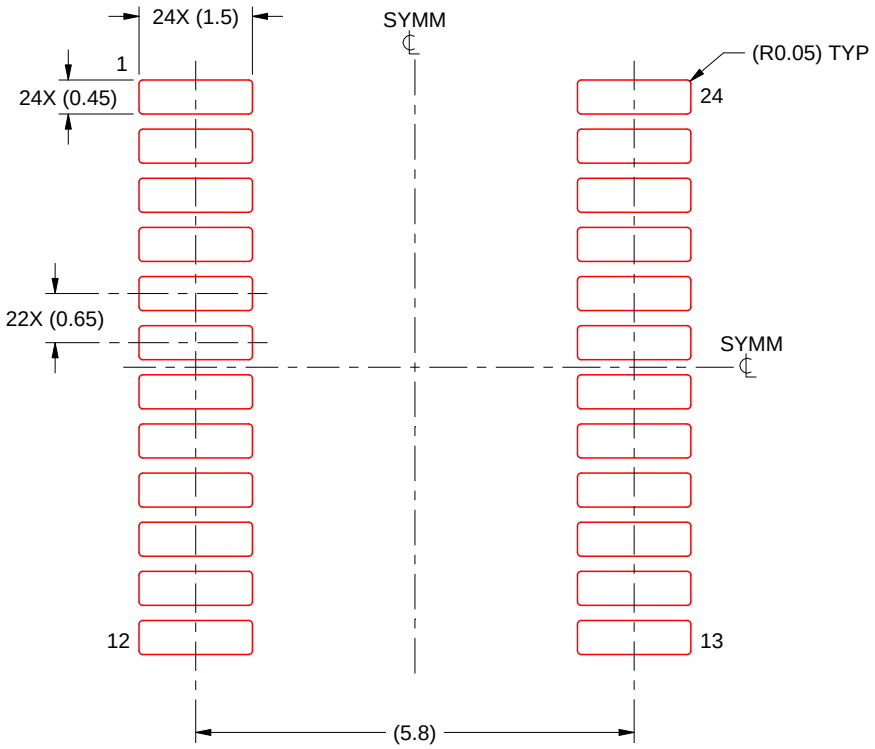


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

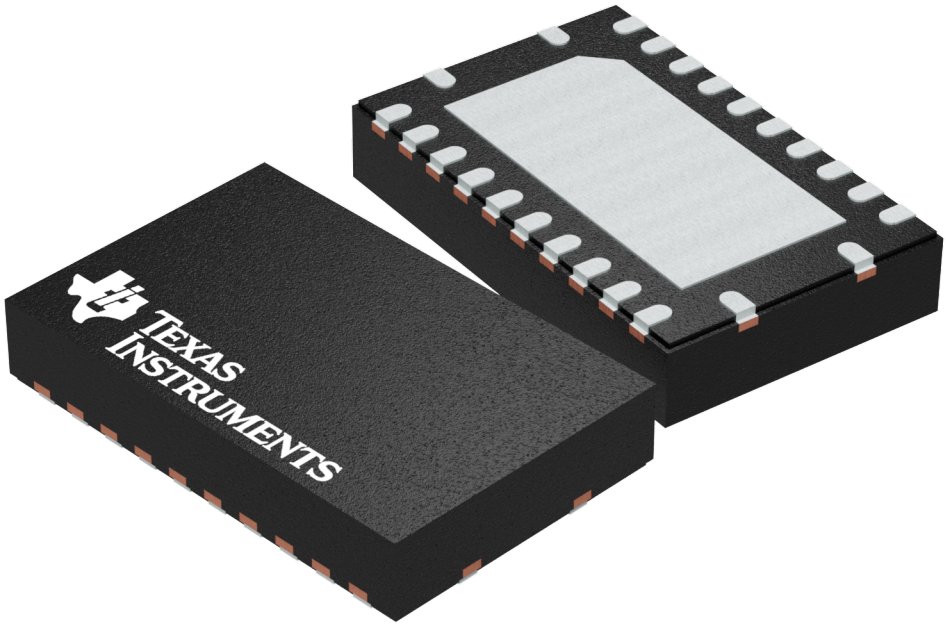
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY 24

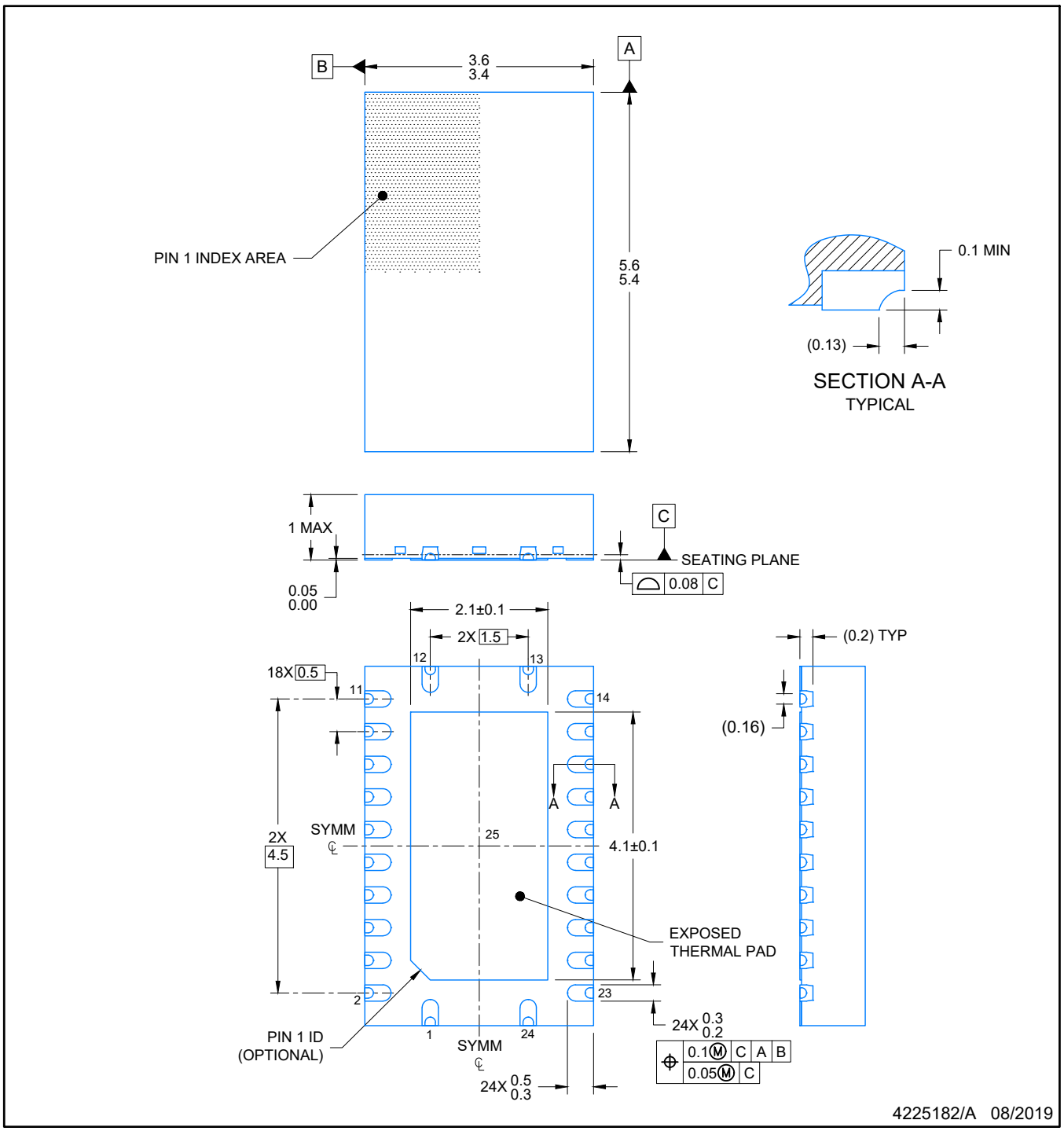
VQFN - 1 mm max height

5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

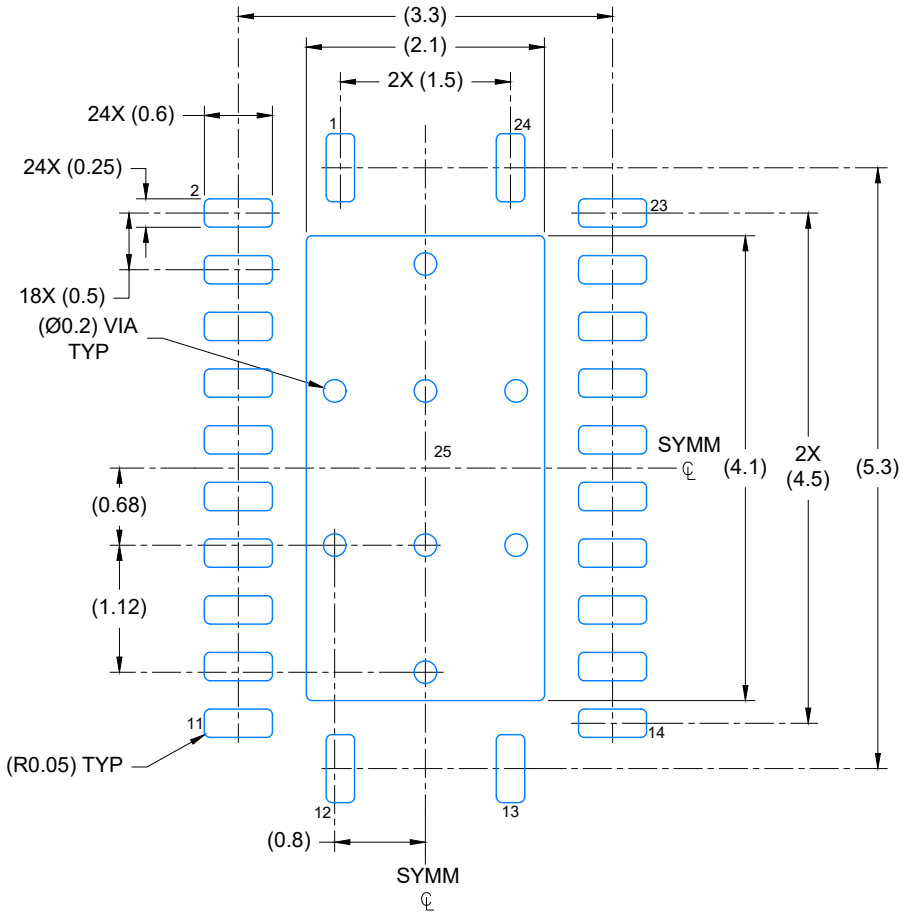


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

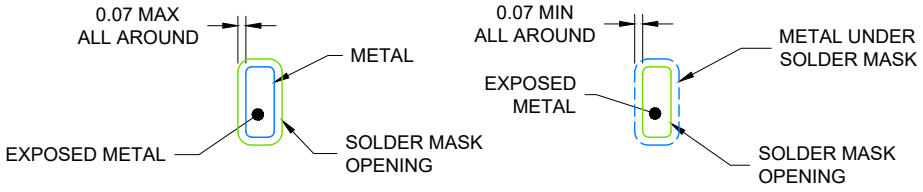


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

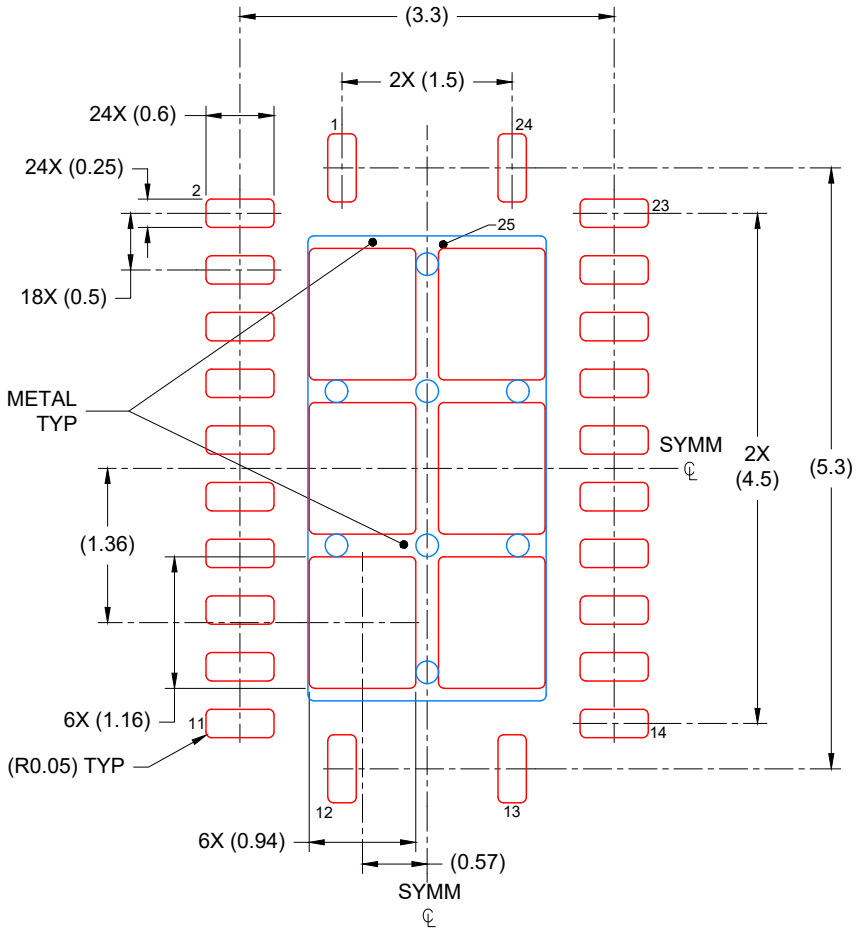
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4225182/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

4225182/A 08/2019

NOTES: (continued)

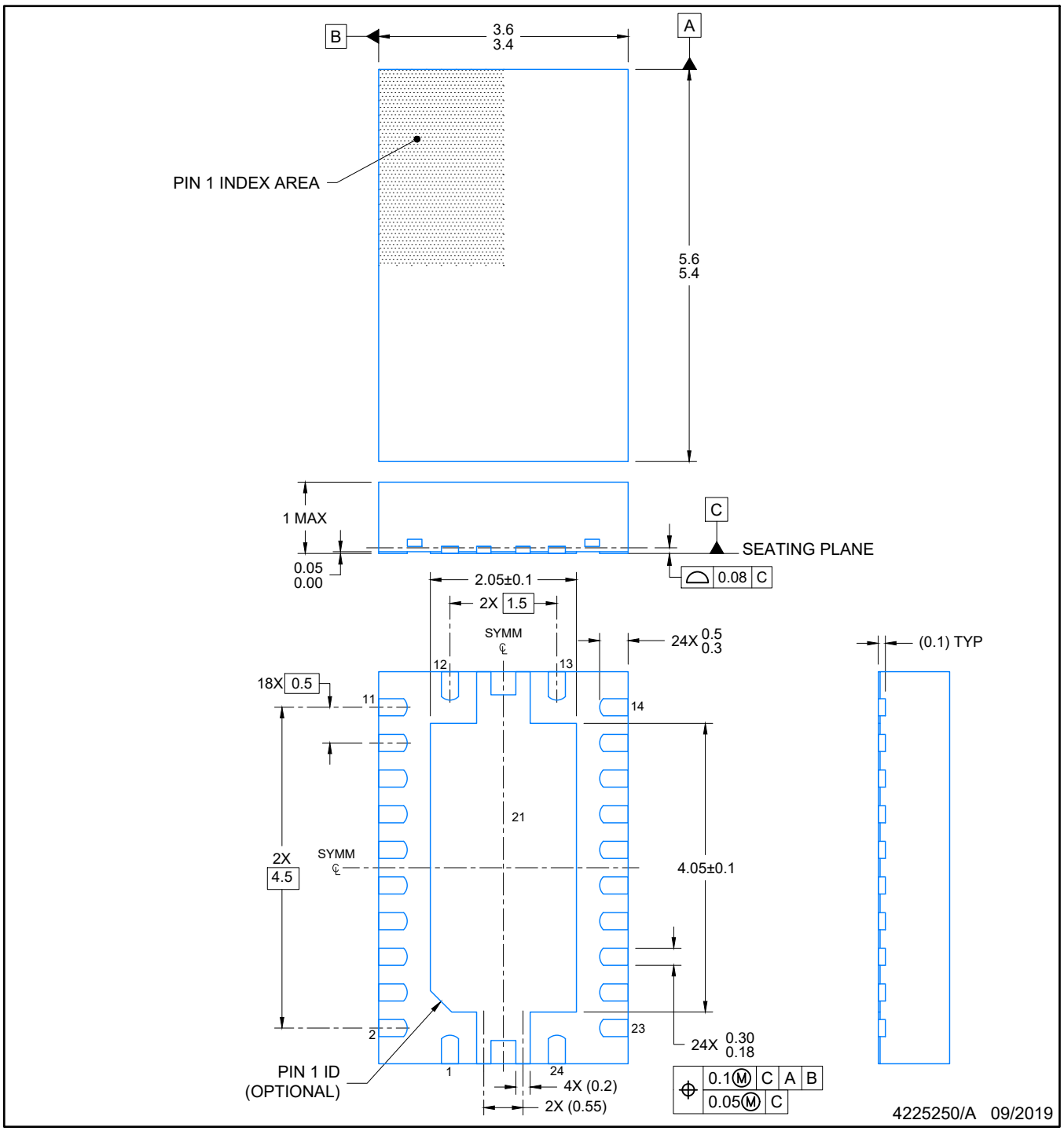
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RHL0024A

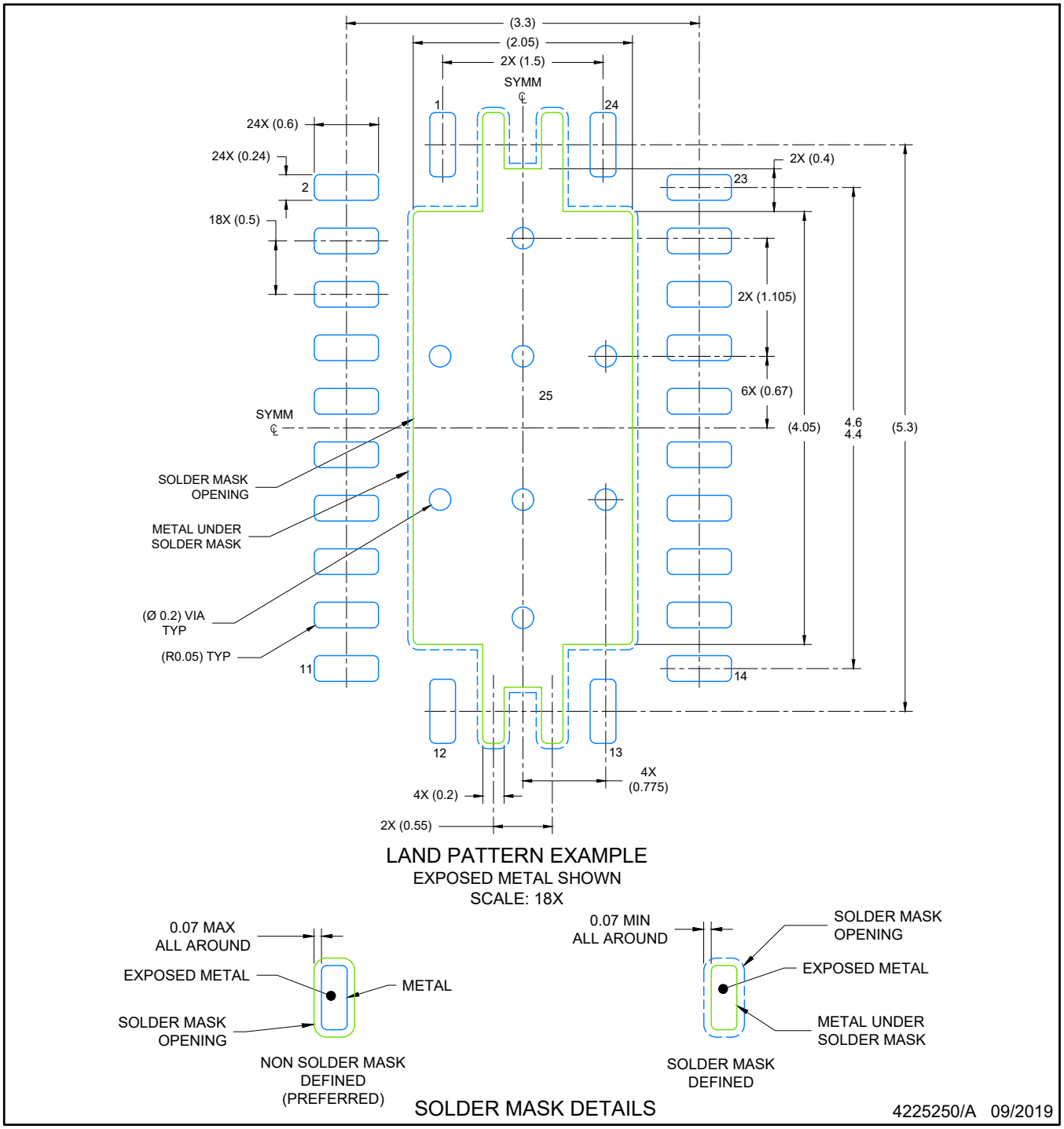
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



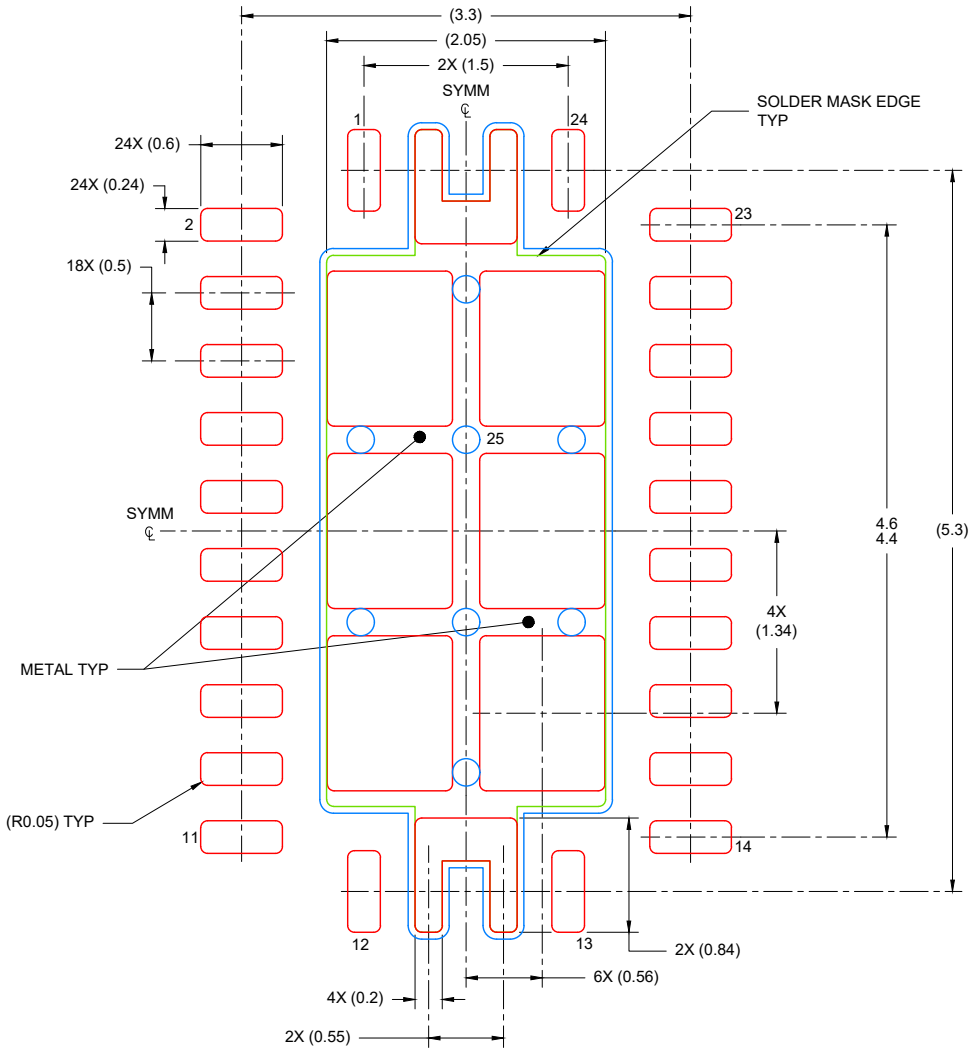
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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